

FIELD DATA

Shadowed fields:

```
fldoffset[0] = 0x00, fldmask[0] = 0x00, fldvalue_dyna[0]: 0x00 0x00
0x00 0x00
fldcontrol[0].inuse = 0x0  fldcontrol[0].refcnt = 0x00 0x00 0x00
0x00
fldoffset[1] = 0x00, fldmask[1] = 0x00, fldvalue_dyna[1]: 0x00 0x00
0x00 0x00
fldcontrol[1].inuse = 0x0  fldcontrol[1].refcnt = 0x00 0x00 0x00
0x00
fldoffset[2] = 0x00, fldmask[2] = 0x00, fldvalue_dyna[2]: 0x00 0x00
0x00 0x00
fldcontrol[2].inuse = 0x0  fldcontrol[2].refcnt = 0x00 0x00 0x00
0x00
fldoffset[3] = 0x00, fldmask[3] = 0x00, fldvalue_dyna[3]: 0x00 0x00
0x00 0x00
fldcontrol[3].inuse = 0x0  fldcontrol[3].refcnt = 0x00 0x00 0x00
0x00
fldoffset[4] = 0x00, fldmask[4] = 0x00, fldvalue_dyna[4]: 0x00 0x00
0x00 0x00
fldcontrol[4].inuse = 0x0  fldcontrol[4].refcnt = 0x00 0x00 0x00
0x00
fldoffset[5] = 0x00, fldmask[5] = 0x00, fldvalue_dyna[5]: 0x00 0x00
0x00 0x00
fldcontrol[5].inuse = 0x0  fldcontrol[5].refcnt = 0x00 0x00 0x00
0x00
fldoffset[6] = 0x00, fldmask[6] = 0x00, fldvalue_dyna[6]: 0x00 0x00
0x00 0x00
fldcontrol[6].inuse = 0x0  fldcontrol[6].refcnt = 0x00 0x00 0x00
0x00
fldoffset[7] = 0x00, fldmask[7] = 0x00, fldvalue_dyna[7]: 0x00 0x00
0x00 0x00
fldcontrol[7].inuse = 0x0  fldcontrol[7].refcnt = 0x00 0x00 0x00
0x00
fldoffset[8] = 0x00, fldmask[8] = 0x00, fldvalue_dyna[8]: 0x00 0x00
0x00 0x00
fldcontrol[8].inuse = 0x0  fldcontrol[8].refcnt = 0x00 0x00 0x00
0x00
fldoffset[9] = 0x00, fldmask[9] = 0x00, fldvalue_dyna[9]: 0x00 0x00
0x00 0x00
fldcontrol[9].inuse = 0x0  fldcontrol[9].refcnt = 0x00 0x00 0x00
0x00
fldoffset[10] = 0x00, fldmask[10] = 0x00, fldvalue_dyna[10]: 0x00 0x00
0x00 0x00
fldcontrol[10].inuse = 0x0  fldcontrol[10].refcnt = 0x00 0x00 0x00
0x00
fldoffset[11] = 0x00, fldmask[11] = 0x00, fldvalue_dyna[11]: 0x00 0x00
0x00 0x00
fldcontrol[11].inuse = 0x0  fldcontrol[11].refcnt = 0x00 0x00 0x00
```


0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000

Field dirty indicator: 0x00000000

FDB reference count fdb: 0 [0 0 0 0]
FDB reference count fdb: 1 [0 0 0 0]
FDB reference count fdb: 2 [0 0 0 0]
FDB reference count fdb: 3 [0 0 0 0]
FDB reference count fdb: 4 [0 0 0 0]
FDB reference count fdb: 5 [0 0 0 0]
FDB reference count fdb: 6 [0 0 0 0]
FDB reference count fdb: 7 [0 0 0 0]
FDB reference count fdb: 8 [0 0 0 0]
FDB reference count fdb: 9 [0 0 0 0]
FDB reference count fdb: 10 [0 0 0 0]
FDB reference count fdb: 11 [0 0 0 0]
FDB reference count fdb: 12 [0 0 0 0]
FDB reference count fdb: 13 [0 0 0 0]
FDB reference count fdb: 14 [0 0 0 0]
FDB reference count fdb: 15 [0 0 0 0]
FDB reference count fdb: 16 [0 0 0 0]
FDB reference count fdb: 17 [0 0 0 0]
FDB reference count fdb: 18 [0 0 0 0]
FDB reference count fdb: 19 [0 0 0 0]

Filter counters:

Filter counter 0: 0 (MIRROR1)
Filter counter 1: 0 (MIRROR2)
Filter counter 2: 0 (MIRROR3)
Filter counter 3: 0 (MIRROR4)
Filter counter 4: 0 (AEPORT_NON_MIRR_DROP)
Filter counter 5: 0 (ZONING TRAP)
Filter counter 6: 0 (FCR_EXPORT_DC)
Filter counter 7: 0 (TIN TRAP)
Filter counter 8: 0 (FICON CUP)
Filter counter 9: 0 (FICON CUP DST)
Filter counter 10: 0 (WELL KNOWN ADDR)
Filter counter 11: 0 (SIM)
Filter counter 12: 0 (UNUSED)
Filter counter 13: 0 (UNUSED)
Filter counter 14: 0 (UNUSED)
Filter counter 15: 0 (UNUSED)
Filter counter 16: 0 (PERF1)
Filter counter 17: 0 (PERF2)
Filter counter 18: 0 (PERF3)
Filter counter 19: 0 (PERF4)
Filter counter 20: 0 (PERF5)
Filter counter 21: 0 (PERF6)
Filter counter 22: 0 (PERF7)

Filter counter 23: 0 (PERF8)
Filter counter 24: 0 (PERF9)
Filter counter 25: 0 (PERF10)
Filter counter 26: 0 (PERF11)
Filter counter 27: 0 (PERF12)
Filter counter 28: 0 (OPM1)
Filter counter 29: 0 (OPM2)
Filter counter 30: 0 (IPM1)
Filter counter 31: 0 (IPM2)

ACL DATA

Logical port 24: Hard Zoning disabled, Soft Zoning disabled
Zone type: WWN Zoning
Frames with hard zone miss: 0

*** Please use filterportshow on user port 56 to display ACL hash tables and Mirroring resources of thischip.
***We show this data only for the first physical port which is an external port.

portFcPortCmdShow --slot 0 36 3
doing portFcPortCmdShow: arg1 = 3, arg2 = -2

portshow 36
portDisableReason: None
portCFlags: 0x1
portFlags: 0x10000907 PRESENT ACTIVE E_PORT G_PORT U_PORT
LOGICAL_ONLINE LOGIN
LocalSwcFlags: 0x0
portType: 26.0
POD Port: Port is licensed
portState: 1 Online
Protocol: FC
portPhys: 6 In_Sync portScn: 16 E_Port Flow
control mode 4
port generation number: 0
state transition count: 2

portId: 012400
portIfId: 4302001e
portWwn: 20:24:d8:1f:cc:2c:99:90
portWwn of device(s) connected:
16b Area list:
Distance: normal
portSpeed: N16Gbps

FEC: Active
Credit Recovery: Active
LE domain: 0
Peer beacon: Off
FC Fastwrite: OFF
Interrupts: 0 Link_failure: 0 Frjt:
0

```

Unknown:          0          Loss_of_sync: 0          Fbsy:
0
Lli:              0          Loss_of_sig:  0
Proc_rqrd:       65821      Protocol_err:  0
Timed_out:       0          Invalid_word:  0
Tx_unavail:      0          Invalid_crc:   0
Delim_err:       0          Address_err:   0
Lr_in:           0          Ols_in:        0
Lr_out:          0          Ols_out:       0

```

```

portloginshow 36
Type  PID      World Wide Name      credit df_sz cos
=====

```

```

portloginshow 36 -history
Type  PID      World Wide Name      logout time
=====

```

```
portregshow 36
```

```
LED registers
```

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=====
0x81cf2000: c4_led_status      000000ff      0x81cf2004:
c4_led_ctl      00000001

```

```
FPL registers
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=====
0x81cf0200: fpl_port_config      232980f0
0x81cf020c: fpl_port_id_ctl      00000000      0x81cf0210:
fpl_port_id_addr      00012400
0x81cf0214: fpl_port_speed      00000003      0x81cf021c:
fpl_lli_ctl      000000c0
0x81cf0228: fpl_lli_os_ctl      bc55bf45      0x81cf022c:
fpl_lli_send_word      bc95b5b5
0x81cf0230: fpl_lli_mark_rx      005fbf45      0x81cf0234:
fpl_lli_rnd_trip_time      00000000
0x81cf0238: fpl_lli_ns_status      02144005      0x81cf023c:
fpl_lli_intr_status      02000000
0x81cf0244: fpl_lli_def      00144005      0x81cf0254:
fpl_lli_intr_enable_clr      305e4007
0x81cf0258: fpl_err_intr_status      00000100      0x81cf0260:
fpl_err_intr_enable_clr      00000000
0x81cf0268: fpl_err_first_error      00000000      0x81cf026c:
fpl_speed_neg_ctl      a404d3b8
0x81cf0270: fpl_speed_neg_stat      0000005c      0x81cf0274:
fpl_softasn_ctl      0000000f
0x81cf0278: fpl_link_init_ctl      00042d48      0x81cf027c:
fpl_link_init_stat      000000e0
0x81cf0280: fpl_aec_ctl      00181060      0x81cf0284:
fpl_aec_ctl2      04009f60
0x81cf0288: fpl_pcs_ctl      00000076      0x81cf028c:

```

```

fpl_fec_ctl          0000063e
0x81cf0290: fpl_fec_cor          00000000    0x81cf0294:
fpl_fec_uncor       00000000
0x81cf0298: fpl_hss_link_ctl        0031f040    0x81cf029c:
fpl_afifo_link_ctl  00000a86
0x81cf02a0: fpl_echo_lb_ctl            0000028c    0x81cf02a4:
fpl_scratch         00000320
0x81cf02a8: fpl_debug                  00050005    0x81cf02ac:
fpl_misc_debug      00000640
0x00000000: SW_shadow_reg          00040000    0x00000000:
SW_c4_phyp->cfgptr   00030003

```

per-fpg (per octet) registers

=====

```

0x8181b82c: fpg_serdes_ctla0          81a37be7    0x8181b830:
fpg_serdes_ctla1      81a37be7
0x8181b834: fpg_serdes_ctlb0          81a1c3c3    0x8181b838:
fpg_serdes_ctlb1      81a1c3c3
0x8181b83c: fpg_serdes_xgmii_1ms      00067c28    0x8181b840:
fpg_serdes_regtimctl  40e47946
0x8181b844: fpg_serdes_asnrsttimctl  00000102

```

HSS PLL registers

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```

0x8181b400: 00_hssplla_vco_coarse_cal0  00000000    0x8181b404:
01_hssplla_vco_coarse_cal1    00000014
0x8181b408: 02_hssplla_vco_coarse_cal2  00000000    0x8181b40c:
03_hssplla_vco_coarse_cal3    00000000
0x8181b410: 04_hssplla_vco_coarse_cal4  00000000    0x8181b424:
09_hssplla_power_ctl          00000000
0x8181b428: 0A_hssplla_charge_pump_ctl   00000004    0x8181b438:
0E_hssplla_pll_misc_ctl       00000000
0x8181b43c: 0F_hssplla_pclk_ctl         000000f8    0x8181b440:
10_hssplla_eyem_intv_ctl      00000000
0x8181b444: 11_hssplla_eyem_intv_lim1    00000000    0x8181b448:
12_hssplla_eyem_intv_lim2     00000000
0x8181b44c: 13_hssplla_eyem_intv_lim3    00000000    0x8181b450:
14_hssplla_eyem_intv_lim4     00000000
0x8181b4f0: 3C_hssplla_macro_tst_ctl4    00000000    0x8181b4f4:
3D_hssplla_macro_tst_ctl3     00000000
0x8181b4f8: 3E_hssplla_macro_tst_ctl2    00000000    0x8181b4fc:
3F_hssplla_macro_tst_ctl1     00000000
0x8181b500: 00_hssp1lb_vco_coarse_cal0   0000000a    0x8181b504:
01_hssp1lb_vco_coarse_cal1    00000014
0x8181b508: 02_hssp1lb_vco_coarse_cal2   00000000    0x8181b50c:
03_hssp1lb_vco_coarse_cal3    00000000
0x8181b510: 04_hssp1lb_vco_coarse_cal4   00000000    0x8181b524:
09_hssp1lb_power_ctl          00000000
0x8181b528: 0A_hssp1lb_charge_pump_ctl   00000004    0x8181b538:
0E_hssp1lb_pll_misc_ctl       00000000
0x8181b53c: 0F_hssp1lb_pclk_ctl         000000f8    0x8181b540:
10_hssp1lb_eyem_intv_ctl      00000000
0x8181b544: 11_hssp1lb_eyem_intv_lim1    00000000    0x8181b548:
12_hssp1lb_eyem_intv_lim2     00000000

```

| | | |
|--|----------|-------------|
| 0x8181b54c: 13_hsspll_b_eyem_intv_lim3 | 00000000 | 0x8181b550: |
| 14_hsspll_b_eyem_intv_lim4 | 00000000 | |
| 0x8181b5f0: 3C_hsspll_b_macro_tst_ctl4 | 00000000 | 0x8181b5f4: |
| 3D_hsspll_b_macro_tst_ctl3 | 00000000 | |
| 0x8181b5f8: 3E_hsspll_b_macro_tst_ctl2 | 00000000 | 0x8181b5fc: |
| 3F_hsspll_b_macro_tst_ctl1 | 00000000 | |

HSS TX registers

=====

| | | |
|---|----------|-------------|
| 0x8181a400: 00_hsstx_cfg_mode_PHY | 00009d48 | 0x8181a404: |
| 01_hsstx_test_ctl | 00000000 | |
| 0x8181a408: 02_hsstx_coeff_ctl_INV | 00000000 | 0x8181a40c: |
| 03_hsstx_drv_mode_ctl | 00000000 | |
| 0x8181a410: 04_hsstx_drv_ovrd_ctl | 00000010 | 0x8181a414: |
| 05_hsstx_dclk_align_ovrd | 00000080 | |
| 0x8181a418: 06_hsstx_imp_cal_ovrd | 00000c0c | 0x8181a41c: |
| 07_hsstx_dclk_drift_tol | 00000004 | |
| 0x8181a420: 08_hsstx_tap0_coeff_TUNE | 00000000 | 0x8181a424: |
| 09_hsstx_tap1_coeff_TUNE | 00000003 | |
| 0x8181a428: 0A_hsstx_tap2_coeff_TUNE | 00000019 | 0x8181a42c: |
| 0B_hsstx_tap3_coeff_TUNE | 00000003 | |
| 0x8181a434: 0D_hsstx_pol_INV | 00000004 | 0x8181a438: |
| 0E_hsstx_ae_cmd | 00000000 | |
| 0x8181a43c: 0F_hsstx_ae_stat | 00000000 | 0x8181a440: |
| 10_hsstx_ae_tap0_TUNE | 00000000 | |
| 0x8181a444: 11_hsstx_ae_tap1_TUNE | 00000000 | 0x8181a448: |
| 12_hsstx_ae_tap2_TUNE | 00000028 | |
| 0x8181a44c: 13_hsstx_ae_tap3_TUNE | 00000000 | 0x8181a454: |
| 15_hsstx_app_tune | 0000120e | |
| 0x8181a458: 16_hsstx_analog_diag | 00000000 | 0x8181a460: |
| 18_hsstx_4x_seg_app | 0000aaaa | |
| 0x8181a464: 19_hsstx_2x_seg_app | 000000f0 | 0x8181a468: |
| 1A_hsstx_1x_seg_app | 0000f508 | |
| 0x8181a46c: 1B_hsstx_seg_4x_term_app | 00000000 | 0x8181a470: |
| 1C_hsstx_seg_2x1x_term_app | 0000030d | |
| 0x8181a474: 1D_hsstx_tap_sign_app | 00000004 | 0x8181a478: |
| 1E_hsstx_ext_addr_data | 00000001 | |
| 0x8181a47c: 1F_hsstx_ext_addr_addr | 00000000 | 0x8181a480: |
| 20_hsstx_pat_buf_bytes_1_0 | 00000000 | |
| 0x8181a484: 21_hsstx_pat_buf_bytes_3_2 | 00000000 | 0x8181a488: |
| 22_hsstx_pat_buf_bytes_5_4 | 00000000 | |
| 0x8181a48c: 23_hsstx_pat_buf_bytes_7_6 | 00000000 | 0x8181a49c: |
| 27_hsstx_8023az_ctl | 00000000 | |
| 0x8181a4a0: 28_hsstx_dcc_ctl | 000060c0 | 0x8181a4a4: |
| 29_hsstx_dcc_ovrd | 00000000 | |
| 0x8181a4a8: 2A_hsstx_dcc_app | 00000101 | 0x8181a4ac: |
| 2B_hsstx_dcc_timeout | 0000ffff | |
| 0x8181a4c0: 30_hsstx_tap_sign_ovrd | 00000000 | 0x8181a4c8: |
| 32_hsstx_seg_4x_ovrd | 00000000 | |
| 0x8181a4cc: 33_hsstx_seg_2x_ovrd | 00000000 | 0x8181a4d0: |
| 34_hsstx_seg_1x_ovrd | 00000000 | |
| 0x8181a4d8: 36_hsstx_tap_seg_4x_term_ovrd | 00000000 | 0x8181a4dc: |
| 37_hsstx_tap_seg_2x_term_ovrd | 00000000 | |
| 0x8181a4e0: 38_hsstx_tap_seg_1x_term_ovrd | 00000000 | 0x8181a4ec: |

| | | | |
|------------------------------------|----------|----------|-------------|
| 3B_hsstx_mac_test_ctl5 | 00000000 | | |
| 0x8181a4f0: 3C_hsstx_mac_test_ctl4 | 00000000 | 00000000 | 0x8181a4f4: |
| 3D_hsstx_mac_test_ctl3 | 00000000 | | |
| 0x8181a4f8: 3E_hsstx_mac_test_ctl2 | 00000000 | 00000000 | 0x8181a4fc: |
| 3F_hsstx_mac_test_ctl1 | 000000c6 | | |

HSS RX registers

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| | | | |
|---|----------|----------|-------------|
| 0x8181a600: 00_hssrx_cfg_mode_PHY | 00009c78 | 00009c78 | 0x8181a604: |
| 01_hssrx_test_ctl | 00000000 | | |
| 0x8181a608: 02_hssrx_phs_rot_ctl | 0000cb80 | 0000cb80 | 0x8181a60c: |
| 03_hssrx_phs_rot_ofs_ctl | 00000610 | | |
| 0x8181a610: 04_hssrx_phs_rot_posn1 | 00000706 | 00000706 | 0x8181a614: |
| 05_hssrx_phs_rot_posn2 | 00000037 | | |
| 0x8181a618: 06_hssrx_phs_rot_sta_ofs1 | 00000000 | 00000000 | 0x8181a61c: |
| 07_hssrx_phs_rot_sta_ofs2 | 0000001f | | |
| 0x8181a620: 08_hssrx_dfe_ctl_PHY | 00000002 | 00000002 | 0x8181a624: |
| 09_hssrx_dfe_smpl_snap1 | 00000000 | | |
| 0x8181a628: 0A_hssrx_dfe_smpl_snap2 | 00008000 | 00008000 | 0x8181a62c: |
| 0B_hssrx_vga_ctl1 | 000041e4 | | |
| 0x8181a630: 0C_hssrx_vga_ctl2 | 00007a95 | 00007a95 | 0x8181a634: |
| 0D_hssrx_vga_ctl3 | 000009e4 | | |
| 0x8181a638: 0E_hssrx_pwr_mgmt_ctl | 0000001f | 0000001f | 0x8181a63c: |
| 0F_hssrx_iqamp_ctl1 | 0000001c | | |
| 0x8181a640: 10_hssrx_iqamp_ctl2 | 00000005 | 00000005 | 0x8181a644: |
| 11_hssrx_dacap_dacan_sel | 00000003 | | |
| 0x8181a648: 12_hssrx_dacap_dacan | 000034ca | 000034ca | 0x8181a64c: |
| 13_hssrx_daca_min | 00000d26 | | |
| 0x8181a650: 14_hssrx_adac_ctl | 00004546 | 00004546 | 0x8181a654: |
| 15_hssrx_ac_cp_ctl | 000031c3 | | |
| 0x8181a658: 16_hssrx_ac_cp_val | 00008049 | 00008049 | 0x8181a65c: |
| 17_hssrx_dfe_h1h2h3_lcl_off_ch | 00000014 | | |
| 0x8181a660: 18_hssrx_dfe_h1h2h3_lcl_off_val | 00000002 | 00000002 | 0x8181a664: |
| 19_hssrx_peaked_intg | 000000ff | | |
| 0x8181a668: 1A_hssrx_cdr_analog_sw | 0000ce00 | 0000ce00 | 0x8181a66c: |
| 1B_hssrx_peaking_amp_init_c_PHY | 00000000 | | |
| 0x8181a670: 1C_hssrx_dac_dpc | 00000027 | 00000027 | 0x8181a674: |
| 1D_hssrx_ddc | 00004240 | | |
| 0x8181a678: 1E_hssrx_int_stat_PHY | 0000ec9f | 0000ec9f | 0x8181a67c: |
| 1F_hssrx_dfe_func_ctl1_PHY | 0000ffff | | |
| 0x8181a680: 20_hssrx_dfe_func_ctl2_INV | 00007ebf | 00007ebf | 0x8181a684: |
| 21_hssrx_ofs_ch_dcc_qcc_idx | 00002000 | | |
| 0x8181a688: 22_hssrx_dfe_ofs_val | 00007979 | 00007979 | 0x8181a68c: |
| 23_hssrx_h_coeff_bist | 00000401 | | |
| 0x8181a690: 24_hssrx_ac_cap_bist | 00000000 | 00000000 | 0x8181a694: |
| 25_hssrx_max_gain_path_idx_res | 00007829 | | |
| 0x8181a698: 26_hssrx_loff_ctl | 00000044 | 00000044 | 0x8181a69c: |
| 27_hssrx_sigdet_ctl | 000027a0 | | |
| 0x8181a6a0: 28_hssrx_ana_ctl_sw | 00000000 | 00000000 | 0x8181a6a4: |
| 29_hssrx_intg_dac_ofs | 0000a9db | | |
| 0x8181a6a8: 2A_hssrx_eye_ctl | 00004400 | 00004400 | 0x8181a6ac: |
| 2B_hssrx_eye_met | 00000004 | | |
| 0x8181a6b0: 2C_hssrx_eye_met_err_cnt | 00000000 | 00000000 | 0x8181a6b4: |
| 2D_hssrx_eye_met_pdf_eyec | 00000000 | | |

| | | |
|--|----------------|-------------|
| 0x8181a6b8: 2E_hssrx_eye_met_pat_len | 0000007f | 0x8181a6bc: |
| 2F_hssrx_dfe_func_ctl3 | 0000dfff | |
| 0x8181a6c0: 30_hssrx_dfe_tap_ctl_idx_ptr | 00000008 | 0x8181a6c4: |
| 31_hssrx_dfe_tap | 00003021 | |
| 0x8181a6c8: 32_hssrx_lte_ctl_TUNE | 00000600 | 0x8181a6e4: |
| 39_hssrx_int_stat2 | 000041ff | |
| 0x8181a6e8: 3A_hssrx_ac_cpl_cur_src_adj | 00000042 | 0x8181a6ec: |
| 3B_hssrx_dcd_ctl | 00007c46 | |
| 0x8181a6f0: 3C_hssrx_dcc_ctl | 00000d00 | 0x8181a6f4: |
| 3D_hssrx_qcc_ctl | 00006989 | |
| 0x8181a6f8: 3E_hssrx_mac_test_ctl2 | 00000000 | 0x8181a6fc: |
| 3F_hssrx_mac_test_ctl1 | 00000000 | |
| 0x8181a648: 12_hssrx_dacap_dacan[02] | 3bc5 34ca | |
| 0x8181a660: 18_hssrx_dfe_h1h2h3_lcl_off_va[00] | 003f 003f 023f | |
| 0101 3f02 3c01 0000 013e | | |
| 0x8181a660: 18_hssrx_dfe_h1h2h3_lcl_off_va[08] | 3f3f 3e01 3f01 | |
| 3e01 3e3f 3f02 3f03 0001 | | |
| 0x8181a660: 18_hssrx_dfe_h1h2h3_lcl_off_va[16] | 3e3e 3e00 0002 | |
| 0002 0002 | | |
| 0x8181a688: 22_hssrx_dfe_ofs_val[00][00] | 7979 0000 7d7c | |
| 0000 037b 0000 | | |
| 0x8181a688: 22_hssrx_dfe_ofs_val[03][00] | 0308 0000 7e03 | |
| 0000 7f00 0000 | | |
| 0x8181a688: 22_hssrx_dfe_ofs_val[06][00] | 7b09 007f 027b | |
| 7f00 7a7f 0000 | | |
| 0x8181a688: 22_hssrx_dfe_ofs_val[09][00] | 057d 7f00 0a7f | |
| 7f00 7a7e 0000 | | |
| 0x8181a688: 22_hssrx_dfe_ofs_val[12][00] | 0101 0000 7c01 | |
| 0000 7f7d 0000 | | |
| 0x8181a688: 22_hssrx_dfe_ofs_val[15][00] | 047b 0000 787b | |
| 0000 7d07 007f | | |
| 0x8181a688: 22_hssrx_dfe_ofs_val[18][00] | 0104 7f00 000c | |
| 0000 0005 0000 | | |
| 0x8181a688: 22_hssrx_dfe_ofs_val[21][00] | 0005 0000 0005 | |
| 0000 0005 0000 | | |
| 0x8181a688: 22_hssrx_dfe_ofs_val[24][00] | 0204 017f 0502 | |
| 7f7f 7b7d 0000 | | |
| 0x8181a694: 25_hssrx_max_gain_path_idx_res[00] | 0056 084b 1002 | |
| 1892 20cf 2895 307d 38d2 | | |
| 0x8181a694: 25_hssrx_max_gain_path_idx_res[08] | 40af 487f 5072 | |
| 5800 6040 683a 70c6 7829 | | |
| 0x8181a6c4: 31_hssrx_dfe_tap[00] | fffe 8081 4242 | |
| 2121 0011 0023 2223 3022 | | |
| 0x8181a6c4: 31_hssrx_dfe_tap[08] | 3022 3030 2211 | |
| 0c0f | | |
| 0x8181a6e8: 3A_hssrx_ac_cpl_cur_src_adj[00] | 0042 0042 0042 | |
| 0042 | | |
| 0x8181a6ec: 3B_hssrx_dcd_ctl[00] | 7c46 5c00 7c87 | |
| 5c00 7c00 | | |
| 0x8181a6f0: 3C_hssrx_dcc_ctl[00] | 0d00 0d81 0d81 | |
| 0d42 | | |
| 0x8181a6f4: 3D_hssrx_qcc_ctl[00] | 698a 6989 | |

xfipcs, fec, aec, & aet registers

```

=====
0x81cf0400: xfipcs_reg          [00] 00002040 00000004 00000000
00000000 00000001 00000008 00000000 00000000
0x81cf0420: xfipcs_reg          [08] 00008001 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81cf0440: xfipcs_reg          [16] 00000000 00000000 00000000
00000000 00000040 00000000 00000000 00000000
0x81cf0460: xfipcs_reg          [24] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81cf0480: xfipcs_reg          [32] 00001005 00008000 00000000
00000000 00000000 00000000 00000000 00000000
0x81cf0620: fec_32g_128g_reg       [08] 00000000 00008003 00000000
00000000 00000000 00000000 00000000
0x81cf0648: fec_32g_128g_reg       [18] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81cf0a00: aec_reg                [00] 00000000 00000000 00000000
00000000 00000740 00000000 00000040 000024a2
0x81cf0c00: aet_reg                [00] 000000b0 00007000 000008c4
00000000 00000000

```

bbc registers

```

=====
0x81cf1800: bbc_trc          4    0    2    2    2    2    1
1
0x81cf1840: bbc_trc          2    2    2    2    2    2    2
0
0x81cf1880: bbc_trc          0    0    0    0    0    0    0
0
0x81cf18c0: bbc_trc          0    0    0    0    0    0    0
0
0x81cf1900: bbc_trc          0    0    0    0    0    0    0
0
0x81cf1804: bbc_mbc          0    0    3    3    3    3    0
0
0x81cf1844: bbc_mbc          0    0    3    3    3    3    3
0
0x81cf1884: bbc_mbc          0    0    0    0    0    0    0
0
0x81cf18c4: bbc_mbc          0    0    0    0    0    0    0
0
0x81cf1904: bbc_mbc          0    0    0    0    0    0    0
0
0x81cf1a00: bbc_rcc          0    0    0    0    0    0    0
0
0x81cf1a20: bbc_rcc          0    0    0    0    0    0    0
0
0x81cf1a40: bbc_rcc          0    0    0    0    0    0    0
0
0x81cf1a60: bbc_rcc          0    0    0    0    0    0    0
0
0x81cf1a80: bbc_rcc          0    0    0    0    0    0    0
0
0x81cf1c00: bbc_rqc          0    0    0    0    0    0    0
0

```

| | | | | | | | |
|-------------------------------------|----------|---|---|---|---|----------------------|---|
| 0x81cf1c20: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81cf1c40: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81cf1c60: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81cf1c80: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81cf1d00: bbc_fbpc | 00000000 | | | | | 0x81cf1d04: bbc_csc | |
| 00000006 | | | | | | | |
| 0x81cf1d08: bbc_rcc_inc | 00000000 | | | | | 0x81cf1d0c: | |
| bbc_rqc_inc | 00000000 | | | | | | |
| 0x81cf1d10: bbc_fbpc_inc | 00000000 | | | | | 0x81cf1d14: | |
| bbc_tmc_inc | 00000000 | | | | | | |
| 0x81cf1d18: bbc_threshold | 00000001 | | | | | 0x81cf1d1c: | |
| bbc_counter_clr | 00000000 | | | | | | |
| 0x81cf1d20: bbc_debug_en | 00000000 | | | | | 0x81cf1d24: bbc_ctrl | |
| 00200120 | | | | | | | |
| 0x81cf1d28: bbc_rqc_rcc_thresh | 00000055 | | | | | 0x81cf1d34: | |
| bbc_bb_sc_n | 00000008 | | | | | | |
| 0x81cf1d38: bbc_crd_reco_debug | 00000000 | | | | | 0x81cf1d3c: | |
| bbc_crd_reco_debug_data | 00000000 | | | | | | |
| 0x81cf1d40: bbc_multi_frm_loss_cnt | 00000000 | | | | | 0x81cf1d44: | |
| bbc_multi_rdy_loss_cnt | 00000000 | | | | | | |
| 0x81cf1d48: bbc_1frm_loss_recov_cnt | 00000000 | | | | | 0x81cf1d4c: | |
| bbc_1rdy_loss_recov_cnt | 00000000 | | | | | | |
| 0x81cf1d58: bbc_int_status | 00000000 | | | | | 0x81cf1d5c: | |
| bbc_int_set | 00000000 | | | | | | |
| 0x81cf1d60: bbc_int_first | 00000000 | | | | | 0x81cf1d64: | |
| bbc_frm_rdy_rx_err_addr | 00000000 | | | | | | |
| 0x81cf1d68: bbc_frm_rdy_tx_err_addr | 00000000 | | | | | 0x81cf1d6c: | |
| bbc_trc_mbc_err_addr | 00000000 | | | | | | |
| 0x81cf1d70: bbc_frm_rdy_rx_dbl_ecc | 00000000 | | | | | 0x81cf1d74: | |
| bbc_frm_rdy_tx_dbl_ecc | 00000000 | | | | | | |
| 0x81cf1d78: bbc_trc_mbc_dbl_ecc | 00000000 | | | | | | |
| 0x81cf1d7c: bbc_fsm_status | 00001011 | | | | | 0x81cf1d80: | |
| bbc_force_err | 00000000 | | | | | | |
| 0x81cf1d84: bbc_crdt_avail0 | 00007ffd | | | | | 0x81cf1d88: | |
| bbc_crdt_avail1 | 00000000 | | | | | | |
| 0x81cf1d8c: bbc_scratch | 00000000 | | | | | | |

FPS registers

=====

| | | |
|----------------------------|----------|-------------|
| 0x81cf0004: fps_er_enc_in | 00000000 | 0x81cf0008: |
| fps_er_crc | 00000000 | |
| 0x81cf000c: fps_er_trunc | 00000000 | 0x81cf0010: |
| fps_er_toolong | 00000000 | |
| 0x81cf0014: fps_er_bad_eof | 00000000 | 0x81cf0018: |
| fps_er_enc_out | 00000000 | |
| 0x81cf001c: fps_er_bad_os | 00000000 | 0x81cf0020: |
| fps_er_flush | 00000000 | |
| 0x81cf0024: fps_er_ifg | 00000000 | 0x81cf0038: |
| fps_er_crc_good_eof | 00000000 | |
| 0x81cf003c: fps_inv_arb | 00000000 | 0x81cf0040: |

```

fps_slow_sts_status      00000000
0x81cf0044: fps_tx_frm_cnt      0f99c9f2      0x81cf0048:
fps_rx_frm_cnt          0efc70e2
0x81cf0050: fps_tx_word_cnt_hi  00000018      0x81cf004c:
fps_tx_word_cnt_lo      32eae8bf
0x81cf0058: fps_rx_word_cnt_hi  00000019      0x81cf0054:
fps_rx_word_cnt_lo      2a1bffdff

```

BAL registers

=====

```

0x81cf7000: bal_desired_buf      00000022      0x81cf7004:
bal_alloc_buf          00000022
0x81cf7008: bal_busy_buf        00000002      0x81cf700c:
bal_usable_buf         00000022
0x81cf7010: bal_max_bor_buf         00000000
0x81cf7014: bal_busy_buf_thresh  00000002

```

TXQ registers

=====

```

0x81cf3004: txq_phys_port_ctl      004e0000
0x81cf3050: txq_link_skew          00000000
0x81cf3068: txq_cr_lk_dttm_intr_sts [00] ffff8002 000000ff
0x81cf3070: txq_cr_lk_dttm_intr_en [00] 00007f3d 00000000
0x81cf3024: txq_disc_frm_trap_cnt     00000014

```

FDS registers

=====

```

0x81cf4000: fds_rxf_ctl              00000008      0x81cf4004:
fds_rxf_wait_thresh    00000c06
0x81cf4018: fds_rxf_first_error        00000000      0x81cf401c:
fds_rxf_first_error_info 00000000
0x81cf4020: fds_rxf_inout_pkt_cnt      99be99be
0x81cf4008: fds_rxf_err_int_status     00000000      0x81cf4024:
fds_rxf_fifo_status     00488888
0x81cf5000: fds_txf_ctl              00000008      0x81cf5004:
fds_txf_wait_ifg_thresh 00a00106
0x81cf5008: fds_txf_err_int_status     00000000      0x81cf5024:
fds_txf_fifo_status     00088888
0x81cf502c: fds_txf_bbc_scs         00000018

```

Logical TXQ registers

=====

```

0x81cf3000: txq_log_port_ctl          00000011      0x81cf3008:
txq_port_status        00000000
0x81cf300c: txq_todo_flags            [00] 00000000 00000000
0x81cf3014: txq_spd_match_desc        [00] 00000000 19f519f5 00000000
00000000
0x81cf3024: txq_spd_match_desc        [04] 00000014
0x81cf3028: txq_vc_weight            [00] 25252501 19010125 3c3c3c19
25013c3c
0x81cf3038: txq_vc_weight            [04] 01252525 01010101 01010101
01010101
0x81cf3048: txq_vc_weight            [08] 01010101 00010101
0x81cf3054: txq_cong_dttm_ctrl        00000106

```

```

0x81cf3058: txq_cong_dttm_intr_sts [00] 00000000 00000000
0x81cf3060: txq_cong_dttm_intr_en [00] 00000000 00000000
0x81cf3078: txq_bw_limit_en_reg [00] 00000000 00000000
0x81cf3080: txq_bw_gua_en_reg [00] 00000000 00000000
0x81cf3088: txq_vc_group [00] 03030300 03030303 03030303
03030303
0x81cf3098: txq_vc_group [04] 03030303 03030303 03030303
03030303
0x81cf30a8: txq_vc_group [08] 03030303 03030303 00000000
00000000
0x81cf30b0: txq_bw_thresh_group [00] 00000000 00000000 00000000
00000000
0x81cf30c0: txq_bw_thresh_group [04] 00000000 00000000 00000000
00000000
0x81cf30d0: txq_bw_thresh_group [08] 00000000 00000000 00000000
00000000
0x81cf30e0: txq_bw_thresh_group [12] 00000000 00000000 00000000
00000000
0x81cf30f0: txq_bw_thresh_group [16] 00000000 00000000 00000000
00000000
0x81cf3100: txq_bw_thresh_group [20] 00000000 00000000 00000000
00000000
0x81cf3110: txq_bw_thresh_group [24] 00000000 00000000 00000000
00000000
0x81cf3120: txq_bw_thresh_group [28] 00000000 00000000 00000000
00000000
0x81cf3130: txq_bw_thresh_group [32] 00000000 00000000 00000000
00000000
0x81cf3140: txq_bw_thresh_group [36] 00000000 00000000 00000000
00000000

```

txq Congestion detection Statistics RAM

```

=====
0x810912c0: vc[0] 00000000 0x810912c4: vc[1]
00000000
0x810912c8: vc[2] 0000025e 0x810912cc: vc[3]
000001af
0x810912d0: vc[4] 00000067 0x810912d4: vc[5]
00000030
0x810912d8: vc[6] 00000000 0x810912dc: vc[7]
00000000
0x810912e0: vc[8] 00000000 0x810912e4: vc[9]
00000000
0x810912e8: vc[10] 00000000 0x810912ec: vc[11]
00000000
0x810912f0: vc[12] 00000000 0x810912f4: vc[13]
00000000
0x810912f8: vc[14] 00000000 0x810912fc: vc[15]
00000000
0x81091300: vc[16] 00000000 0x81091304: vc[17]
00000000
0x81091308: vc[18] 00000000 0x8109130c: vc[19]
00000000
0x81091310: vc[20] 00000000 0x81091314: vc[21]

```

```

00000000
0x81091318: vc[22]      00000000      0x8109131c: vc[23]
00000000
0x81091320: vc[24]      00000000      0x81091324: vc[25]
00000000
0x81091328: vc[26]      00000000      0x8109132c: vc[27]
00000000
0x81091330: vc[28]      00000000      0x81091334: vc[29]
00000000
0x81091338: vc[30]      00000000      0x8109133c: vc[31]
00000000
0x81091340: vc[32]      00000000      0x81091344: vc[33]
00000000
0x81091348: vc[34]      00000000      0x8109134c: vc[35]
00000000
0x81091350: vc[36]      00000000      0x81091354: vc[37]
00000000
0x81091358: vc[38]      00000000      0x8109135c: vc[39]
00000000

```

Logical STS registers

=====

```

0x81585704: sts_ftb_type1_miss      00000000
0x81585708: sts_ftb_type2_miss      00000000
0x8158570c: sts_ftb_type6_miss      00000000
0x81585710: sts_hard_zoning_miss    00000000
0x81585714: sts_lun_zoning_miss     00000000
0x8158571c: sts_unroutable              00000000
0x81582734: sts_rte_cl2            00000000      0x81582738:
sts_rte_cl3      0efb6fc5      0x8158273c: sts_rte_link_ctl
000078ab      0x81585728: sts_tx_timeout      00000000

```

Logical STS filter registers

=====

```

0x81585680: stsflt_trig      [00] 00000000 00000000 00000000
00000000
0x81585690: stsflt_trig      [04] 00000000 00000000 00000000
00000000
0x815856a0: stsflt_trig      [08] 00000000 00000000 00000000
00000000
0x815856b0: stsflt_trig      [12] 00000000 00000000 00000000
00000000
0x815856c0: stsflt_trig      [16] 00000000 00000000 00000000
00000000
0x815856d0: stsflt_trig      [20] 00000000 00000000 00000000
00000000
0x815856e0: stsflt_trig      [24] 00000000 00000000 00000000
00000000
0x815856f0: stsflt_trig      [28] 00000000 00000000 00000000
00000000
0x81585700: stsflt_trig      [32]

```

Logical STS discard registers

```

=====
0x81583b98: disc_mcast_wka          00000000    0x81583b9c:
disc_inv_did          00000000
0x81583ba0: disc_cl1_cl4          00000000    0x81583ba4:
disc_sid_chk_fail    00000000
0x81583ba8: disc_inv_dom_egid_txpt 00000000    0x81583bac:
disc_vft_hop_cnt_1   00000000
0x81583bb0: disc_classf          00000000    0x81583bb4:
disc_fcp_cdb_inv     00000000
0x81583bb8: disc_vfid_trap_enabled 00000000    0x81583bbc:
disc_vfid_hdr_chk_fail 00000000
0x81583bc0: disc_shim_cksum_fail  00000000    0x81583bc4:
disc_fed_edit_cmd_err 00000000
0x81583bc8: disc_ftb_vm_mode     00000000    0x81583bcc:
disc_ftb_agnt2_miss  00000000
0x81583bd0: disc_ecb_reserved    00000000    0x81583bd4:
disc_ecb_de_pad_err   00000000
0x81583bd8: disc_ecb_de_tag_err  00000000    0x81583bdc:
disc_ecb_de_seq_err   00000000
0x81583be0: disc_ecb_err         00000000    0x81583be4:
disc_ftb_type4_match  00000000
0x81583be8: disc_fcp_rsp_ftb_type4 00000000    0x81583bec:
disc_ftb_type5_match  00000000
0x81583bf0: disc_ftb_type3_match 00000000    0x81583bf4:
disc_els_ftb_type3    00000000
0x81583bf8: disc_ftb_type1_match 00000000    0x81583bfc:
disc_els_rsp_ex_port  00000000
0x81583c00: disc_inv_drp_dps     00000000    0x81583c04:
disc_did_lookup_miss  00000000
0x81583c08: disc_ftb_type2_match 00000000    0x81583c0c:
disc_trpd_plogi_pdisc 00000000
0x81583c10: disc_type2_lookup_miss 00000000    0x81583c14:
disc_ftb_type6_match  00000000
0x81583c18: disc_els_rep_ex_port 00000000    0x81583c1c:
disc_els_sid_lkup_bit1 00000000
0x81583c20: disc_els_sid_lkup_bit0 00000000    0x81583c24:
disc_bls_frm_trap_bit1 00000000
0x81583c28: disc_ftb_token_err   00000000    0x81583c2c:
disc_asic_internal_err 00000000
0x81583c30: disc_hard_zone_miss  00000000    0x81583c34:
disc_lun_zone_miss    00000000
0x81583c38: discflt_frame_disc   00000000    0x81583c3c:
discflt_parity_err    00000000
0x81583c40: disc_frame_marked_du 00000000    0x81583c44:
disc_frame_marked_to  00000000
0x81583c48: disc_lkup_rte_prty_err 00000000

```

portstatsshow 36

```

stat_wtx          103933411890    4-byte words transmitted
stat_wrx          108080572392    4-byte words received
stat_ftx          261736786      Frames transmitted
stat_frx          251424795      Frames received
stat_c2_frx       0              Class 2 frames received

```

| | | |
|------------------------------|-----------------------------|-------------------------|
| stat_c3_frx | 251359173 | Class 3 frames received |
| stat_lc_rx | 30891 | Link control frames |
| received | | |
| stat_mc_rx | 0 | Multicast frames |
| received | | |
| stat_mc_to | 0 | Multicast timeouts |
| stat_mc_tx | 0 | Multicast frames |
| transmitted | | |
| tim_txcrd_z | 1188 | Time TX Credit Zero |
| (2.5Us ticks) | | |
| tim_txcrd_z_vc 0- 3: | 0 0 | 606 431 |
| tim_txcrd_z_vc 4- 7: | 103 48 | 0 0 |
| tim_txcrd_z_vc 8-11: | 0 0 | 0 0 |
| tim_txcrd_z_vc 12-15: | 0 0 | 0 0 |
| lat_tot_pkt_vc 0- 3: | 1 1 | 1 1 |
| lat_tot_pkt_vc 4- 7: | 1 1 | 1 1 |
| lat_tot_pkt_vc 8-11: | 1 1 | 1 1 |
| lat_tot_pkt_vc 12-15: | 1 1 | 1 1 |
| lat_hi_time_vc 0- 3: | 0 0 | 0 0 |
| lat_hi_time_vc 4- 7: | 0 0 | 0 0 |
| lat_hi_time_vc 8-11: | 0 0 | 0 0 |
| lat_hi_time_vc 12-15: | 0 0 | 0 0 |
| lat_lo_time_vc 0- 3: | 1 1 | 1 1 |
| lat_lo_time_vc 4- 7: | 1 1 | 1 1 |
| lat_lo_time_vc 8-11: | 1 1 | 1 1 |
| lat_lo_time_vc 12-15: | 1 1 | 1 1 |
| max_latency_vc 0- 3: | 1 1 | 1 1 |
| max_latency_vc 4- 7: | 1 1 | 1 1 |
| max_latency_vc 8-11: | 1 1 | 1 1 |
| max_latency_vc 12-15: | 1 1 | 1 1 |
| latency_dma_ts | 09-09-2024 UTC Mon 08:47:24 | TXQ |
| Latency DMA TimeStamp | | |
| fec_cor_detected | 5642 | Count of blocks that |
| were corrected by FEC | | |
| fec_uncor_detected | 0 | Count of blocks that |
| were left uncorrected by FEC | | |
| er_enc_in | 0 | Encoding errors inside |
| of frames | | |
| er_crc | 0 | Frames with CRC errors |
| er_trunc | 0 | Frames shorter than |
| minimum | | |
| er_toolong | 0 | Frames longer than |
| maximum | | |
| er_bad_eof | 0 | Frames with bad end-of- |
| frame | | |
| er_enc_out | 0 | Encoding error outside |
| of frames | | |
| er_bad_os | 0 | Invalid ordered set |
| er_pcs_blk | 0 | PCS block errors |
| er_rx_c3_timeout | 0 | Class 3 receive frames |
| discarded due to timeout | | |
| er_tx_c3_timeout | 0 | Class 3 transmit frames |
| discarded due to timeout | | |
| er_unroutable | 0 | Frames that are |

| | | | |
|-------------------------------|-----------------------------|--|---------------------------------|
| unroutable | | | |
| er_unreachable destination | 0 | | Frame with unreachable |
| er_other_discard | 0 | | Other discards |
| er_type1_miss | 0 | | frames with FTB type 1 |
| er_type2_miss | 0 | | frames with FTB type 2 |
| er_type6_miss | 0 | | frames with FTB type 6 |
| er_zone_miss | 0 | | frames with hard zoning |
| er_lun_zone_miss | 0 | | frames with LUN zoning |
| er_crc_good_eof | 0 | | Crc error with good eof |
| er_inv_arb | 0 | | Invalid ARB |
| er_single_credit_loss on link | 0 | | Single vcrdy/frame loss |
| er_multi_credit_loss on link | 0 | | Multiple vcrdy/frame |
| other_credit_loss credit loss | 0 | | Link timeout/complete |
| phy_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | | Timestamp of |
| phy_port stats clear | | | |
| lgc_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | | Timestamp of |
| lgc_port stats clear | | | |
| fec_corrected_rate second | 2.17e-02 | | FEC Corrected blocks per second |

```
portstats64show 36
stat64_wtx 24 top_int : 4-byte words transmitted
853234326 bottom_int : 4-byte words transmitted
stat64_wrx 25 top_int : 4-byte words received
704402559 bottom_int : 4-byte words received
stat64_ftx 0 top_int : Frames transmitted
261734215 bottom_int : Frames transmitted
stat64_frx 0 top_int : Frames received
251420484 bottom_int : Frames received
stat64_c2_frx 0 top_int : Class 2 frames received
0 bottom_int : Class 2 frames received
stat64_c3_frx 0 top_int : Class 3 frames received
251358401 bottom_int : Class 3 frames received
stat64_lc_rx 0 top_int : Link control frames received
30891 bottom_int : Link control frames
received
stat64_mc_rx 0 top_int : Multicast frames received
0 bottom_int : Multicast frames received
stat64_mc_to 0 top_int : Multicast timeouts
0 bottom_int : Multicast timeouts
stat64_mc_tx 0 top_int : Multicast frames transmitted
0 bottom_int : Multicast frames
transmitted
tim64_rdy_pri 0 top_int : Time R_RDY high priority
0 bottom_int : Time R_RDY high priority
```

| | | |
|---|--------|--|
| tim64_txcrd_z | 0 | top_int : Time BB_credit zero |
| | 1188 | bottom_int : Time BB_credit zero |
| er64_enc_in | 0 | top_int : Encoding errors inside of |
| frames | | |
| | 0 | bottom_int : Encoding errors inside of |
| frames | | |
| er64_crc | 0 | top_int : Frames with CRC errors |
| | 0 | bottom_int : Frames with CRC errors |
| er64_trunc | 0 | top_int : Frames shorter than minimum |
| | 0 | bottom_int : Frames shorter than minimum |
| er64_toolong | 0 | top_int : Frames longer than maximum |
| | 0 | bottom_int : Frames longer than maximum |
| er64_bad_eof | 0 | top_int : Frames with bad end-of-frame |
| | 0 | bottom_int : Frames with bad end-of- |
| frame | | |
| er64_enc_out | 0 | top_int : Encoding error outside of |
| frames | | |
| | 0 | bottom_int : Encoding error outside of |
| frames | | |
| er64_disc_c3 | 0 | top_int : Class 3 frames discarded |
| | 0 | bottom_int : Class 3 frames discarded |
| er64_pcs_blk | 0 | top_int : PCS block errors |
| | 0 | bottom_int : PCS block errors |
| stat64_fec_uncor | 0 | top_int : FEC uncorrected errors |
| detected | | |
| | 0 | bottom_int : FEC uncorrected |
| errors detected | | |
| stat64_rateTxFrame | 1320 | Tx frame rate (fr/sec) |
| stat64_rateRxFrame | 2131 | Rx frame rate (fr/sec) |
| stat64_rateTxPeakFrame | 0 | Tx peak frame rate (fr/sec) |
| stat64_rateRxPeakFrame | 0 | Rx peak frame rate (fr/sec) |
| stat64_rateTxWord | 530439 | Tx Word rate (words/sec) |
| stat64_rateRxWord | 997854 | Rx Word rate (words/sec) |
| stat64_rateTxPeakWord | 0 | Tx peak Word rate (words/sec) |
| stat64_rateRxPeakWord | 0 | Rx peak Word rate (words/sec) |
| stat64_PRJTFrames | 0 | top_int : Number of PRJT frames |
| returned to this port | | |
| | 0 | bottom_int : Number of PRJT |
| frames returned to this port | | |
| stat64_PBSYFrames | 0 | top_int : Number of PBSY frames |
| returned to this port | | |
| | 0 | bottom_int : Number of PBSY |
| frames returned to this port | | |
| stat64_inputBuffersFull | 0 | top_int : Number of occurrences |
| when all input buffers full | | |
| | 0 | bottom_int : Number of |
| occurrences when all input buffers full | | |
| stat64_rxClass1Frames | 0 | top_int : Number of class 1 |
| frames received | | |
| | 0 | bottom_int : Number of class 1 |
| frames received | | |
| stat64_aveTxFrameSize | 401 | Average Tx Frame size |
| stat64_aveRxFrameSize | 468 | Average Rx Frame size |
| Lr_in | 0 | top_int |

```

Ols_in          0          bottom_int
                0          top_int
                0          bottom_int
Lr_out          0          top_int
                0          bottom_int
Ols_out         0          top_int
                0          bottom_int
Link_failure    0          top_int
                0          bottom_int
Invalid_CRC     0          top_int
                0          bottom_int
Invalid_word    0          top_int
                0          bottom_int
Protocol_err    0          top_int
                0          bottom_int
Loss_of_sig     0          top_int
                0          bottom_int
Loss_of_sync    0          top_int
                0          bottom_int
er_bad_os       0          top_int : Invalid ordered set
                0          bottom_int: Invalid ordered set

```

```

portrouteshow 36
port address ID: 0x012400
external unicast routing table:
  0: Embedded
 255: Embedded
internal unicast routing table:

```

```

portcamshow 36
-----
Port  SID used  DID used  SID entries  DID entries
36    0         0        000000     000000
-----

```

```

ptbufshow, ptcreditshow, ptdatashow, ptstatsshow 36
S:
S:VF Enable:          1
S:
S:C4 Global Variable:
S:-----
-----
S:trace_stop:        0
S:
S:C4 Phy Data Pointers: c4_phyp = 0xb6af4100
S:-----
-----
S:tnodep              0xbb84dd20      pt
      0x4302801e
S:proto_phyp          0xb880c000      phy_cfg
0xb6af5140
S:c4_chp              0x97e28000      c4_lgcp
0x97fc0000

```

```

S:c4_phy_regp          0x81cf0000      proc_dir
0xb851f0a0
S:-----
-----
S:magic_id             0xc4345678      num_port_timer      12
S:prev_if_id          0x4302001e      S:ftx
261736786            tov              0
S:initialized          1                port_idx             30
S:ui_idx               36              slot_no
0
S:blade_idx           30
S:unused               0                sw_usr_ports         400
0                                                              intr_debounced
S:aec_status           0x0              reason_code
0
S:debug                0x00000004      debug_trc_line       0
S:rxbuf_list_head     0xffffffff      rxbuf_list_tail
0x30c7
S:isAePort             0                port_misc_data
0
S:num_fault1_rx_disc   0                num_fault2_rx_disc   0
S:p_lll_cause0         1                p_sig_regained       0
S:p_sync_regained      1                enc_out
0x0
S:cached_fps_status    0                cached_sts_status    0
S:cached_er_crc_good_eof 0
S:cached_er_bad_os     0                cached_er_too_long    0
S:cached_er_trunc      0
cached_tot_er_crc_good_eof 0
S:num_pt_excess_intr   0                num_no_fid            0
S:num_fault1_cnt       0                num_fault2_cnt
0
S:num_fault_lip        0                num_fault_lll         0
S:num_fault_rx_fifo    0                num_fault_hss         0
S:num_fault_bwait      0                lli_intr_prim
0
S:num_sw_link_to       0
be_link_err_mon_count 0
S:ecb_enc_enabled      0                ecb_comp_enabled
0
S:ecb_rsv_enc          0                ecb_rsv_comp         0
S:ecb_enc_bm           0x0              ecb_key_index
0xffffffff
S:fab_idx              0
S:num_be_lto           0                lto_count_reset_intvl
0
S:lr_count_reset_intvl 0                num_be_lr
0
S:num_fault_qsfp       0                check_lto
0
S:credit_loaded        0                num_credit_overrun
0
S:fec_enabled          0x1              fec_los_to_flag      0x1
S:phy_stats_clear_ts   1725611419      pcs_err_online

```

```

0
S:pcs_err_light_det          0          pcs_err_ignore
0
S:pcs_blk_err                0          pcs_hiber          0
S:phy_port_status           2          ecb_enc_lr_count

S:dport_mode                0          avoid_lto_det      0
S:sn_debounced              0x0      sn_started_kr_reqd  1
S:major_timer_started       0x0      ready_bm           0x0
S:parln_1_bm                0x0      parln_0_bm         0x0
S:be_los_of_sync_event_intvl 0
be_los_of_sync_event        0
S:errataPtenable_cntr       0          errataPoll_cntr

S:jda_rx_sig_loss_det       0          jda_rx_sig_loss_cnt
0

S:encrypt_blk_error         0
S:
S:      c4_trunk
S:=====
S:mark_ts                    0x0      deskew             0x0
S:master_phyp                0x0
S:
S:adelay[00]: 0x00000000 0x00000000 0x00000000 0x00000000
S:adelay[04]: 0x00000000 0x00000000 0x00000000 0x00000000
S:
S:      c4_buf
S:=====
S:tx_csc                      6          rx_csc
6
S:ld_vc_credits              0          tx_flag
0x100
S:alloc_buffers              34          req_buffers        34
S:est_buffers                20          ld_use_est         0
S:bb_sc_n                    8          rx_bb_sc_n
8
S:data_cr                    5          nondata_cr
6
S:cr_enable                  0
S:ld_nondata_cr              6          tnodep
0xbb84de00
S:tx_credits[0] 4  0  2  2  2  2  1  1
S:tx_credits[8] 2  2  2  2  2  2  2  0
S:tx_credits[16]  0  0  0  0  0  0  0  0  0  0
S:tx_credits[24]  0  0  0  0  0  0  0  0  0  0
S:tx_credits[32]  0  0  0  0  0  0  0  0  0  0
S:rx_credits[0] 4  0  2  2  2  2  1  1
S:rx_credits[8] 2  2  2  2  2  2  2  0
S:rx_credits[16]  0  0  0  0  0  0  0  0  0  0
S:rx_credits[24]  0  0  0  0  0  0  0  0  0  0
S:rx_credits[32]  0  0  0  0  0  0  0  0  0  0
S:tx_mbc[0]  0  0  3  3  3  3  0  0
S:tx_mbc[8]  0  0  3  3  3  3  3  0
S:tx_mbc[16]  0  0  0  0  0  0  0  0

```

```

S:tx_mbc[24]    0    0    0    0    0    0    0    0
S:tx_mbc[32]    0    0    0    0    0    0    0    0
S:rx_mbc[0]     0    0    3    3    3    3    0    0
S:rx_mbc[8]     0    0    3    3    3    3    3    0
S:rx_mbc[16]    0    0    0    0    0    0    0    0
S:rx_mbc[24]    0    0    0    0    0    0    0    0
S:rx_mbc[32]    0    0    0    0    0    0    0    0

```

S:

S:C4 Chip Variables: c4_phyp->c4_chp = 0x97e28000

S:-----

S:version = 2.1

S:magic_id 0xc4234567 init_state 0x8

S:reset_reg_mem 0x1

S:ch_int0_en_bm 0x0 intr0_cause 0x0

S:ch_int1_en_bm 0x0 intr1_cause 0x0

S:ch_int2_en_bm 0x0 intr2_cause 0x0

S:ch 0x43010080 ch_cfg

0xb7013ba0

S:raslog_hndl.hndl 0x0 obj_halted 0x0

S:c4_chip_regp 0x80000000 c4_fpg_regp

0x81800000

S:num_chip_timer 0x5

S:hi_task_bm 0x0 lo_task_bm 0x0

S:c4_deferq.q_head 0x0 c4_deferq.q_tail 0x0

S:c4_tmrq.q_head 0x0 c4_tmrq.q_tail 0x0

slot_no 0

S:chip_inst 0 chip_idx 0

S:pll_initialized 1

pll_serdes_initialized 1

S:init_tries 0 init_ptEnableBM

0xba01b488

S:tick_polling 0xb980c9c0 sec_polling

0xb980c960

S:bb_fid 129

S:ecb_key_bm[0] 0x0 ecb_key_bm[1] 0x0

S:ecb_key_bm[2] 0x0 ecb_key_bm[3] 0x0

S:is_chip_enc_enabled 0

is_chip_comp_enabled 0x0

S:ftb_rsrcp->ftb_flags 0x0 act_rsrcp->act_flag 0x1

S:lue_rsrcp->lue_flags[0] 0x0 lue_rsrcp-

>lue_flags[1] 0x0

S:c4_phyp[00]: 0xb6ab0000 0xb6ab2080 0xb6ab4100 0xb6ab6180

S:c4_phyp[04]: 0xb6ab9040 0xb6abb0c0 0xb6abd140 0xb6ac0000

S:c4_phyp[08]: 0xb6ac2080 0xb6ac4100 0xb6ac6180 0xb6ac9040

S:c4_phyp[12]: 0xb6acb0c0 0xb6acd140 0xb6ad0000 0xb6ad2080

S:c4_phyp[16]: 0xb6ad4100 0xb6ad6180 0xb6ad9040 0xb6adb0c0

S:c4_phyp[20]: 0xb6add140 0xb6ae0000 0xb6ae2080 0xb6ae4100

S:c4_phyp[24]: 0xb6ae6180 0xb6ae9040 0xb6aeb0c0 0xb6aed140

S:c4_phyp[28]: 0xb6af0000 0xb6af2080 0xb6af4100 0xb6af6180

S:c4_phyp[32]: 0xb6af9040 0xb6afb0c0 0xb6afd140 0xb6b00000

S:c4_phyp[36]: 0xb6b02080 0xb6b04100 0xb6b06180 0xb6b09040

S:c4_phyp[40]: 0xb6b0b0c0 0xb6b0d140 0xb6b10000 0xb6b12080

S:c4_phyp[44]: 0xb6b14100 0xb6b16180 0xb6b19040 0xb6b1b0c0

```

S:c4_phyp[48]: 0xb6b1d140 0xb6b20000 0xb6b22080 0xb6b24100
S:c4_phyp[52]: 0xb6b26180 0xb6b29040 0xb6b2b0c0 0xb6b2d140
S:c4_phyp[56]: 0xb6b30000 0xb6b32080 0xb6b34100 0xb6b36180
S:c4_phyp[60]: 0xb6b39040 0xb6b3b0c0 0xb6b3d140 0xb6b40000
S:c4_lgcp[00]: 0x97f48000 0x97f4c000 0x97f50000 0x97f54000
S:c4_lgcp[04]: 0x97f58000 0x97f5c000 0x97f60000 0x97f64000
S:c4_lgcp[08]: 0x97f68000 0x97f6c000 0x97f70000 0x97f74000
S:c4_lgcp[12]: 0x97f78000 0x97f7c000 0x97f80000 0x97f84000
S:c4_lgcp[16]: 0x97f88000 0x97f8c000 0x97f90000 0x97f94000
S:c4_lgcp[20]: 0x97f98000 0x97f9c000 0x97fa0000 0x97fa4000
S:c4_lgcp[24]: 0x97fa8000 0x97fac000 0x97fb0000 0x97fb4000
S:c4_lgcp[28]: 0x97fb8000 0x97fbc000 0x97fc0000 0x97fc4000
S:c4_lgcp[32]: 0x97fc8000 0x97fcc000 0x97fd0000 0x97fd4000
S:c4_lgcp[36]: 0x97fd8000 0x97fdc000 0x97fe0000 0x97fe4000
S:c4_lgcp[40]: 0x97fe8000 0x97fec000 0x97ff0000 0x97ff4000
S:c4_lgcp[44]: 0x97ff8000 0x97ffc000 0x8e000000 0x8e004000
S:c4_lgcp[48]: 0x8e008000 0x8e00c000 0x8e010000 0x8e014000
S:c4_lgcp[52]: 0x8e018000 0x8e01c000 0x8e020000 0x8e024000
S:c4_lgcp[56]: 0x8e028000 0x8e02c000 0x8e030000 0x8e034000
S:c4_lgcp[60]: 0x8e038000 0x8e03c000 0x8e040000 0x8e044000
S:chip_timers[00]: 0xb980c720 0xb980c780 0xb980c7e0 0xb980c840
S:chip_timers[04]: 0xb980c8a0 0xb980c900
S:disc_trap_enable_required      0x0          rxlp_disc_log_stop
          0x0
S:curr_rxlp_frm_cnt      0x0          curr_rxlp_disc_frm_cnt  0x0
S:sw_disc_frm_cnt      0x0          last_disc_frm_cnt      0x0
S:txq_nopop_pr_cnt      0x0          pollErrataDfe_ptBM
0xba01b4b0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][0]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][1] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][2]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][0] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][1]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][2] 0x0
S:
S:C4 Logical Port Variables
S:-----
-----
S:c4_lgc_regp      0x81cf0000
S:c4_phyp:
S:      0xb6af4100      0x0          0x0          0x0

S:      0x0          0x0          0x0          0x0

S:master_phyp      0xb6af4100      if_id
0x4302001e
S:min_phyp      0x0          max_phyp      0x0
S:num_phy_ports      1          lgc_num      30
S:num_iu_to      0          sw_txq_bm
0
S:port_fid      128          unused      0
S:port_group      3          lgc_stats_clear_ts
1725611419
S:domain_tbl_sel      94          area_tbl_sel

```

```

    30
S:egid_tbl_sel          2
S:serv_lo_bm           0x0
S:
S:Proto Phy Variables:
S:-----
-----
S:magic_id             0xc4123456      asic_phyp
0xb6af4100
S:port_id              0x4302801e      phy_cfg
0xb6af5140
S:upsm_hdl             0xb8019aa0      physm_hdl
0xb8019820
S:ov_snsn_hdl         0xb80196e0      sw_snsn_hdl
0xb8019780
S:ov_lksm_hdl         0xb80198c0      sw_lksm_hdl
0xb8019960
S:trksm_hdl           0xb8019a00      lr_flag          0x0
S:lr_active           0x0                qsfp_txrx_rate_sel
0x0
S:
S:UPSM                UP24: UPST_E_PORT          --> UP26: UPST_TRUE_E_PORT
S:SNSM(OV)            SN02: OV_SNST_HW_NEG      --> SN04: OV_SNST_NEGOTIATED
S:SNSM(SW)            SW00: SW_SNST_STAGE_WS   --> SW00: SW_SNST_STAGE_WS
S:PHYSM               PP04: PHYST_NO_SYNC      --> PP05: PHYST_IN_SYNC
S:LKSM(OV)            LK06: OV_LKST_HW_RESET  --> LK04: OV_LKST_ACTIVE
S:LKSM(SW)            SW13: INACTIVE          --> SW13: INACTIVE
S:TRKSM               TRK0: TRKST_INIT        --> TRK0: TRKST_INIT
S:
S:physm variables:
S:-----
-----
S:proto_phyp          0xb880c000      physm_hdl
0xb8019820
S:force_offline       0                copper              0
S:fault_reason        0: UNKNOWN
S:phy_media_present   1
S:
S:snsn variables:
S:-----
-----
S:speed               0x8                proto_phyp
0xb880c000
S:hw_sn_tries_left    0x64              sw_sn_tries_left    0x0
S:curr_txsp_count     0x0
S:tx_max              0x0                curr_tx_idx
0x0
S:curr_tx             0x0                curr_rxsp_count
0x0
S:rx_max              0x0                curr_rx_idx
0x0
S:curr_rx             0x0                rx_mem
0x0
S:rxsp_rec_count      0x0

```



```

S:nc_start          0x0          tx_start          0x0
S:sync_start       0x0          sync_present     0x0
S:diag_auto        0x0          diag_speed       0xff
S:striped_wd_tov   3000          hw_wd_tov
      3000
S:step             0x0          qsfp28_speed_mode
      0x0
S:qsfp_mode0_hw_sn_tries_left  0x0
S:qsfp_mode1_hw_sn_tries_left  0x0
S:
S:lksm variables:
S:-----
-----
S:proto_phyph      0xb880c000    ov_lksm_hdl
0xb80198c0
sw_lksm_hdl        0xb8019960
num_lf1            0
S:hw_link_tries_left  9          sw_link_tries_left  5
S:buf_ptype        0x3          stored_entry_state  0x1
S:handshake_owner  0x0          0x1          mark_unsent
      0x0
S:busybuf_stuck    0x0          lr_wait          0x0
S:
S:trksm variables:
S:-----
-----
S:Not a trunk port
S:
S:upsm variables:
S:-----
-----
S:proto_phyph      0xb880c000    upsm_hdl
0xb8019aa0
S:bb_credits        0          port_beacon        0
S:port_diag_flag    0          force_offline
      0
S:port_fault_rsn    0: PORT_NO_FAULT
S:retry_init_rsn    0: UNKNOWN
S:linit_reason      0          linit_result        0
S:ie_fctl_mode      4          fec_in_sync_tries_left  4
S:retry_sn_fail_init  0
retry_link_fail_init  0
S:excess_lr_count   0
S:
S:c4_ch_cfg
S:-----
-----
S:c4_desc_ring_size 256          292          256          256          292
292          2          292          292
S:thresh_def        0          16          1          0
S:intr_tries        500          cmem_pattern
0xdeadbeef
S:cmem_pattern_upwd  2          cmem_init_time      16
S:cmem_init_tries   5

```

```

S:ctrl_par_thresh      2      data_par_thresh
   4
S:cam_par_thresh      4      buf_loss_thresh
   12
S:crit_par_thresh     2      non_crit_par_thresh
   6
S:pci_abort_thresh    10     pci_err_thresh      5
S:excess_chintr_thresh 8     sw_err_thresh       20
S:err_sample_period   300   intr_sleep
20000
S:frame_timeout      2500   proxy_dev           16384
S:vf_route           81920   qos                 2048
S:stats              2048   f_redirect          2048
S:rsp_trap           2048   lun_zoning          20480
S:area_mode          0     ftb_max_loop[0]    0
S:ftb_max_loop[1]    6     ftb_max_loop[2]    9
S:ftb_max_loop[3]    10    ftb_max_loop[4]    10
S:ftb_max_loop[5]    5     ftb_max_loop[6]    6
S:ftb_seg_size[0]    0     ftb_seg_size[1]
16384
S:ftb_seg_size[2]    65536  ftb_seg_size[3]
16384
S:ftb_seg_size[4]    16384  ftb_seg_size[5]
65536
S:ftb_seg_size[6]    16384  ftb_seg_base[0]    0
S:ftb_seg_base[1]    0     ftb_seg_base[2]
65536
S:ftb_seg_base[3]    16384  ftb_seg_base[4]
32768
S:ftb_seg_base[5]    131072 ftb_seg_base[6]
49152
asic_err_monitor_period1 300
asic_err_monitor_period2 86400
zone_chk_to_poll_period 25
zone_chk_class2_reject_tov 220
S:
S:c4_phy_cfg
S:-----
-----

```

```

S:version = 2.1
S:pt      0x4302801e   fab_ptr
0x9a800000
S:fabattr      0x9a8000d4   fab_iop
   0x9a800050
S:cfgbm      0xbb84db64   port_ctrl
0xb6af5158
S:pcap.pcap_bm 0x8d215547   pcap.pcap2_bm
0x588289
S:pcap.pcap3_bm 0x1bebe0c
ui_idx      36     S:slot_no
   0
is_icl      0     S:sw_usr_ports     400
S:neg_speed   10 8 5 0 0 0
S:my_domain   0x1   port_mode          0x0

```

```

S:hw_sn_maxtries          100          sw_sn_maxtries
    0
S:hw_link_maxtries        10          sw_link_maxtries          5
S:rx_cyc_tov              28          rttov                    300
S:bufrdy_tov              300        busybuf_tov              286
S:mark_tov                300        lksm_tov                 3000
S:buf_dealloc_wait        4          hw_wd_tov               3000
S:hw_lk_train_tov         540        hw_lk_test_tov
    150
S:syswait_tx_12_lips      1          lip_rx_tov              55
S:al_time_tov             15        lp_tov                   2000
S:intr_tries_port         500        intr_mod_debounce
    250
S:intr_lsrflt_debounce    500        intr_efifo_debounce     100
S:port_no_fid             3          excess_ptintr_thresh    8
S:port_fault1_thresh      100        port_fault1_spur_thresh 250
S:port_fault1_disc_thresh 500
port_fault1_disc_spur_thresh 1000
S:port_fault2_thresh      5          losync_tov              100
S:port_sw_link_to         15        en_8g_scramble
    1
frc_hw_sn_mode            0x1
S:enc_poll_thresh         0          fec_enable
    0
S:fec_in_sync_to          50        fec_in_sync_try_max
    4
S:port_be_lto_threshold   100        port_be_lr_threshold
    2
S:be_cr_in_sync_to        5
port_credit_overrun_thresh 10
S:jda_sfp_losig_tov       400
jda_sfp_losig_try_max     30
S:striped_wd_tov          3000
no_sync_debounce          1200
S:
S:    fab_iop
S:=====
S:fab_iop->interop_mode 0x0          fab_iop->lab_mode          0x0
S:fab_iop->fl_bbc         0x0          fab_iop->fl_fan
    0x0
S:fab_iop->fl_cls         0x4          fab_iop->fl_rscn
    0x0
S:fab_iop->domain_id_offset 0x60        fab_iop-
>mcmt_fabric_mode        0x0
S:fab_iop->mcmt_default_zone 0x0          fab_iop-
>mcmt_safe_zone          0x0
S:
S:    port_ctrl
S:=====
S:port_ctrl.port_type     1          port_ctrl.port_grp       3
S:port_ctrl.port_number  36          port_ctrl.vc_mode        1
S:
S:    port_ctrl.lcap
S:=====

```

```

S:has_serdes          0          has_media          1
S:topology            1          skip_nego          0
S:skip_pnego         0          skip_init_event   0
S:en_shim             0          speed_neg
  1
S:loop_back           0          num_speeds        5
S:fec_enable          0
S:
S:      port_ctrl.speed_list array
S:=====
S:speed_list[0].auto_neg  1      speed_list[0].lnk_speed  0x0000000a
S:speed_list[1].auto_neg  1      speed_list[1].lnk_speed  0x00000008
S:speed_list[2].auto_neg  0      speed_list[2].lnk_speed  0x00000006
S:speed_list[3].auto_neg  1      speed_list[3].lnk_speed  0x00000005
S:speed_list[4].auto_neg  0      speed_list[4].lnk_speed  0x00000003
S:speed_list[5].auto_neg  0      speed_list[5].lnk_speed  0x00000000
S:
S:      port_ctrl.cm
S:=====
S:port_ctrl.cm.num_vcs      8
S:port_ctrl.cm.min_bufs     8
S:port_ctrl.cm.cr_shar_bufs 0
S:port_ctrl.vc_alloc
S:port_ctrl.vc_alloc      2 0 1 1 1 1 1 1
S:port_ctrl.vc_alloc      0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.norm_vc_alloc
S:port_ctrl.norm_vc_alloc  4 0 5 5 5 5 1 1
S:port_ctrl.norm_vc_alloc  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.cm.skip_bb_credit 0
S:port_ctrl.cm.use_shim_based_sublist 0
S:
S:      port_ctrl.serdes_set
S:=====
S:serdes_type              0x8
S:serdes_data_t.ibm_hss_serdes.tx_drive_power 0x1
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b_sign 0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b 0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_a 0x0
S:serdes_data_t.ibm_hss_serdes.rxeq 0x0
S:
S:      cfgbm
S:=====
S:old_distance             0x0          gport_lockdown     0x0
S:tpport                   0x1          speed               0x0
S:disable_eport            0x0          fcacc               0x0
S:lport_lockdown           0x0          priv_lport_lockdown
  0x0
S:vcxlt_linit              0x0          delay_flogi        0x0
S:isl_interop               0x0          distance            0x0
S:BufStarvFlag              0x0          credit_sharing     0x0
S:lport_halfduplex          0x0          lport_fairness     0x0
S:soft_neg                  0x0          asn_frc_hwretry   0x0

```

```

S:cr_recov          0x0          fport_buffers      0x0
S:export           0x0          export_mode
    0x0
S:csctl_en         0x0          mirror_port        0x0
S:fault_delay      0x0          non_dfe            0x0
S:fec_configured*(0=ENAB)  0          fec_tts
    0
S:port_persistently_disabled (permanently) 0 (0)
S:
S:      cfg property
S:=====
S:priv_pcfg_bm      0x00000000      lgcl_pcfg_bm
0xbb84dba4
S:fport_buffer      0x00000000
S:
S:
S:C4 Discard Cntrs: rxlp_stats = 0xb6af44b0
S:-----
-----
S:disc_mcast_wka    0x0          disc_inv_did       0x0
S:disc_cl1_cl4      0x0          disc_sid_chk_fail  0x0
S:disc_inv_dom_egid_txpt  0x1d      disc_vft_hop_cnt_1
    0x0
S:disc_classf       0x0          disc_fcp_cdb_inv   0x0
S:disc_vfid_trap_enabled  0x0
disc_vfid_hdr_chk_fail 0x0
S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err 0x0
S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err 0x0
S:disc_ftb_vm_mode  0x0          disc_ftb_agnt2_miss  0x0
S:disc_ecb_de_pad_err 0x0          disc_ecb_de_tag_err   0x0
S:disc_ecb_de_seq_err 0x0          disc_ecb_err          0x0
S:disc_ftb_type4_match 0x0          disc_fcp_rsp_ftb_type4 0x0
S:disc_fcp_rsp_ftb_type4 0x0          disc_ftb_type5_match
    0x0
S:disc_ftb_type3_match 0x0          disc_els_ftb_type3   0x0
S:disc_ftb_type1_match 0x0          disc_els_rsp_ex_port  0x0
S:disc_inv_drp_dps   0x0          disc_did_lookup_miss  0x0
S:disc_ftb_type2_match 0x0          disc_trpd_plogi_pdisc 0x0
S:disc_type2_lookup_miss 0x0          disc_ftb_type6_match
    0x0
S:disc_els_rep_ex_port 0x0          disc_els_sid_lkup_bit1 0x0
S:disc_els_sid_lkup_bit0 0x0
disc_bls_frm_trap_bit1 0x0
S:disc_ftb_token_err 0x0          disc_asic_internal_err 0x0
S:disc_hard_zone_miss 0x0          disc_lun_zone_miss    0x0
S:discflt_frame_disc 0x0          discflt_parity_err    0x0
S:disc_frame_marked_du 0x1          disc_frame_marked_to  0x0
E:Connection type: FE
E:Port type: E_port
E:Trunk port: No
E:Configured Speed: AUTO_SPEED_NEGO
E:Max Capable Speed: 32G
E:Current SNSM Speed: 16G
E:Hardware TX Speed: 16G (0x00000003)

```

E:Hardware RX Speed: 32G (0x00000040)

E:

| | | | |
|-------------------|-------|------------------|-------|
| E:Interrupts: | 0 | Link_failure: | 0 |
| Loss_of_sync: | 0 | Loss_of_sig: | 0 |
| E:Lli: | 0 | Invalid_word: | 0 |
| E:trapped_frm: | 65821 | fwd_status_ok: | 65821 |
| E:fwd_timeout: | 0 | fwd_tx_unavail: | 0 |
| E:fwd_unroutable: | 0 | fwd_zone_out: | 0 |
| E:fwd_other_err: | 0 | frm_err_discard: | 0 |
| E:Fltr listA: | 0 | Fltr listB: | 0 |
| E:Zone trap fwd: | 0 | Zone trap disc: | 0 |
| E:shim_csum: | 0 | RTE_perr: | 0 |
| E:Invalid_crc: | 0 | Delim_err: | 0 |
| E:Protocol_err: | 0 | | |
| E:Lr_in: | 0 | Lr_out: | 0 |
| E:Ols_in: | 0 | Ols_out: | 0 |

filterportshow 36

FILTER DATA

Shadow settings:

Filter Enable: 0x00000420
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000

Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass: 0x00000000
Real settings:
Enable RAM: 0x00000420, 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass RAM: 0x00000000

Shadowed filters:

Filter 0: Not Installed (MIRROR1)(LISTA)
c4_fldenable[0] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[0] = 0x00000000, c4_fltr_config[0] = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
c4_fldenable[1] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[1] = 0x00000000, c4_fltr_config[1] = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
c4_fldenable[2] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[2] = 0x00000000, c4_fltr_config[2] = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)

```
    c4_fldenable[3] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[3] = 0x00000000,c4_fltr_config[3] = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
    c4_fldenable[4] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[4] = 0x00000000,c4_fltr_config[4] = 0x00000000
Filter 5: Installed (ZONING TRAP)(LISTA)
    c4_fldenable[5] = 0x00000000 0x00000000 0x00000000
0x06007410
    c4_fldnegate[5] = 0xfd9ffffff,c4_fltr_config[5] = 0x000001c0
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
    c4_fldenable[6] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[6] = 0x00000000,c4_fltr_config[6] = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
    c4_fldenable[7] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[7] = 0x00000000,c4_fltr_config[7] = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
    c4_fldenable[8] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[8] = 0x00000000,c4_fltr_config[8] = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
    c4_fldenable[9] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[9] = 0x00000000,c4_fltr_config[9] = 0x00000000
Filter 10: Installed (WELL KNOWN ADDR)(FORWARD)
    c4_fldenable[10] = 0x00000001 0x00000000 0x00000000
0x00000000
    c4_fldnegate[10] = 0xffffffff,c4_fltr_config[10] =
0x00000054
Filter 11: Not Installed (SIM)(LISTA)
    c4_fldenable[11] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[11] = 0x00000000,c4_fltr_config[11] =
0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
    c4_fldenable[12] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[12] = 0x00000000,c4_fltr_config[12] =
0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
    c4_fldenable[13] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[13] = 0x00000000,c4_fltr_config[13] =
0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
    c4_fldenable[14] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[14] = 0x00000000,c4_fltr_config[14] =
0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
    c4_fldenable[15] = 0x00000000 0x00000000 0x00000000
```



```
0x00000000
    c4_fldnegate[15] = 0x00000000,c4_fltr_config[15] =
0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
    c4_fldenable[16] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[16] = 0x00000000,c4_fltr_config[16] =
0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
    c4_fldenable[17] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[17] = 0x00000000,c4_fltr_config[17] =
0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
    c4_fldenable[18] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[18] = 0x00000000,c4_fltr_config[18] =
0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
    c4_fldenable[19] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[19] = 0x00000000,c4_fltr_config[19] =
0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
    c4_fldenable[20] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[20] = 0x00000000,c4_fltr_config[20] =
0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
    c4_fldenable[21] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[21] = 0x00000000,c4_fltr_config[21] =
0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
    c4_fldenable[22] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[22] = 0x00000000,c4_fltr_config[22] =
0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
    c4_fldenable[23] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[23] = 0x00000000,c4_fltr_config[23] =
0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
    c4_fldenable[24] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[24] = 0x00000000,c4_fltr_config[24] =
0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
    c4_fldenable[25] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[25] = 0x00000000,c4_fltr_config[25] =
0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
```

```
    c4_fldenable[26] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[26] = 0x00000000,c4_fltr_config[26] =
0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
    c4_fldenable[27] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[27] = 0x00000000,c4_fltr_config[27] =
0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
    c4_fldenable[28] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[28] = 0x00000000,c4_fltr_config[28] =
0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
    c4_fldenable[29] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[29] = 0x00000000,c4_fltr_config[29] =
0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    c4_fldenable[30] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[30] = 0x00000000,c4_fltr_config[30] =
0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    c4_fldenable[31] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[31] = 0x00000000,c4_fltr_config[31] =
0x00000000
```

Real filters:

```
Filter 0: Not Installed (MIRROR1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x000e0000
Filter 5: Installed (ZONING TRAP)(LISTA)
```

fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x06007410,
fld negate ram = 0x019ffffff, fltr config ram = 0x000e0000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 10: Installed (WELL KNOWN ADDR)(FORWARD)
fld enable ram = 0x00000001, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x03ffffffe, fltr config ram = 0x00000054
Filter 11: Not Installed (SIM)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000054
Filter 12: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,

fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter dirty indicator: 0x00000000
Performance filters: 0
Port Mirror filters: 0 (0x0)

FIELD DATA

Shadowed fields:

fldoffset[0] = 0x05, fldmask[0] = 0x00, fldvalue_dyna[0]: 0xff 0x00
0x00 0x00
fldcontrol[0].inuse = 0x1000000 fldcontrol[0].refcnt = 0x01 0x00
0x00 0x00
fldoffset[1] = 0x00, fldmask[1] = 0x00, fldvalue_dyna[1]: 0x00 0x00
0x00 0x00
fldcontrol[1].inuse = 0x0 fldcontrol[1].refcnt = 0x00 0x00 0x00
0x00
fldoffset[2] = 0x00, fldmask[2] = 0x00, fldvalue_dyna[2]: 0x00 0x00
0x00 0x00
fldcontrol[2].inuse = 0x0 fldcontrol[2].refcnt = 0x00 0x00 0x00
0x00
fldoffset[3] = 0x00, fldmask[3] = 0x00, fldvalue_dyna[3]: 0x00 0x00
0x00 0x00
fldcontrol[3].inuse = 0x0 fldcontrol[3].refcnt = 0x00 0x00 0x00
0x00
fldoffset[4] = 0x00, fldmask[4] = 0x00, fldvalue_dyna[4]: 0x00 0x00
0x00 0x00
fldcontrol[4].inuse = 0x0 fldcontrol[4].refcnt = 0x00 0x00 0x00
0x00
fldoffset[5] = 0x00, fldmask[5] = 0x00, fldvalue_dyna[5]: 0x00 0x00
0x00 0x00
fldcontrol[5].inuse = 0x0 fldcontrol[5].refcnt = 0x00 0x00 0x00
0x00
fldoffset[6] = 0x00, fldmask[6] = 0x00, fldvalue_dyna[6]: 0x00 0x00
0x00 0x00
fldcontrol[6].inuse = 0x0 fldcontrol[6].refcnt = 0x00 0x00 0x00
0x00
fldoffset[7] = 0x00, fldmask[7] = 0x00, fldvalue_dyna[7]: 0x00 0x00
0x00 0x00
fldcontrol[7].inuse = 0x0 fldcontrol[7].refcnt = 0x00 0x00 0x00
0x00
fldoffset[8] = 0x00, fldmask[8] = 0x00, fldvalue_dyna[8]: 0x00 0x00
0x00 0x00
fldcontrol[8].inuse = 0x0 fldcontrol[8].refcnt = 0x00 0x00 0x00
0x00
fldoffset[9] = 0x00, fldmask[9] = 0x00, fldvalue_dyna[9]: 0x00 0x00
0x00 0x00
fldcontrol[9].inuse = 0x0 fldcontrol[9].refcnt = 0x00 0x00 0x00
0x00
fldoffset[10] = 0x00, fldmask[10] = 0x00, fldvalue_dyna[10]: 0x00 0x00
0x00 0x00
fldcontrol[10].inuse = 0x0 fldcontrol[10].refcnt = 0x00 0x00 0x00
0x00

```
fldoffset[11] = 0x00, fldmask[11] = 0x00, fldvalue_dyna[11]:0x00 0x00
0x00 0x00
fldcontrol[11].inuse = 0x0 fldcontrol[11].refcnt = 0x00 0x00 0x00
0x00
fldoffset[12] = 0x00, fldmask[12] = 0x00, fldvalue_dyna[12]:0x00 0x00
0x00 0x00
fldcontrol[12].inuse = 0x0 fldcontrol[12].refcnt = 0x00 0x00 0x00
0x00
fldoffset[13] = 0x00, fldmask[13] = 0x00, fldvalue_dyna[13]:0x00 0x00
0x00 0x00
fldcontrol[13].inuse = 0x0 fldcontrol[13].refcnt = 0x00 0x00 0x00
0x00
fldoffset[14] = 0x00, fldmask[14] = 0x00, fldvalue_dyna[14]:0x00 0x00
0x00 0x00
fldcontrol[14].inuse = 0x0 fldcontrol[14].refcnt = 0x00 0x00 0x00
0x00
fldoffset[15] = 0x00, fldmask[15] = 0x00, fldvalue_dyna[15]:0x00 0x00
0x00 0x00
fldcontrol[15].inuse = 0x0 fldcontrol[15].refcnt = 0x00 0x00 0x00
0x00
fldoffset[16] = 0x00, fldmask[16] = 0x00, fldvalue_dyna[16]:0x00 0x00
0x00 0x00
fldcontrol[16].inuse = 0x0 fldcontrol[16].refcnt = 0x00 0x00 0x00
0x00
fldoffset[17] = 0x00, fldmask[17] = 0x00, fldvalue_dyna[17]:0x00 0x00
0x00 0x00
fldcontrol[17].inuse = 0x0 fldcontrol[17].refcnt = 0x00 0x00 0x00
0x00
fldoffset[18] = 0x00, fldmask[18] = 0x00, fldvalue_dyna[18]:0x00 0x00
0x00 0x00
fldcontrol[18].inuse = 0x0 fldcontrol[18].refcnt = 0x00 0x00 0x00
0x00
fldoffset[19] = 0x00, fldmask[19] = 0x00, fldvalue_dyna[19]:0x00 0x00
0x00 0x00
fldcontrol[19].inuse = 0x0 fldcontrol[19].refcnt = 0x00 0x00 0x00
0x00
```

Real fields:

```
fldoffset RAM: 0x00000005, 0x00000000, 0x00000000, 0x00000000,
0x00000000
fldmask RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000
fld value4 RAM:
0x000000ff
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
```

0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000

Field dirty indicator: 0x00000000

FDB reference count fdb: 0 [1 0 0 0]
FDB reference count fdb: 1 [0 0 0 0]
FDB reference count fdb: 2 [0 0 0 0]
FDB reference count fdb: 3 [0 0 0 0]
FDB reference count fdb: 4 [0 0 0 0]
FDB reference count fdb: 5 [0 0 0 0]
FDB reference count fdb: 6 [0 0 0 0]
FDB reference count fdb: 7 [0 0 0 0]
FDB reference count fdb: 8 [0 0 0 0]
FDB reference count fdb: 9 [0 0 0 0]
FDB reference count fdb: 10 [0 0 0 0]
FDB reference count fdb: 11 [0 0 0 0]
FDB reference count fdb: 12 [0 0 0 0]
FDB reference count fdb: 13 [0 0 0 0]
FDB reference count fdb: 14 [0 0 0 0]
FDB reference count fdb: 15 [0 0 0 0]
FDB reference count fdb: 16 [0 0 0 0]
FDB reference count fdb: 17 [0 0 0 0]
FDB reference count fdb: 18 [0 0 0 0]
FDB reference count fdb: 19 [0 0 0 0]

Filter counters:

Filter counter 0: 0 (MIRROR1)
Filter counter 1: 0 (MIRROR2)
Filter counter 2: 0 (MIRROR3)
Filter counter 3: 0 (MIRROR4)
Filter counter 4: 0 (AEPORT_NON_MIRR_DROP)
Filter counter 5: 0 (ZONING TRAP)
Filter counter 6: 0 (FCR_EXPORT_DC)
Filter counter 7: 0 (TIN TRAP)
Filter counter 8: 0 (FICON CUP)
Filter counter 9: 0 (FICON CUP DST)
Filter counter 10: 0 (WELL KNOWN ADDR)
Filter counter 11: 0 (SIM)
Filter counter 12: 0 (UNUSED)
Filter counter 13: 0 (UNUSED)
Filter counter 14: 0 (UNUSED)
Filter counter 15: 0 (UNUSED)
Filter counter 16: 0 (PERF1)
Filter counter 17: 0 (PERF2)
Filter counter 18: 0 (PERF3)
Filter counter 19: 0 (PERF4)

Filter counter 20: 0 (PERF5)
Filter counter 21: 0 (PERF6)
Filter counter 22: 0 (PERF7)
Filter counter 23: 0 (PERF8)
Filter counter 24: 0 (PERF9)
Filter counter 25: 0 (PERF10)
Filter counter 26: 0 (PERF11)
Filter counter 27: 0 (PERF12)
Filter counter 28: 0 (OPM1)
Filter counter 29: 0 (OPM2)
Filter counter 30: 0 (IPM1)
Filter counter 31: 0 (IPM2)

ACL DATA

Logical port 30: Hard Zoning disabled, Soft Zoning disabled
Zone type: WWN Zoning
Frames with hard zone miss: 0

*** Please use filterportshow on user port 56 to display ACL hash tables and Mirroring resources of thischip.
***We show this data only for the first physical port which is an external port.

portFcPortCmdShow --slot 0 37 3
doing portFcPortCmdShow: arg1 = 3, arg2 = -2

portshow 37
portDisableReason: None
portCFlags: 0x1
portFlags: 0x20b03 PRESENT ACTIVE F_PORT G_PORT U_PORT
LOGICAL_ONLINE LOGIN NOELP ACCEPT FLOGI
LocalSwcFlags: 0x0
portType: 26.0
POD Port: Port is licensed
portState: 1 Online
Protocol: FC
portPhys: 6 In_Sync portScn: 32 F_Port
port generation number: 56
state transition count: 4

portId: 012500
portIfId: 4302001c
portWwn: 20:25:d8:1f:cc:2c:99:90
portWwn of device(s) connected:
10:00:00:10:9b:d2:24:4e
16b Area list:
Distance: normal
portSpeed: N16Gbps

FEC: Inactive
Credit Recovery: Active
Aoq: Inactive
FAA: Inactive


```

F_Trunk: Inactive
LE domain: 0
Peer beacon: Off
FC Fastwrite: OFF
Interrupts:      8          Link_failure: 1          Frjt:
0
Unknown:         0          Loss_of_sync: 0          Fbsy:
0
Lli:             8          Loss_of_sig: 1
Proc_rqrd:      1075       Protocol_err: 0
Timed_out:      0          Invalid_word: 510
Tx_unavail:     0          Invalid_crc: 1
Delim_err:      0          Address_err: 0
Lr_in:          2          0ls_in:      1
Lr_out:         1          0ls_out:     1

```

portloginshow 37

| Type | PID | World Wide Name | credit | df_sz | cos | |
|------|--------|-------------------------|--------|-------|-----|--------------|
| fe | 012500 | 10:00:00:10:9b:d2:24:4e | 80 | 2048 | 8 | scr=0x3 |
| ff | 012500 | 10:00:00:10:9b:d2:24:4e | 0 | 0 | 8 | d_id=FFFFFFA |
| ff | 012500 | 10:00:00:10:9b:d2:24:4e | 0 | 0 | 8 | d_id=FFFFFFC |

portloginshow 37 -history

| Type | PID | World Wide Name | logout time |
|------|--------|-------------------------|---------------------|
| fe | 012500 | 10:00:00:10:9b:d2:24:4e | 09/06/2024 17:34:15 |

portregshow 37

LED registers

```

=====
0x81ce2000: c4_led_status      000000ff    0x81ce2004:
c4_led_ctl      00000001

```

FPL registers

```

=====
0x81ce0200: fpl_port_config      23298232
0x81ce020c: fpl_port_id_ctl      00000005    0x81ce0210:
fpl_port_id_addr      00012500
0x81ce0214: fpl_port_speed      00000003    0x81ce021c:
fpl_lli_ctl      000000c0
0x81ce0228: fpl_lli_os_ctl      bc55bf45    0x81ce022c:
fpl_lli_send_word      bc95b5b5
0x81ce0230: fpl_lli_mark_rx      00000000    0x81ce0234:
fpl_lli_rnd_trip_time      00000000
0x81ce0238: fpl_lli_ns_status      02144000    0x81ce023c:
fpl_lli_intr_status      02000000
0x81ce0244: fpl_lli_def      00144000    0x81ce0254:
fpl_lli_intr_enable_clr      305e4007
0x81ce0258: fpl_err_intr_status      00000142    0x81ce0260:

```

```

fpl_err_intr_enable_clr 00000000
0x81ce0268: fpl_err_first_error 00000000 0x81ce026c:
fpl_speed_neg_ctl a404d3b8
0x81ce0270: fpl_speed_neg_stat 0000005c 0x81ce0274:
fpl_softasn_ctl 0000000f
0x81ce0278: fpl_link_init_ctl 00042d40 0x81ce027c:
fpl_link_init_stat 000000e0
0x81ce0280: fpl_aec_ctl 00181060 0x81ce0284:
fpl_aec_ctl2 04009f60
0x81ce0288: fpl_pcs_ctl 00000072 0x81ce028c:
fpl_fec_ctl 00000404
0x81ce0290: fpl_fec_cor 00000000 0x81ce0294:
fpl_fec_uncor 00000000
0x81ce0298: fpl_hss_link_ctl 0031f040 0x81ce029c:
fpl_afifo_link_ctl 00000a86
0x81ce02a0: fpl_echo_lb_ctl 0000028c 0x81ce02a4:
fpl_scratch 0000032a
0x81ce02a8: fpl_debug 00050005 0x81ce02ac:
fpl_misc_debug 00000400
0x00000000: SW_shadow_reg 00040000 0x00000000:
SW_c4_phyp->cfgptr 00030003

```

per-fpg (per octet) registers

=====

```

0x8181b82c: fpg_serdes_ctla0 81a37be7 0x8181b830:
fpg_serdes_ctla1 81a37be7
0x8181b834: fpg_serdes_ctlb0 81a1c3c3 0x8181b838:
fpg_serdes_ctlb1 81a1c3c3
0x8181b83c: fpg_serdes_xgmii_1ms 00067c28 0x8181b840:
fpg_serdes_regtimctl 40e47946
0x8181b844: fpg_serdes_asnrsttimctl 00000102

```

HSS PLL registers

=====

```

0x8181b400: 00_hssplla_vco_coarse_cal0 00000000 0x8181b404:
01_hssplla_vco_coarse_cal1 00000014
0x8181b408: 02_hssplla_vco_coarse_cal2 00000000 0x8181b40c:
03_hssplla_vco_coarse_cal3 00000000
0x8181b410: 04_hssplla_vco_coarse_cal4 00000000 0x8181b424:
09_hssplla_power_ctl 00000000
0x8181b428: 0A_hssplla_charge_pump_ctl 00000004 0x8181b438:
0E_hssplla_pll_misc_ctl 00000000
0x8181b43c: 0F_hssplla_pclk_ctl 000000f8 0x8181b440:
10_hssplla_eyem_intv_ctl 00000000
0x8181b444: 11_hssplla_eyem_intv_lim1 00000000 0x8181b448:
12_hssplla_eyem_intv_lim2 00000000
0x8181b44c: 13_hssplla_eyem_intv_lim3 00000000 0x8181b450:
14_hssplla_eyem_intv_lim4 00000000
0x8181b4f0: 3C_hssplla_macro_tst_ctl4 00000000 0x8181b4f4:
3D_hssplla_macro_tst_ctl3 00000000
0x8181b4f8: 3E_hssplla_macro_tst_ctl2 00000000 0x8181b4fc:
3F_hssplla_macro_tst_ctl1 00000000
0x8181b500: 00_hssppll_vco_coarse_cal0 0000000a 0x8181b504:
01_hssppll_vco_coarse_cal1 00000014

```

| | | |
|---|----------|-------------|
| 0x8181b508: 02_hsspll_b_vco_coarse_cal2 | 00000000 | 0x8181b50c: |
| 03_hsspll_b_vco_coarse_cal3 | 00000000 | |
| 0x8181b510: 04_hsspll_b_vco_coarse_cal4 | 00000000 | 0x8181b524: |
| 09_hsspll_b_power_ctl | 00000000 | |
| 0x8181b528: 0A_hsspll_b_charge_pump_ctl | 00000004 | 0x8181b538: |
| 0E_hsspll_b_pll_misc_ctl | 00000000 | |
| 0x8181b53c: 0F_hsspll_b_pclk_ctl | 000000f8 | 0x8181b540: |
| 10_hsspll_b_eyem_intv_ctl | 00000000 | |
| 0x8181b544: 11_hsspll_b_eyem_intv_lim1 | 00000000 | 0x8181b548: |
| 12_hsspll_b_eyem_intv_lim2 | 00000000 | |
| 0x8181b54c: 13_hsspll_b_eyem_intv_lim3 | 00000000 | 0x8181b550: |
| 14_hsspll_b_eyem_intv_lim4 | 00000000 | |
| 0x8181b5f0: 3C_hsspll_b_macro_tst_ctl4 | 00000000 | 0x8181b5f4: |
| 3D_hsspll_b_macro_tst_ctl3 | 00000000 | |
| 0x8181b5f8: 3E_hsspll_b_macro_tst_ctl2 | 00000000 | 0x8181b5fc: |
| 3F_hsspll_b_macro_tst_ctl1 | 00000000 | |

HSS TX registers

=====

| | | |
|--|----------|-------------|
| 0x8181a000: 00_hsstx_cfg_mode_PHY | 00009d48 | 0x8181a004: |
| 01_hsstx_test_ctl | 00000000 | |
| 0x8181a008: 02_hsstx_coeff_ctl_INV | 00000000 | 0x8181a00c: |
| 03_hsstx_drv_mode_ctl | 00000000 | |
| 0x8181a010: 04_hsstx_drv_ovrd_ctl | 00000010 | 0x8181a014: |
| 05_hsstx_dclk_align_ovrd | 00000080 | |
| 0x8181a018: 06_hsstx_imp_cal_ovrd | 00000c0c | 0x8181a01c: |
| 07_hsstx_dclk_drift_tol | 00000004 | |
| 0x8181a020: 08_hsstx_tap0_coeff_TUNE | 00000000 | 0x8181a024: |
| 09_hsstx_tap1_coeff_TUNE | 00000003 | |
| 0x8181a028: 0A_hsstx_tap2_coeff_TUNE | 00000019 | 0x8181a02c: |
| 0B_hsstx_tap3_coeff_TUNE | 00000003 | |
| 0x8181a034: 0D_hsstx_pol_INV | 00000004 | 0x8181a038: |
| 0E_hsstx_ae_cmd | 00000000 | |
| 0x8181a03c: 0F_hsstx_ae_stat | 00000000 | 0x8181a040: |
| 10_hsstx_ae_tap0_TUNE | 00000000 | |
| 0x8181a044: 11_hsstx_ae_tap1_TUNE | 00000000 | 0x8181a048: |
| 12_hsstx_ae_tap2_TUNE | 00000028 | |
| 0x8181a04c: 13_hsstx_ae_tap3_TUNE | 00000000 | 0x8181a054: |
| 15_hsstx_app_tune | 0000120e | |
| 0x8181a058: 16_hsstx_analog_diag | 00000000 | 0x8181a060: |
| 18_hsstx_4x_seg_app | 0000aaaa | |
| 0x8181a064: 19_hsstx_2x_seg_app | 000000f0 | 0x8181a068: |
| 1A_hsstx_1x_seg_app | 0000f508 | |
| 0x8181a06c: 1B_hsstx_seg_4x_term_app | 00000000 | 0x8181a070: |
| 1C_hsstx_seg_2x1x_term_app | 0000030d | |
| 0x8181a074: 1D_hsstx_tap_sign_app | 00000004 | 0x8181a078: |
| 1E_hsstx_ext_addr_data | 00000001 | |
| 0x8181a07c: 1F_hsstx_ext_addr_addr | 00000000 | 0x8181a080: |
| 20_hsstx_pat_buf_bytes_1_0 | 00000000 | |
| 0x8181a084: 21_hsstx_pat_buf_bytes_3_2 | 00000000 | 0x8181a088: |
| 22_hsstx_pat_buf_bytes_5_4 | 00000000 | |
| 0x8181a08c: 23_hsstx_pat_buf_bytes_7_6 | 00000000 | 0x8181a09c: |
| 27_hsstx_8023az_ctl | 00000000 | |
| 0x8181a0a0: 28_hsstx_dcc_ctl | 000060c0 | 0x8181a0a4: |

| | | | |
|---|----------|----------|-------------|
| 29_hsstx_dcc_ovrd | 00000000 | | |
| 0x8181a0a8: 2A_hsstx_dcc_app | | 00000104 | 0x8181a0ac: |
| 2B_hsstx_dcc_timeout | 0000ffff | | |
| 0x8181a0c0: 30_hsstx_tap_sign_ovrd | | 00000000 | 0x8181a0c8: |
| 32_hsstx_seg_4x_ovrd | 00000000 | | |
| 0x8181a0cc: 33_hsstx_seg_2x_ovrd | | 00000000 | 0x8181a0d0: |
| 34_hsstx_seg_1x_ovrd | 00000000 | | |
| 0x8181a0d8: 36_hsstx_tap_seg_4x_term_ovrd | | 00000000 | 0x8181a0dc: |
| 37_hsstx_tap_seg_2x_term_ovrd | 00000000 | | |
| 0x8181a0e0: 38_hsstx_tap_seg_1x_term_ovrd | | 00000000 | 0x8181a0ec: |
| 3B_hsstx_mac_test_ctl5 | 00000000 | | |
| 0x8181a0f0: 3C_hsstx_mac_test_ctl4 | | 00000000 | 0x8181a0f4: |
| 3D_hsstx_mac_test_ctl3 | 00000000 | | |
| 0x8181a0f8: 3E_hsstx_mac_test_ctl2 | | 00000000 | 0x8181a0fc: |
| 3F_hsstx_mac_test_ctl1 | 000000c6 | | |

HSS RX registers

=====

| | | | |
|---|----------|----------|-------------|
| 0x8181a200: 00_hssrx_cfg_mode_PHY | | 00009c78 | 0x8181a204: |
| 01_hssrx_test_ctl | 00000000 | | |
| 0x8181a208: 02_hssrx_phs_rot_ctl | | 0000cb80 | 0x8181a20c: |
| 03_hssrx_phs_rot_ofs_ctl | 00000610 | | |
| 0x8181a210: 04_hssrx_phs_rot_posn1 | | 0000071f | 0x8181a214: |
| 05_hssrx_phs_rot_posn2 | 0000000f | | |
| 0x8181a218: 06_hssrx_phs_rot_sta_ofs1 | | 00000001 | 0x8181a21c: |
| 07_hssrx_phs_rot_sta_ofs2 | 00000000 | | |
| 0x8181a220: 08_hssrx_dfe_ctl_PHY | | 00000002 | 0x8181a224: |
| 09_hssrx_dfe_smpl_snap1 | 00000000 | | |
| 0x8181a228: 0A_hssrx_dfe_smpl_snap2 | | 00008000 | 0x8181a22c: |
| 0B_hssrx_vga_ctl1 | 000041ee | | |
| 0x8181a230: 0C_hssrx_vga_ctl2 | | 00007b96 | 0x8181a234: |
| 0D_hssrx_vga_ctl3 | 000009e4 | | |
| 0x8181a238: 0E_hssrx_pwr_mgmt_ctl | | 0000001f | 0x8181a23c: |
| 0F_hssrx_iqamp_ctl1 | 0000001b | | |
| 0x8181a240: 10_hssrx_iqamp_ctl2 | | 00000006 | 0x8181a244: |
| 11_hssrx_dacap_dacan_sel | 00000003 | | |
| 0x8181a248: 12_hssrx_dacap_dacan | | 000032cc | 0x8181a24c: |
| 13_hssrx_daca_min | 00000e22 | | |
| 0x8181a250: 14_hssrx_adac_ctl | | 00000033 | 0x8181a254: |
| 15_hssrx_ac_cp_ctl | 000031c3 | | |
| 0x8181a258: 16_hssrx_ac_cp_val | | 0000004a | 0x8181a25c: |
| 17_hssrx_dfe_h1h2h3_lcl_off_ch | 00000014 | | |
| 0x8181a260: 18_hssrx_dfe_h1h2h3_lcl_off_val | | 00000000 | 0x8181a264: |
| 19_hssrx_peaked_intg | 000000ff | | |
| 0x8181a268: 1A_hssrx_cdr_analog_sw | | 0000ce00 | 0x8181a26c: |
| 1B_hssrx_peaking_amp_init_c_PHY | 00000000 | | |
| 0x8181a270: 1C_hssrx_dac_dpc | | 00000027 | 0x8181a274: |
| 1D_hssrx_ddc | 00004240 | | |
| 0x8181a278: 1E_hssrx_int_stat_PHY | | 0000ec9f | 0x8181a27c: |
| 1F_hssrx_dfe_func_ctl1_PHY | 0000ffff | | |
| 0x8181a280: 20_hssrx_dfe_func_ctl2_INV | | 00007ebf | 0x8181a284: |
| 21_hssrx_ofs_ch_dcc_qcc_idx | 00002000 | | |
| 0x8181a288: 22_hssrx_dfe_ofs_val | | 0000057e | 0x8181a28c: |
| 23_hssrx_h_coeff_bist | 00000401 | | |

| | | |
|--|----------------|-------------|
| 0x8181a290: 24_hssrx_ac_cap_bist | 00002093 | 0x8181a294: |
| 25_hssrx_max_gain_path_idx_res | 00007829 | |
| 0x8181a298: 26_hssrx_loff_ctl | 00000055 | 0x8181a29c: |
| 27_hssrx_sigdet_ctl | 000029a0 | |
| 0x8181a2a0: 28_hssrx_ana_ctl_sw | 00000000 | 0x8181a2a4: |
| 29_hssrx_intg_dac_ofs | 0000a0a1 | |
| 0x8181a2a8: 2A_hssrx_eye_ctl | 00004400 | 0x8181a2ac: |
| 2B_hssrx_eye_met | 00000004 | |
| 0x8181a2b0: 2C_hssrx_eye_met_err_cnt | 00000000 | 0x8181a2b4: |
| 2D_hssrx_eye_met_pdf_eyec | 00000000 | |
| 0x8181a2b8: 2E_hssrx_eye_met_pat_len | 0000007f | 0x8181a2bc: |
| 2F_hssrx_dfe_func_ctl3 | 0000dfff | |
| 0x8181a2c0: 30_hssrx_dfe_tap_ctl_idx_ptr | 00000008 | 0x8181a2c4: |
| 31_hssrx_dfe_tap | 00001122 | |
| 0x8181a2c8: 32_hssrx_lte_ctl_TUNE | 00000600 | 0x8181a2e4: |
| 39_hssrx_int_stat2 | 000041ff | |
| 0x8181a2e8: 3A_hssrx_ac_cpl_cur_src_adj | 00000041 | 0x8181a2ec: |
| 3B_hssrx_dcd_ctl | 00007c55 | |
| 0x8181a2f0: 3C_hssrx_dcc_ctl | 00000d00 | 0x8181a2f4: |
| 3D_hssrx_qcc_ctl | 00006947 | |
| 0x8181a2f8: 3E_hssrx_mac_test_ctl2 | 00000000 | 0x8181a2fc: |
| 3F_hssrx_mac_test_ctl1 | 00000000 | |
| 0x8181a248: 12_hssrx_dacap_dacan[02] | 38c8 32cc | |
| 0x8181a260: 18_hssrx_dfe_h1h2h3_lcl_off_va[00] | 0201 3f01 3e3d | |
| 0100 0005 3e01 003f 033f | | |
| 0x8181a260: 18_hssrx_dfe_h1h2h3_lcl_off_va[08] | 0200 3e00 3f01 | |
| 3f3f 3f00 3e00 3c02 0001 | | |
| 0x8181a260: 18_hssrx_dfe_h1h2h3_lcl_off_va[16] | 013d 3d3d 3e00 | |
| 3d00 0000 | | |
| 0x8181a288: 22_hssrx_dfe_ofs_val[00][00] | 057e 0000 7c7e | |
| 0000 0178 0000 | | |
| 0x8181a288: 22_hssrx_dfe_ofs_val[03][00] | 7b00 0000 7e0b | |
| 007f 7900 0000 | | |
| 0x8181a288: 22_hssrx_dfe_ofs_val[06][00] | 0404 7f00 7d02 | |
| 0000 7b7b 0000 | | |
| 0x8181a288: 22_hssrx_dfe_ofs_val[09][00] | 7801 0000 7806 | |
| 0000 007f 0000 | | |
| 0x8181a288: 22_hssrx_dfe_ofs_val[12][00] | 047c 7f00 797d | |
| 0000 7a7c 0000 | | |
| 0x8181a288: 22_hssrx_dfe_ofs_val[15][00] | 7f7a 0000 067e | |
| 7f00 7c00 0000 | | |
| 0x8181a288: 22_hssrx_dfe_ofs_val[18][00] | 7902 0000 7c7f | |
| 0000 0006 007f | | |
| 0x8181a288: 22_hssrx_dfe_ofs_val[21][00] | 0006 007f 0006 | |
| 007f 0006 007f | | |
| 0x8181a288: 22_hssrx_dfe_ofs_val[24][00] | 0501 0000 007b | |
| 0000 017d 0000 | | |
| 0x8181a294: 25_hssrx_max_gain_path_idx_res[00] | 0061 0857 1011 | |
| 188e 20df 289f 3084 38cd | | |
| 0x8181a294: 25_hssrx_max_gain_path_idx_res[08] | 40af 487f 5072 | |
| 5800 6040 683a 70c6 7829 | | |
| 0x8181a2c4: 31_hssrx_dfe_tap[00] | fffe 8181 4242 | |
| 2122 0011 0024 2324 2121 | | |
| 0x8181a2c4: 31_hssrx_dfe_tap[08] | 1122 2130 3030 | |

```

0d0d
0x8181a2e8: 3A_hssrx_ac_cpl_cur_src_adj[00]      0041 0041  0041
0041
0x8181a2ec: 3B_hssrx_dcd_ctl[00]      7c55 5c00  7c81
5c00  7c43
0x8181a2f0: 3C_hssrx_dcc_ctl[00]      0d00 0d41  0d42
0d42
0x8181a2f4: 3D_hssrx_qcc_ctl[00]      6900 6947

```

xfipcs, fec, aec, & aet registers

=====

```

0x81ce0400: xfipcs_reg      [00] 00002040 00000004 00000000
00000000  00000001 00000008 00000000 00000000
0x81ce0420: xfipcs_reg      [08] 00008001 00000000 00000000
00000000  00000000 00000000 00000000 00000000
0x81ce0440: xfipcs_reg      [16] 00000000 00000000 00000000
00000000  00000040 00000000 00000000 00000000
0x81ce0460: xfipcs_reg      [24] 00000000 00000000 00000000
00000000  00000000 00000000 00000000 00000000
0x81ce0480: xfipcs_reg      [32] 00001005 00008000 00000000
00000000  00000000 00000000 00000000 00000000
0x81ce0620: fec_32g_128g_reg [08] 00000000 00008003 00000000
00000000  00000000 00000000 00000000
0x81ce0648: fec_32g_128g_reg [18] 00000000 00000000 00000000
00000000  00000000 00000000 00000000 00000000
0x81ce0a00: aec_reg         [00] 00000000 00005000 00000000
00000000  00000740 0000ffe0 00000040 000024a2
0x81ce0c00: aet_reg         [00] 000000b0 00007000 000008c4
00000000  00000000

```

bbc registers

=====

```

0x81ce1800: bbc_trc      80  0  0  0  0  0  0
0
0x81ce1840: bbc_trc      0  0  0  0  0  0  0
0
0x81ce1880: bbc_trc      0  0  0  0  0  0  0
0
0x81ce18c0: bbc_trc      0  0  0  0  0  0  0
0
0x81ce1900: bbc_trc      0  0  0  0  0  0  0
0
0x81ce1804: bbc_mbc      0  0  0  0  0  0  0
0
0x81ce1844: bbc_mbc      0  0  0  0  0  0  0
0
0x81ce1884: bbc_mbc      0  0  0  0  0  0  0
0
0x81ce18c4: bbc_mbc      0  0  0  0  0  0  0
0
0x81ce1904: bbc_mbc      0  0  0  0  0  0  0
0
0x81ce1a00: bbc_rcc      0  0  0  0  0  0  0
0

```

| | | | | | | | |
|-------------------------------------|----------|---|---|---|---|----------------------|---|
| 0x81ce1a20: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81ce1a40: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81ce1a60: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81ce1a80: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81ce1c00: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81ce1c20: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81ce1c40: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81ce1c60: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81ce1c80: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81ce1d00: bbc_fbpc | 00000000 | | | | | 0x81ce1d04: bbc_csc | |
| 00000000 | | | | | | | |
| 0x81ce1d08: bbc_rcc_inc | 00000000 | | | | | 0x81ce1d0c: | |
| bbc_rqc_inc | 00000000 | | | | | | |
| 0x81ce1d10: bbc_fbpc_inc | 00000000 | | | | | 0x81ce1d14: | |
| bbc_tmc_inc | 00000000 | | | | | | |
| 0x81ce1d18: bbc_threshold | 00000010 | | | | | 0x81ce1d1c: | |
| bbc_counter_clr | 00000000 | | | | | | |
| 0x81ce1d20: bbc_debug_en | 00000000 | | | | | 0x81ce1d24: bbc_ctrl | |
| 00200220 | | | | | | | |
| 0x81ce1d28: bbc_rqc_rcc_thresh | 00000055 | | | | | 0x81ce1d34: | |
| bbc_bb_sc_n | 00000008 | | | | | | |
| 0x81ce1d38: bbc_crd_reco_debug | 00000000 | | | | | 0x81ce1d3c: | |
| bbc_crd_reco_debug_data | 00000000 | | | | | | |
| 0x81ce1d40: bbc_multi_frm_loss_cnt | 00000000 | | | | | 0x81ce1d44: | |
| bbc_multi_rdy_loss_cnt | 00000000 | | | | | | |
| 0x81ce1d48: bbc_1frm_loss_recov_cnt | 00000000 | | | | | 0x81ce1d4c: | |
| bbc_1rdy_loss_recov_cnt | 00000000 | | | | | | |
| 0x81ce1d58: bbc_int_status | 00000000 | | | | | 0x81ce1d5c: | |
| bbc_int_set | 00000000 | | | | | | |
| 0x81ce1d60: bbc_int_first | 00000000 | | | | | 0x81ce1d64: | |
| bbc_frm_rdy_rx_err_addr | 00000000 | | | | | | |
| 0x81ce1d68: bbc_frm_rdy_tx_err_addr | 00000000 | | | | | 0x81ce1d6c: | |
| bbc_trc_mbc_err_addr | 00000000 | | | | | | |
| 0x81ce1d70: bbc_frm_rdy_rx_dbl_ecc | 00000000 | | | | | 0x81ce1d74: | |
| bbc_frm_rdy_tx_dbl_ecc | 00000000 | | | | | | |
| 0x81ce1d78: bbc_trc_mbc_dbl_ecc | 00000000 | | | | | | |
| 0x81ce1d7c: bbc_fsm_status | 00001011 | | | | | 0x81ce1d80: | |
| bbc_force_err | 00000000 | | | | | | |
| 0x81ce1d84: bbc_crdt_avail0 | ffffffff | | | | | 0x81ce1d88: | |
| bbc_crdt_avail1 | 000000ff | | | | | | |
| 0x81ce1d8c: bbc_scratch | 00000000 | | | | | | |

FPS registers

=====

| | | | | | | | |
|---------------------------|----------|--|--|--|--|-------------|--|
| 0x81ce0004: fps_er_enc_in | 00000000 | | | | | 0x81ce0008: | |
|---------------------------|----------|--|--|--|--|-------------|--|

```

fps_er_crc          00000001
0x81ce000c: fps_er_trunc          00000000      0x81ce0010:
fps_er_toolong     00000000
0x81ce0014: fps_er_bad_eof        00000000      0x81ce0018:
fps_er_enc_out     00000000
0x81ce001c: fps_er_bad_os        00001f51      0x81ce0020:
fps_er_flush       00000000
0x81ce0024: fps_er_ifg           00000000      0x81ce0038:
fps_er_crc_good_eof 00000001
0x81ce003c: fps_inv_arb          00000000      0x81ce0040:
fps_slow_sts_status 00000000
0x81ce0044: fps_tx_frm_cnt         0088cf64      0x81ce0048:
fps_rx_frm_cnt     02a68fe3
0x81ce0050: fps_tx_word_cnt_hi      00000000      0x81ce004c:
fps_tx_word_cnt_lo 1e8cfc80
0x81ce0058: fps_rx_word_cnt_hi      00000004      0x81ce0054:
fps_rx_word_cnt_lo e8195905

```

BAL registers

=====

```

0x81ce7000: bal_desired_buf        00000008      0x81ce7004:
bal_alloc_buf      00000008
0x81ce7008: bal_busy_buf                00000006      0x81ce700c:
bal_usable_buf     00000008
0x81ce7010: bal_max_bor_buf            00000000
0x81ce7014: bal_busy_buf_thresh       00000006

```

TXQ registers

=====

```

0x81ce3004: txq_phys_port_ctl        004c0000
0x81ce3050: txq_link_skew              00000000
0x81ce3068: txq_cr_lk_dttm_intr_sts [00] 00000000 00000000
0x81ce3070: txq_cr_lk_dttm_intr_en [00] 00000001 00000000
0x81ce3024: txq_disc_frm_trap_cnt      00000014

```

FDS registers

=====

```

0x81ce4000: fds_rxf_ctl                00000008      0x81ce4004:
fds_rxf_wait_thresh 00000c06
0x81ce4018: fds_rxf_first_error        00000000      0x81ce401c:
fds_rxf_first_error_info 00000000
0x81ce4020: fds_rxf_inout_pkt_cnt      69ed69ed
0x81ce4008: fds_rxf_err_int_status     00000000      0x81ce4024:
fds_rxf_fifo_status 00488888
0x81ce5000: fds_txf_ctl                00000008      0x81ce5004:
fds_txf_wait_ifg_thresh 00a00106
0x81ce5008: fds_txf_err_int_status     00000000      0x81ce5024:
fds_txf_fifo_status 00088888
0x81ce502c: fds_txf_bbc_scs           00000028

```

Logical TXQ registers

=====

```

0x81ce3000: txq_log_port_ctl          00000011      0x81ce3008:
txq_port_status     00000000

```



```

0x81ce300c: txq_todo_flags [00] 00000000 00000000
0x81ce3014: txq_spd_match_desc [00] 00000000 388a388a 00000000
00000000
0x81ce3024: txq_spd_match_desc [04] 00000014
0x81ce3028: txq_vc_weight [00] 25252501 19010125 3c3c3c19
25013c3c
0x81ce3038: txq_vc_weight [04] 01252525 01010101 01010101
01010101
0x81ce3048: txq_vc_weight [08] 01010101 00010101
0x81ce3054: txq_cong_dttm_ctrl 00000106
0x81ce3058: txq_cong_dttm_intr_sts [00] 00000000 00000000
0x81ce3060: txq_cong_dttm_intr_en [00] 00000000 00000000
0x81ce3078: txq_bw_limit_en_reg [00] 00000000 00000000
0x81ce3080: txq_bw_gua_en_reg [00] 00000000 00000000
0x81ce3088: txq_vc_group [00] 03030300 03030303 03030303
03030303
0x81ce3098: txq_vc_group [04] 03030303 03030303 03030303
03030303
0x81ce30a8: txq_vc_group [08] 03030303 03030303 00000000
00000000
0x81ce30b0: txq_bw_thresh_group [00] 00000000 00000000 00000000
00000000
0x81ce30c0: txq_bw_thresh_group [04] 00000000 00000000 00000000
00000000
0x81ce30d0: txq_bw_thresh_group [08] 00000000 00000000 00000000
00000000
0x81ce30e0: txq_bw_thresh_group [12] 00000000 00000000 00000000
00000000
0x81ce30f0: txq_bw_thresh_group [16] 00000000 00000000 00000000
00000000
0x81ce3100: txq_bw_thresh_group [20] 00000000 00000000 00000000
00000000
0x81ce3110: txq_bw_thresh_group [24] 00000000 00000000 00000000
00000000
0x81ce3120: txq_bw_thresh_group [28] 00000000 00000000 00000000
00000000
0x81ce3130: txq_bw_thresh_group [32] 00000000 00000000 00000000
00000000
0x81ce3140: txq_bw_thresh_group [36] 00000000 00000000 00000000
00000000

```

txq Congestion detection Statistics RAM

```

=====
0x81091180: vc[0] 00000000 0x81091184: vc[1]
00000000
0x81091188: vc[2] 00000000 0x8109118c: vc[3]
00000000
0x81091190: vc[4] 00000000 0x81091194: vc[5]
00000000
0x81091198: vc[6] 00000000 0x8109119c: vc[7]
00000000
0x810911a0: vc[8] 00000000 0x810911a4: vc[9]
00000000
0x810911a8: vc[10] 00000000 0x810911ac: vc[11]

```

```

00000000
0x810911b0: vc[12]      00000000      0x810911b4: vc[13]
00000000
0x810911b8: vc[14]      00000000      0x810911bc: vc[15]
00000000
0x810911c0: vc[16]      00000000      0x810911c4: vc[17]
00000000
0x810911c8: vc[18]      00000000      0x810911cc: vc[19]
00000000
0x810911d0: vc[20]      00000000      0x810911d4: vc[21]
00000000
0x810911d8: vc[22]      00000000      0x810911dc: vc[23]
00000000
0x810911e0: vc[24]      00000000      0x810911e4: vc[25]
00000000
0x810911e8: vc[26]      00000000      0x810911ec: vc[27]
00000000
0x810911f0: vc[28]      00000000      0x810911f4: vc[29]
00000000
0x810911f8: vc[30]      00000000      0x810911fc: vc[31]
00000000
0x81091200: vc[32]      00000000      0x81091204: vc[33]
00000000
0x81091208: vc[34]      00000000      0x8109120c: vc[35]
00000000
0x81091210: vc[36]      00000000      0x81091214: vc[37]
00000000
0x81091218: vc[38]      00000000      0x8109121c: vc[39]
00000000

```

Logical STS registers

=====

```

0x81585584: sts_ftb_type1_miss      00000000
0x81585588: sts_ftb_type2_miss      00000000
0x8158558c: sts_ftb_type6_miss      00000000
0x81585590: sts_hard_zoning_miss     00000000
0x81585594: sts_lun_zoning_miss     00000000
0x8158559c: sts_unroutable          00000000
0x815825b4: sts_rte_cl2              00000000      0x815825b8:
sts_rte_cl3              02a68fe3      0x815825bc: sts_rte_link_ctl
00000000      0x815855a8: sts_tx_timeout      00000000

```

Logical STS filter registers

=====

```

0x81585500: stsflt_trig      [00] 00000000 00000000 00000000
00000000
0x81585510: stsflt_trig      [04] 00000000 00000000 00000000
00000000
0x81585520: stsflt_trig      [08] 00000000 00000000 00000000
00000000
0x81585530: stsflt_trig      [12] 00000000 00000000 00000000
00000000
0x81585540: stsflt_trig      [16] 00000000 00000000 00000000

```

```

00000000
0x81585550: sts_flt_trig [20] 00000000 00000000 00000000
00000000
0x81585560: sts_flt_trig [24] 00000000 00000000 00000000
00000000
0x81585570: sts_flt_trig [28] 00000000 00000000 00000000
00000000
0x81585580: sts_flt_trig [32]

```

Logical STS discard registers

=====

```

0x815838b0: disc_mcast_wka 00000000 0x815838b4:
disc_inv_did 00000000
0x815838b8: disc_cl1_cl4 00000000 0x815838bc:
disc_sid_chk_fail 00000000
0x815838c0: disc_inv_dom_egid_txpt 00000000 0x815838c4:
disc_vft_hop_cnt_1 00000000
0x815838c8: disc_classf 00000000 0x815838cc:
disc_fcp_cdb_inv 00000000
0x815838d0: disc_vfid_trap_enabled 00000000 0x815838d4:
disc_vfid_hdr_chk_fail 00000000
0x815838d8: disc_shim_cksum_fail 00000000 0x815838dc:
disc_fed_edit_cmd_err 00000000
0x815838e0: disc_ftb_vm_mode 00000000 0x815838e4:
disc_ftb_agnt2_miss 00000000
0x815838e8: disc_ecb_reserved 00000000 0x815838ec:
disc_ecb_de_pad_err 00000000
0x815838f0: disc_ecb_de_tag_err 00000000 0x815838f4:
disc_ecb_de_seq_err 00000000
0x815838f8: disc_ecb_err 00000000 0x815838fc:
disc_ftb_type4_match 00000000
0x81583900: disc_fcp_rsp_ftb_type4 00000000 0x81583904:
disc_ftb_type5_match 00000000
0x81583908: disc_ftb_type3_match 00000000 0x8158390c:
disc_els_ftb_type3 00000000
0x81583910: disc_ftb_type1_match 00000000 0x81583914:
disc_els_rsp_ex_port 00000000
0x81583918: disc_inv_drp_dps 00000000 0x8158391c:
disc_did_lookup_miss 00000000
0x81583920: disc_ftb_type2_match 00000000 0x81583924:
disc_trpd_plogi_pdisc 00000000
0x81583928: disc_type2_lookup_miss 00000000 0x8158392c:
disc_ftb_type6_match 00000000
0x81583930: disc_els_rep_ex_port 00000000 0x81583934:
disc_els_sid_lkup_bit1 00000000
0x81583938: disc_els_sid_lkup_bit0 00000000 0x8158393c:
disc_bls_frm_trap_bit1 00000000
0x81583940: disc_ftb_token_err 00000000 0x81583944:
disc_asic_internal_err 00000000
0x81583948: disc_hard_zone_miss 00000000 0x8158394c:
disc_lun_zone_miss 00000000
0x81583950: disc_flt_frame_disc 00000000 0x81583954:
disc_flt_parity_err 00000000
0x81583958: disc_frame_marked_du 00000000 0x8158395c:

```

```
disc_frame_marked_to 00000000
0x81583960: disc_lkup_rte_prty_err 00000000
```

portstatsshow 37

```
stat_wtx          512555998      4-byte words transmitted
stat_wrx          21073838131     4-byte words received
stat_ftx          8965976      Frames transmitted
stat_frx          44470225     Frames received
stat_c2_frx       0          Class 2 frames received
stat_c3_frx       44470243     Class 3 frames received
stat_lc_rx        0          Link control frames
received
stat_mc_rx        0          Multicast frames
received
stat_mc_to        0          Multicast timeouts
stat_mc_tx        0          Multicast frames
transmitted
tim_txcrd_z       0          Time TX Credit Zero
(2.5Us ticks)
tim_txcrd_z_vc   0- 3: 0          0          0          0
tim_txcrd_z_vc   4- 7: 0          0          0          0
tim_txcrd_z_vc   8-11: 0         0          0          0
tim_txcrd_z_vc  12-15: 0         0          0          0
lat_tot_pkt_vc   0- 3: 1          1          1          1
lat_tot_pkt_vc   4- 7: 1          1          1          1
lat_tot_pkt_vc   8-11: 1          1          1          1
lat_tot_pkt_vc  12-15: 1          1          1          1
lat_hi_time_vc   0- 3: 0          0          0          0
lat_hi_time_vc   4- 7: 0          0          0          0
lat_hi_time_vc   8-11: 0         0          0          0
lat_hi_time_vc  12-15: 0         0          0          0
lat_lo_time_vc   0- 3: 1          1          1          1
lat_lo_time_vc   4- 7: 1          1          1          1
lat_lo_time_vc   8-11: 1          1          1          1
lat_lo_time_vc  12-15: 1          1          1          1
max_latency_vc   0- 3: 1          1          1          1
max_latency_vc   4- 7: 1          1          1          1
max_latency_vc   8-11: 1          1          1          1
max_latency_vc  12-15: 1          1          1          1
latency_dma_ts   09-09-2024 UTC Mon 08:47:24      TXQ
Latency DMA TimeStamp
fec_cor_detected 0          Count of blocks that
were corrected by FEC
fec_uncor_detected 0         Count of blocks that
were left uncorrected by FEC
er_enc_in        0          Encoding errors inside
of frames
er_crc           1          Frames with CRC errors
er_trunc         0          Frames shorter than
minimum
er_toolong       0          Frames longer than
maximum
er_bad_eof       0          Frames with bad end-of-
```

| | | | |
|--------------------------|-----------------------------|--|--------------------------|
| frame | | | |
| er_enc_out | 0 | | Encoding error outside |
| of frames | | | |
| er_bad_os | 8017 | | Invalid ordered set |
| er_pcs_blk | 510 | | PCS block errors |
| er_rx_c3_timeout | 0 | | Class 3 receive frames |
| discarded due to timeout | | | |
| er_tx_c3_timeout | 0 | | Class 3 transmit frames |
| discarded due to timeout | | | |
| er_unroutable | 0 | | Frames that are |
| unroutable | | | |
| er_unreachable | 0 | | Frame with unreachable |
| destination | | | |
| er_other_discard | 0 | | Other discards |
| er_type1_miss | 0 | | frames with FTB type 1 |
| miss | | | |
| er_type2_miss | 0 | | frames with FTB type 2 |
| miss | | | |
| er_type6_miss | 0 | | frames with FTB type 6 |
| miss | | | |
| er_zone_miss | 0 | | frames with hard zoning |
| miss | | | |
| er_lun_zone_miss | 0 | | frames with LUN zoning |
| miss | | | |
| er_crc_good_eof | 1 | | Crc error with good eof |
| er_inv_arb | 0 | | Invalid ARB |
| er_single_credit_loss | 0 | | Single vcrdy/frame loss |
| on link | | | |
| er_multi_credit_loss | 0 | | Multiple vcrdy/frame |
| loss on link | | | |
| other_credit_loss | 0 | | Link timeout/complete |
| credit loss | | | |
| phy_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | | Timestamp of |
| phy_port stats clear | | | |
| lgc_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | | Timestamp of |
| lgc_port stats clear | | | |
| fec_corrected_rate | 0 | | FEC Corrected blocks per |
| second | | | |

portstats64show 37

| | | |
|---------------|------------|--|
| stat64_wtx | 0 | top_int : 4-byte words transmitted |
| | 512554459 | bottom_int : 4-byte words transmitted |
| stat64_wrx | 4 | top_int : 4-byte words received |
| | 3893712688 | bottom_int : 4-byte words received |
| stat64_ftx | 0 | top_int : Frames transmitted |
| | 8965862 | bottom_int : Frames transmitted |
| stat64_frx | 0 | top_int : Frames received |
| | 44469678 | bottom_int : Frames received |
| stat64_c2_frx | 0 | top_int : Class 2 frames received |
| | 0 | bottom_int : Class 2 frames received |
| stat64_c3_frx | 0 | top_int : Class 3 frames received |
| | 44469887 | bottom_int : Class 3 frames received |
| stat64_lc_rx | 0 | top_int : Link control frames received |
| | 0 | bottom_int : Link control frames |

| | | | |
|---|-------|------------|--------------------------------|
| received | | | |
| stat64_mc_rx | 0 | top_int | : Multicast frames received |
| | 0 | bottom_int | : Multicast frames received |
| stat64_mc_to | 0 | top_int | : Multicast timeouts |
| | 0 | bottom_int | : Multicast timeouts |
| stat64_mc_tx | 0 | top_int | : Multicast frames transmitted |
| | 0 | bottom_int | : Multicast frames |
| transmitted | | | |
| tim64_rdy_pri | 0 | top_int | : Time R_RDY high priority |
| | 0 | bottom_int | : Time R_RDY high priority |
| tim64_txcrd_z | 0 | top_int | : Time BB_credit zero |
| | 0 | bottom_int | : Time BB_credit zero |
| er64_enc_in | 0 | top_int | : Encoding errors inside of |
| frames | 0 | bottom_int | : Encoding errors inside of |
| frames | | | |
| er64_crc | 0 | top_int | : Frames with CRC errors |
| | 1 | bottom_int | : Frames with CRC errors |
| er64_trunc | 0 | top_int | : Frames shorter than minimum |
| | 0 | bottom_int | : Frames shorter than minimum |
| er64_toolong | 0 | top_int | : Frames longer than maximum |
| | 0 | bottom_int | : Frames longer than maximum |
| er64_bad_eof | 0 | top_int | : Frames with bad end-of-frame |
| | 0 | bottom_int | : Frames with bad end-of- |
| frame | | | |
| er64_enc_out | 0 | top_int | : Encoding error outside of |
| frames | 0 | bottom_int | : Encoding error outside of |
| frames | | | |
| er64_disc_c3 | 0 | top_int | : Class 3 frames discarded |
| | 0 | bottom_int | : Class 3 frames discarded |
| er64_pcs_blk | 0 | top_int | : PCS block errors |
| | 510 | bottom_int | : PCS block errors |
| stat64_rateTxFrame | 35 | | Tx frame rate (fr/sec) |
| stat64_rateRxFrame | 132 | | Rx frame rate (fr/sec) |
| stat64_rateTxPeakFrame | 0 | | Tx peak frame rate (fr/sec) |
| stat64_rateRxPeakFrame | 0 | | Rx peak frame rate (fr/sec) |
| stat64_rateTxWord | 472 | | Tx Word rate (words/sec) |
| stat64_rateRxWord | 60212 | | Rx Word rate (words/sec) |
| stat64_rateTxPeakWord | 0 | | Tx peak Word rate (words/sec) |
| stat64_rateRxPeakWord | 0 | | Rx peak Word rate (words/sec) |
| stat64_PRJTframes | 0 | top_int | : Number of PRJT frames |
| returned to this port | 0 | bottom_int | : Number of PRJT |
| frames returned to this port | | | |
| stat64_PBSYframes | 0 | top_int | : Number of PBSY frames |
| returned to this port | 0 | bottom_int | : Number of PBSY |
| frames returned to this port | | | |
| stat64_inputBuffersFull | 0 | top_int | : Number of occurrences |
| when all input buffers full | 0 | bottom_int | : Number of |
| occurrences when all input buffers full | | | |
| stat64_rxClass1Frames | 0 | top_int | : Number of class 1 |

```

frames received
                                0                bottom_int : Number of class 1
frames received
stat64_aveTxFrameSize  13                Average Tx Frame size
stat64_aveRxFrameSize  456                Average Rx Frame size
Lr_in                   0                top_int
                                2                bottom_int
Ols_in                  0                top_int
                                1                bottom_int
Lr_out                  0                top_int
                                1                bottom_int
Ols_out                 0                top_int
                                1                bottom_int
Link_failure            0                top_int
                                1                bottom_int
Invalid_CRC             0                top_int
                                1                bottom_int
Invalid_word            0                top_int
                                510            bottom_int
Protocol_err            0                top_int
                                0                bottom_int
Loss_of_sig             0                top_int
                                1                bottom_int
Loss_of_sync            0                top_int
                                0                bottom_int
er_bad_os               0                top_int : Invalid ordered set
                                8017            bottom_int: Invalid ordered set

```

```

portrouteshow 37
port address ID: 0x012500
external unicast routing table:
    0: Embedded
    255: Embedded
internal unicast routing table:

```

```
portcamshow 37
```

```

-----
Port  SID used  DID used  SID entries  DID entries
37    5         1        012600      012500
                010b00
                012500
                010c00
                010a00
-----

```

```
SID free, DID free: (59205, 59205)
```

```

ptbufshow, ptcreditshow, ptdatashow, ptstatsshow 37
S:
S:VF Enable:           1
S:
S:C4 Global Variable:
S:-----
-----

```

```

S:trace_stop:          0
S:
S:C4 Phy Data Pointers: c4_phyp = 0xb6af0000
S:-----
-----
S:tnodep                0xbb84b7e0      pt
      0x4302801c
S:proto_phyp            0xb880b900      phy_cfg
0xb6af1040
S:c4_chp                0x97e28000      c4_lgcp
0x97fb8000
S:c4_phy_regp           0x81ce0000      proc_dir
0xb851e280
S:-----
-----
S:magic_id              0xc4345678      num_port_timer      12
S:prev_if_id            0x4302001c      S:ftx
8965976      tov      0
S:initialized           1      port_idx            28
S:ui_idx                37      slot_no
0
S:blade_idx             28      sw_usr_ports        400
S:unused                0      intr_debounced
0
S:aec_status            0x0      reason_code
0
S:debug                 0x00000004      debug_trc_line      0
S:rxbuf_list_head       0xffffffff      rxbuf_list_tail     0x35
S:isAePort              0      port_misc_data
0
S:num_fault1_rx_disc    0      num_fault2_rx_disc  0
S:p_lli_cause0          2      p_sig_regained      2
S:p_sync_regained       0      enc_out
0x0
S:cached_fps_status     0      cached_sts_status   0
S:cached_er_crc_good_eof 0
S:cached_er_bad_os      0      cached_er_too_long  0
S:cached_er_trunc       0
cached_tot_er_crc_good_eof 0
S:num_pt_excess_intr    0      num_no_fid          0
S:num_fault1_cnt        0      num_fault2_cnt
0
S:num_fault_lip         0      num_fault_lli       0
S:num_fault_rx_fifo     0      num_fault_hss       0
S:num_fault_bwait       0      lli_intr_prim
0
S:num_sw_link_to        0
be_link_err_mon_count  0
S:ecb_enc_enabled       0      ecb_comp_enabled
0
S:ecb_rsv_enc           0      ecb_rsv_comp        0
S:ecb_enc_bm            0x0      ecb_key_index
0xffffffff
S:fab_idx               0

```



```

S:num_be_lto          0          lto_count_reset_intvl
  0
S:lr_count_reset_intvl      0          num_be_lr
  0
S:num_fault_qsfps      0          check_lto
  0
S:credit_loaded          80          num_credit_overrun
  0
S:fec_enabled           0x0          fec_los_to_flag          0x0
S:phy_stats_clear_ts      1725611419  pcs_err_online
  510
S:pcs_err_light_det       510          pcs_err_ignore
  0
S:pcs_blk_err           510          pcs_hiber          0
S:phy_port_status        2          ecb_enc_lr_count
  0
S:dport_mode            0          avoid_lto_det          0
S:sn_debounced           0x0          sn_started_kr_reqd      1
S:major_timer_started     0x0          ready_bm          0x0
S:parln_1_bm             0x0          parln_0_bm          0x0
S:be_los_of_sync_event_intvl
be_los_of_sync_event      0          0
S:errataPtenable_cntr     0          errataPoll_cntr
  0
S:jda_rx_sig_loss_det     0          jda_rx_sig_loss_cnt
  0
S:encrypt_blk_error       0
S:
S:      c4_trunk
S:=====
S:mark_ts                0x0          deskew          0x0
S:master_phyp             0x0
S:
S:adelay[00]: 0x00000000 0x00000000 0x00000000 0x00000000
S:adelay[04]: 0x00000000 0x00000000 0x00000000 0x00000000
S:
S:      c4_buf
S:=====
S:tx_csc                  0          rx_csc
  0
S:ld_vc_credits           0          tx_flag          0x0
S:alloc_buffers           8          req_buffers       8
S:est_buffers             20          ld_use_est        0
S:bb_sc_n                 8          rx_bb_sc_n
  8
S:data_cr                 5          nondata_cr
  6
S:cr_enable               0
S:ld_nondata_cr           6          tnodep
0xbb84b8c0
S:tx_credits[0] 0 0 0 0 0 0 0 0
S:tx_credits[8] 0 0 0 0 0 0 0 0
S:tx_credits[16] 0 0 0 0 0 0 0 0 0
S:tx_credits[24] 0 0 0 0 0 0 0 0 0

```

```

S:tx_credits[32]      0      0      0      0      0      0      0      0      0
S:rx_credits[0] 0    0    0    0    0    0    0    0    0
S:rx_credits[8] 0    0    0    0    0    0    0    0    0
S:rx_credits[16]      0      0      0      0      0      0      0      0      0
S:rx_credits[24]      0      0      0      0      0      0      0      0      0
S:rx_credits[32]      0      0      0      0      0      0      0      0      0
S:tx_mbc[0]      0    0    0    0    0    0    0    0    0
S:tx_mbc[8]      0    0    0    0    0    0    0    0    0
S:tx_mbc[16]     0    0    0    0    0    0    0    0    0
S:tx_mbc[24]     0    0    0    0    0    0    0    0    0
S:tx_mbc[32]     0    0    0    0    0    0    0    0    0
S:rx_mbc[0]      0    0    0    0    0    0    0    0    0
S:rx_mbc[8]      0    0    0    0    0    0    0    0    0
S:rx_mbc[16]     0    0    0    0    0    0    0    0    0
S:rx_mbc[24]     0    0    0    0    0    0    0    0    0
S:rx_mbc[32]     0    0    0    0    0    0    0    0    0

```

S:

S:C4 Chip Variables: c4_phyp->c4_chp = 0x97e28000

S:-----

S:version = 2.1

S:magic_id 0xc4234567 init_state 0x8

S:reset_reg_mem 0x1

S:ch_int0_en_bm 0x0 intr0_cause 0x0

S:ch_int1_en_bm 0x0 intr1_cause 0x0

S:ch_int2_en_bm 0x0 intr2_cause 0x0

S:ch 0x43010080 ch_cfg

0xb7013ba0

S:raslog_hndl.hndl 0x0 obj_halted 0x0

S:c4_chip_regp 0x80000000 c4_fpg_regp

0x81800000

S:num_chip_timer 0x5

S:hi_task_bm 0x0 lo_task_bm 0x0

S:c4_deferq.q_head 0x0 c4_deferq.q_tail 0x0

S:c4_tmrq.q_head 0x0 c4_tmrq.q_tail 0x0

slot_no 0

S:chip_inst 0 chip_idx 0

S:pll_initialized 1

pll_serdes_initialized 1

S:init_tries 0 init_ptEnableBM

0xba01b488

S:tick_polling 0xb980c9c0 sec_polling

0xb980c960

S:bb_fid 129

S:ecb_key_bm[0] 0x0 ecb_key_bm[1] 0x0

S:ecb_key_bm[2] 0x0 ecb_key_bm[3] 0x0

S:is_chip_enc_enabled 0

is_chip_comp_enabled 0x0

S:ftb_rsrcp->ftb_flags 0x0 act_rsrcp->act_flag 0x1

S:lue_rsrcp->lue_flags[0] 0x0 lue_rsrcp-

>lue_flags[1] 0x0

S:c4_phyp[00]: 0xb6ab0000 0xb6ab2080 0xb6ab4100 0xb6ab6180

S:c4_phyp[04]: 0xb6ab9040 0xb6abb0c0 0xb6abd140 0xb6ac0000

S:c4_phyp[08]: 0xb6ac2080 0xb6ac4100 0xb6ac6180 0xb6ac9040

```

S:c4_phyp[12]: 0xb6acb0c0 0xb6acd140 0xb6ad0000 0xb6ad2080
S:c4_phyp[16]: 0xb6ad4100 0xb6ad6180 0xb6ad9040 0xb6adb0c0
S:c4_phyp[20]: 0xb6add140 0xb6ae0000 0xb6ae2080 0xb6ae4100
S:c4_phyp[24]: 0xb6ae6180 0xb6ae9040 0xb6aeb0c0 0xb6aed140
S:c4_phyp[28]: 0xb6af0000 0xb6af2080 0xb6af4100 0xb6af6180
S:c4_phyp[32]: 0xb6af9040 0xb6afb0c0 0xb6afd140 0xb6b00000
S:c4_phyp[36]: 0xb6b02080 0xb6b04100 0xb6b06180 0xb6b09040
S:c4_phyp[40]: 0xb6b0b0c0 0xb6b0d140 0xb6b10000 0xb6b12080
S:c4_phyp[44]: 0xb6b14100 0xb6b16180 0xb6b19040 0xb6b1b0c0
S:c4_phyp[48]: 0xb6b1d140 0xb6b20000 0xb6b22080 0xb6b24100
S:c4_phyp[52]: 0xb6b26180 0xb6b29040 0xb6b2b0c0 0xb6b2d140
S:c4_phyp[56]: 0xb6b30000 0xb6b32080 0xb6b34100 0xb6b36180
S:c4_phyp[60]: 0xb6b39040 0xb6b3b0c0 0xb6b3d140 0xb6b40000
S:c4_lgcp[00]: 0x97f48000 0x97f4c000 0x97f50000 0x97f54000
S:c4_lgcp[04]: 0x97f58000 0x97f5c000 0x97f60000 0x97f64000
S:c4_lgcp[08]: 0x97f68000 0x97f6c000 0x97f70000 0x97f74000
S:c4_lgcp[12]: 0x97f78000 0x97f7c000 0x97f80000 0x97f84000
S:c4_lgcp[16]: 0x97f88000 0x97f8c000 0x97f90000 0x97f94000
S:c4_lgcp[20]: 0x97f98000 0x97f9c000 0x97fa0000 0x97fa4000
S:c4_lgcp[24]: 0x97fa8000 0x97fac000 0x97fb0000 0x97fb4000
S:c4_lgcp[28]: 0x97fb8000 0x97fbc000 0x97fc0000 0x97fc4000
S:c4_lgcp[32]: 0x97fc8000 0x97fcc000 0x97fd0000 0x97fd4000
S:c4_lgcp[36]: 0x97fd8000 0x97fdc000 0x97fe0000 0x97fe4000
S:c4_lgcp[40]: 0x97fe8000 0x97fec000 0x97ff0000 0x97ff4000
S:c4_lgcp[44]: 0x97ff8000 0x97ffc000 0x8e000000 0x8e004000
S:c4_lgcp[48]: 0x8e008000 0x8e00c000 0x8e010000 0x8e014000
S:c4_lgcp[52]: 0x8e018000 0x8e01c000 0x8e020000 0x8e024000
S:c4_lgcp[56]: 0x8e028000 0x8e02c000 0x8e030000 0x8e034000
S:c4_lgcp[60]: 0x8e038000 0x8e03c000 0x8e040000 0x8e044000
S:chip_timers[00]: 0xb980c720 0xb980c780 0xb980c7e0 0xb980c840
S:chip_timers[04]: 0xb980c8a0 0xb980c900
S:disc_trap_enable_required      0x0          rxlp_disc_log_stop
          0x0
S:curr_rxlp_frm_cnt      0x0          curr_rxlp_disc_frm_cnt  0x0
S:sw_disc_frm_cnt      0x0          last_disc_frm_cnt      0x0
S:txq_nopop_pr_cnt      0x0          pollErrataDfe_ptBM
0xba01b4b0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][0]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][1] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][2]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][0] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][1]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][2] 0x0
S:
S:C4 Logical Port Variables
S:-----
-----
S:c4_lgc_regp      0x81ce0000
S:c4_phyp:
S:      0xb6af0000      0x0          0x0          0x0

S:      0x0          0x0          0x0          0x0

S:master_phyp      0xb6af0000      if_id

```

```

0x4302001c
S:min_phyp          0x0          max_phyp          0x0
S:num_phy_ports     1          lgc_num          28
S:num_iu_to         0          sw_txq_bm
0
S:port_fid         128         unused           0
S:port_group       3          lgc_stats_clear_ts
1725611419
S:domain_tbl_sel   92          area_tbl_sel
28
S:egid_tbl_sel     2
S:serv_lo_bm       0x0
S:

```

S:Proto Phy Variables:

```

S:-----
-----

```

```

S:magic_id         0xc4123456   asic_phyp
0xb6af0000
S:port_id          0x4302801c   phy_cfg
0xb6af1040
S:upsm_hdl         0xb8018f00   physm_hdl
0xb8018c80
S:ov_snsn_hdl     0xb8018b40   sw_snsn_hdl
0xb8018be0
S:ov_lksm_hdl     0xb8018d20   sw_lksm_hdl
0xb8018dc0
S:trksm_hdl       0xb8018e60   lr_flag          0x0
S:lr_active       0x0          qsfm_txxrx_rate_sel
0x0

```

S:

```

S:UPSM           UP22: UPST_G_PORT          --> UP23: UPST_F_PORT
S:SNSM(OV)       SN02: OV_SNST_HW_NEG        --> SN04: OV_SNST_NEGOTIATED
S:SNSM(SW)       SW00: SW_SNST_STAGE_WS    --> SW00: SW_SNST_STAGE_WS
S:PHYSM          PP04: PHYST_NO_SYNC         --> PP05: PHYST_IN_SYNC
S:LKSM(OV)       LK07: OV_LKST_SW_RESET        --> LK04: OV_LKST_ACTIVE
S:LKSM(SW)       SW12: LR2_ACWT           --> SW00: AC
S:TRKSM          TRK0: TRKST_INIT         --> TRK0: TRKST_INIT

```

S:

S:physm variables:

```

S:-----
-----

```

```

S:proto_phyp      0xb880b900   physm_hdl
0xb8018c80
S:force_offline   0          copper           0
S:fault_reason    0: UNKNOWN
S:phy_media_present 1

```

S:

S:snsn variables:

```

S:-----
-----

```

```

S:speed          0x8          proto_phyp
0xb880b900
S:hw_sn_tries_left 0x64         sw_sn_tries_left 0x0
S:curr_txsp_count 0x0

```

```

S:tx_max          0x0          curr_tx_indx
   0x0
S:curr_tx         0x0          curr_rxsp_count
   0x0
S:rx_max          0x0          curr_rx_indx
   0x0
S:curr_rx         0x0          rx_mem
   0x0
S:rxsp_rec_count  0x0
S:nc_start        0x0          tx_start          0x0
S:sync_start      0x0          sync_present    0x0
S:diag_auto       0x0          diag_speed      0xff
S:striped_wd_tov  3000        hw_wd_tov
   3000
S:step            0x0          qsfp28_speed_mode
   0x0
S:qsfp_mode0_hw_sn_tries_left  0x0
S:qsfp_mode1_hw_sn_tries_left  0x0
S:
S:lksm variables:
S:-----
-----
S:proto_phy      0xb880b900    ov_lksm_hdl
0xb8018d20
sw_lksm_hdl      0xb8018dc0
num_lf1          0
S:hw_link_tries_left  9          sw_link_tries_left  5
S:buf_ptype      0x1          stored_entry_state  0x2
S:handshake_owner 0x0          mark_unsent
   0x0
S:busybuf_stuck  0x0          lr_wait          0x0
S:
S:trksm variables:
S:-----
-----
S:Not a trunk port
S:
S:upsm variables:
S:-----
-----
S:proto_phy      0xb880b900    upsm_hdl
0xb8018f00
S:bb_credits     80          port_beacon        0
S:port_diag_flag 0          force_offline
   0
S:port_fault_rsn 0: PORT_NO_FAULT
S:retry_init_rsn 0: UNKNOWN
S:limit_reason   0          limit_result        0
S:ie_fctl_mode   0          fec_in_sync_tries_left  0
S:retry_sn_fail_init 0
retry_link_fail_init 0
S:excess_lr_count 0
S:
S:c4_ch_cfg

```

```

S:-----
-----
S:c4_desc_ring_size      256      292      256      256      292
292      2      292      292
S:thresh_def            0      16      1      0
S:intr_tries            500      cmem_pattern
0xdeadbeef
S:cmem_pattern_upwd     2      cmem_init_time      16
S:cmem_init_tries      5
S:ctrl_par_thresh      2      data_par_thresh
4
S:cam_par_thresh        4      buf_loss_thresh
12
S:crit_par_thresh      2      non_crit_par_thresh
6
S:pci_abort_thresh     10      pci_err_thresh      5
S:excess_chintr_thresh 8      sw_err_thresh      20
S:err_sample_period    300      intr_sleep
20000
S:frame_timeout        2500      proxy_dev      16384
S:vf_route             81920      qos      2048
S:stats 2048           f_redirect      2048
S:rsp_trap             2048      lun_zoning      20480
S:area_mode            0      ftb_max_loop[0]    0
S:ftb_max_loop[1]      6      ftb_max_loop[2]    9
S:ftb_max_loop[3]      10     ftb_max_loop[4]    10
S:ftb_max_loop[5]      5      ftb_max_loop[6]    6
S:ftb_seg_size[0]      0      ftb_seg_size[1]
16384
S:ftb_seg_size[2]      65536     ftb_seg_size[3]
16384
S:ftb_seg_size[4]      16384     ftb_seg_size[5]
65536
S:ftb_seg_size[6]      16384     ftb_seg_base[0]    0
S:ftb_seg_base[1]      0      ftb_seg_base[2]
65536
S:ftb_seg_base[3]      16384     ftb_seg_base[4]
32768
S:ftb_seg_base[5]      131072    ftb_seg_base[6]
49152
asic_err_monitor_period1 300
asic_err_monitor_period2 86400
zone_chk_to_poll_period 25
zone_chk_class2_reject_tov
S:
S:c4_phy_cfg
S:-----
-----
S:version = 2.1
S:pt                    0x4302801c      fab_ptr
0x9a800000
S:fabattr                0x9a8000d4      fab_iop
0x9a800050
S:cfgbm                  0xbb84b624      port_ctrl

```

```

0xb6af1058
S:pcap.pcap_bm          0x8d215547      pcap.pcap2_bm
0x588289
S:pcap.pcap3_bm        0x1bebe0c
ui_idx                  37              S:slot_no
    0
is_icl                  0              S:sw_usr_ports      400
S:neg_speed            10 8 5 0 0 0
S:my_domain            0x1
S:hw_sn_maxtries      100            sw_sn_maxtries
    0
S:hw_link_maxtries    10            sw_link_maxtries    5
S:rx_cyc_tov          28            rttov               300
S:bufrdy_tov          300          busybuf_tov         286
S:mark_tov            300          lksm_tov            3000
S:buf_dealloc_wait    4            hw_wd_tov           3000
S:hw_lk_train_tov     540          hw_lk_test_tov
    150
S:syswait_tx_12_lips  1            lip_rx_tov          55
S:al_time_tov         15          lp_tov              2000
S:intr_tries_port     500          intr_mod_debounce
    250
S:intr_lsrflt_debounce 500          intr_efifo_debounce 100
S:port_no_fid         3            excess_ptintr_thresh 8
S:port_fault1_thresh  100          port_fault1_spur_thresh 250
S:port_fault1_disc_thresh 500
port_fault1_disc_spur_thresh 1000
S:port_fault2_thresh  5            losync_tov          100
S:port_sw_link_to     15          en_8g_scramble
    1
frc_hw_sn_mode         0x1
S:enc_poll_thresh     0            fec_enable
    0
S:fec_in_sync_to      50          fec_in_sync_try_max
    4
S:port_be_lto_threshold 100          port_be_lr_threshold
    2
S:be_cr_in_sync_to    5
port_credit_overrun_thresh 10
S:jda_sfp_losig_tov   400
jda_sfp_losig_try_max 30
S:striped_wd_tov      3000
no_sync_debounce      1200
S:
S:    fab_iop
S:=====
S:fab_iop->interop_mode 0x0      fab_iop->lab_mode    0x0
S:fab_iop->fl_bbc      0x0          fab_iop->fl_fan
    0x0
S:fab_iop->fl_cls      0x4          fab_iop->fl_rscn
    0x0
S:fab_iop->domain_id_offset 0x60      fab_iop-
>mcdt_fabric_mode     0x0
S:fab_iop->mcdt_default_zone 0x0          fab_iop-

```

```

>mcddt_safe_zone          0x0
S:
S:   port_ctrl
S:=====
S:port_ctrl.port_type    1          port_ctrl.port_grp      3
S:port_ctrl.port_number 37          port_ctrl.vc_mode       1
S:
S:   port_ctrl.lcap
S:=====
S:has_serdes             0          has_media              1
S:topology               1          skip_nego              0
S:skip_pnego            0          skip_init_event       0
S:en_shim                0          speed_neg              0
S:en_shim                1
S:loop_back              0          num_speeds            5
S:fec_enable             0
S:
S:   port_ctrl.speed_list array
S:=====
S:speed_list[0].auto_neg 1          speed_list[0].lnk_speed 0x0000000a
S:speed_list[1].auto_neg 1          speed_list[1].lnk_speed 0x00000008
S:speed_list[2].auto_neg 0          speed_list[2].lnk_speed 0x00000006
S:speed_list[3].auto_neg 1          speed_list[3].lnk_speed 0x00000005
S:speed_list[4].auto_neg 0          speed_list[4].lnk_speed 0x00000003
S:speed_list[5].auto_neg 0          speed_list[5].lnk_speed 0x00000000
S:
S:   port_ctrl.cm
S:=====
S:port_ctrl.cm.num_vcs      8
S:port_ctrl.cm.min_bufs    8
S:port_ctrl.cm.cr_shar_bufs 0
S:port_ctrl.vc_alloc
S:port_ctrl.vc_alloc      2 0 1 1 1 1 1 1
S:port_ctrl.vc_alloc      0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.norm_vc_alloc
S:port_ctrl.norm_vc_alloc  4 0 5 5 5 5 1 1
S:port_ctrl.norm_vc_alloc  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.cm.skip_bb_credit      0
S:port_ctrl.cm.use_shim_based_sublist 0
S:
S:   port_ctrl.serdes_set
S:=====
S:serdes_type              0x8
S:serdes_data_t.ibm_hss_serdes.tx_drive_power      0x1
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b_sign 0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b      0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_a      0x0
S:serdes_data_t.ibm_hss_serdes.rxeq                0x0
S:
S:   cfgbm
S:=====
S:old_distance            0x0          gport_lockdown        0x0

```



```

S:tport          0x1          speed          0x0
S:disable_eport  0x0          fcacc          0x0
S:lport_lockdown 0x0          0x0          priv_lport_lockdown
          0x0
S:vcxlt_linit   0x0          delay_flogi    0x0
S:isl_interop   0x0          distance       0x0
S:BufStarvFlag  0x0          credit_sharing 0x0
S:lport_halfduplex 0x0          lport_fairness 0x0
S:soft_neg      0x0          asn_frc_hwretry 0x0
S:cr_recov      0x0          fport_buffers  0x0
S:export        0x0          0x0          export_mode
          0x0
S:csctl_en      0x0          mirror_port    0x0
S:fault_delay   0x0          non_dfe        0x0
S:fec_configured*(0=ENAB) 0          0          fec_tts
          0
S:port_persistently_disabled (permanently) 0 (0)
S:
S:      cfg property
S:=====
S:priv_pcfg_bm  0x00000000  lgcl_pcfg_bm
0xbb84b664
S:fport_buffer  0x00000000
S:
S:
S:C4 Discard Cntrs: rxlp_stats = 0xb6af03b0
S:-----
-----
S:disc_mcast_wka  0x0          disc_inv_did    0x0
S:disc_cl1_cl4    0x0          disc_sid_chk_fail 0x0
S:disc_inv_dom_egid_txpt 0x9          disc_vft_hop_cnt_1
          0x0
S:disc_classf     0x0          disc_fcp_cdb_inv 0x0
S:disc_vfid_trap_enabled 0x0
disc_vfid_hdr_chk_fail 0x0
S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err 0x0
S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err 0x0
S:disc_ftb_vm_mode 0x0          disc_ftb_agnt2_miss 0x0
S:disc_ecb_de_pad_err 0x0          disc_ecb_de_tag_err 0x0
S:disc_ecb_de_seq_err 0x0          disc_ecb_err 0x0
S:disc_ftb_type4_match 0x0          disc_fcp_rsp_ftb_type4 0x0
S:disc_fcp_rsp_ftb_type4 0x0          disc_ftb_type5_match
          0x0
S:disc_ftb_type3_match 0x0          disc_els_ftb_type3 0x0
S:disc_ftb_type1_match 0x0          disc_els_rsp_ex_port 0x0
S:disc_inv_drp_dps 0x0          disc_did_lookup_miss 0x0
S:disc_ftb_type2_match 0x0          disc_trpd_plogi_pdisc 0x0
S:disc_type2_lookup_miss 0x0          disc_ftb_type6_match
          0x0
S:disc_els_rep_ex_port 0x0          disc_els_sid_lkup_bit1 0x0
S:disc_els_sid_lkup_bit0 0x0
disc_bls_frm_trap_bit1 0x0
S:disc_ftb_token_err 0x0          disc_asic_internal_err 0x0
S:disc_hard_zone_miss 0x0          disc_lun_zone_miss 0x0

```

```

S:disc_flt_frame_disc 0x0          disc_flt_parity_err 0x0
S:disc_frame_marked_du 0x0        disc_frame_marked_to 0x0
E:Connection type: FE
E:Port type: F_port
E:Trunk port: No
E:Configured Speed: AUTO_SPEED_NEGO
E:Max Capable Speed: 32G
E:Current SNSM Speed: 16G
E:Hardware TX Speed: 16G (0x00000003)
E:Hardware RX Speed: 32G (0x00000040)
E:
E:Interrupts:      8          Link_failure:      1
Loss_of_sync:     0          Loss_of_sig:      1
E:Lli:            8          Invalid_word:     0
E:trapped_frm:   1075        fwd_status_ok:   1075
E:fwd_timeout:   0          fwd_tx_unavail:  0
E:fwd_unroutable: 0          fwd_zone_out:    0
E:fwd_other_err: 0          frm_err_discard: 0
E:Fltr listA:    0          Fltr listB:      0
E:Zone trap fwd: 0          Zone trap disc:  0
E:shim_csum:     0          RTE_perr:        0
E:Invalid_crc:  0          Delim_err:       0
E:Protocol_err: 0
E:Lr_in:         2          Lr_out:          1
E:Ols_in:        1          Ols_out:         1

```

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FILTER DATA

Shadow settings:

```

Filter Enable: 0x00000420
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000

```

Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass: 0x00000019

Real settings:

Enable RAM: 0x00000420, 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass RAM: 0x00000019

Shadowed filters:

Filter 0: Not Installed (MIRROR1)(LISTA)

c4_fldenable[0] = 0x00000000 0x00000000 0x00000000
0x00000000

c4_fldnegate[0] = 0x00000000, c4_fltr_config[0] = 0x00000000

Filter 1: Not Installed (MIRROR2)(LISTA)
c4_fldenable[1] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[1] = 0x00000000,c4_fltr_config[1] = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
c4_fldenable[2] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[2] = 0x00000000,c4_fltr_config[2] = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
c4_fldenable[3] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[3] = 0x00000000,c4_fltr_config[3] = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
c4_fldenable[4] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[4] = 0x00000000,c4_fltr_config[4] = 0x00000000
Filter 5: Installed (ZONING TRAP)(LISTA)
c4_fldenable[5] = 0x00000000 0x00000000 0x00000000
0x06007c10
c4_fldnegate[5] = 0xfd9ffffff,c4_fltr_config[5] = 0x000001c0
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
c4_fldenable[6] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[6] = 0x00000000,c4_fltr_config[6] = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
c4_fldenable[7] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[7] = 0x00000000,c4_fltr_config[7] = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
c4_fldenable[8] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[8] = 0x00000000,c4_fltr_config[8] = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
c4_fldenable[9] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[9] = 0x00000000,c4_fltr_config[9] = 0x00000000
Filter 10: Installed (WELL KNOWN ADDR)(FORWARD)
c4_fldenable[10] = 0x00000001 0x00000000 0x00000000
0x00000000
c4_fldnegate[10] = 0xffffffff,c4_fltr_config[10] =
0x00000054
Filter 11: Not Installed (SIM)(LISTA)
c4_fldenable[11] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[11] = 0x00000000,c4_fltr_config[11] =
0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
c4_fldenable[12] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[12] = 0x00000000,c4_fltr_config[12] =
0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
c4_fldenable[13] = 0x00000000 0x00000000 0x00000000
0x00000000

```
    c4_fldnegate[13] = 0x00000000,c4_fltr_config[13] =
0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
    c4_fldenable[14] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[14] = 0x00000000,c4_fltr_config[14] =
0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
    c4_fldenable[15] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[15] = 0x00000000,c4_fltr_config[15] =
0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
    c4_fldenable[16] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[16] = 0x00000000,c4_fltr_config[16] =
0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
    c4_fldenable[17] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[17] = 0x00000000,c4_fltr_config[17] =
0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
    c4_fldenable[18] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[18] = 0x00000000,c4_fltr_config[18] =
0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
    c4_fldenable[19] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[19] = 0x00000000,c4_fltr_config[19] =
0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
    c4_fldenable[20] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[20] = 0x00000000,c4_fltr_config[20] =
0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
    c4_fldenable[21] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[21] = 0x00000000,c4_fltr_config[21] =
0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
    c4_fldenable[22] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[22] = 0x00000000,c4_fltr_config[22] =
0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
    c4_fldenable[23] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[23] = 0x00000000,c4_fltr_config[23] =
0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
    c4_fldenable[24] = 0x00000000 0x00000000 0x00000000
```

```
0x00000000
    c4_fldnegate[24] = 0x00000000,c4_fltr_config[24] =
0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
    c4_fldenable[25] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[25] = 0x00000000,c4_fltr_config[25] =
0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
    c4_fldenable[26] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[26] = 0x00000000,c4_fltr_config[26] =
0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
    c4_fldenable[27] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[27] = 0x00000000,c4_fltr_config[27] =
0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
    c4_fldenable[28] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[28] = 0x00000000,c4_fltr_config[28] =
0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
    c4_fldenable[29] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[29] = 0x00000000,c4_fltr_config[29] =
0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    c4_fldenable[30] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[30] = 0x00000000,c4_fltr_config[30] =
0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    c4_fldenable[31] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[31] = 0x00000000,c4_fltr_config[31] =
0x00000000
```

Real filters:

```
Filter 0: Not Installed (MIRROR1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
```

Filter 3: Not Installed (MIRROR4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x000e0000

Filter 5: Installed (ZONING TRAP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x06007c10,
fld negate ram = 0x019ffffff, fltr config ram = 0x000e0000

Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 7: Not Installed (TIN TRAP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 8: Not Installed (FICON CUP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 9: Not Installed (FICON CUP DST)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 10: Installed (WELL KNOWN ADDR)(FORWARD)
fld enable ram = 0x00000001, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x03ffffffe, fltr config ram = 0x00000054

Filter 11: Not Installed (SIM)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000054

Filter 12: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 13: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 14: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 15: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 16: Not Installed (PERF1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,

0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 30: Not Installed (IPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter dirty indicator: 0x00000000
Performance filters: 0
Port Mirror filters: 0 (0x0)

FIELD DATA

Shadowed fields:

fldoffset[0] = 0x05, fldmask[0] = 0x00, fldvalue_dyna[0]: 0xff 0x00
0x00 0x00
fldcontrol[0].inuse = 0x1000000 fldcontrol[0].refcnt = 0x01 0x00
0x00 0x00
fldoffset[1] = 0x00, fldmask[1] = 0x00, fldvalue_dyna[1]: 0x00 0x00
0x00 0x00
fldcontrol[1].inuse = 0x0 fldcontrol[1].refcnt = 0x00 0x00 0x00
0x00
fldoffset[2] = 0x00, fldmask[2] = 0x00, fldvalue_dyna[2]: 0x00 0x00
0x00 0x00
fldcontrol[2].inuse = 0x0 fldcontrol[2].refcnt = 0x00 0x00 0x00
0x00
fldoffset[3] = 0x00, fldmask[3] = 0x00, fldvalue_dyna[3]: 0x00 0x00
0x00 0x00
fldcontrol[3].inuse = 0x0 fldcontrol[3].refcnt = 0x00 0x00 0x00
0x00
fldoffset[4] = 0x00, fldmask[4] = 0x00, fldvalue_dyna[4]: 0x00 0x00
0x00 0x00
fldcontrol[4].inuse = 0x0 fldcontrol[4].refcnt = 0x00 0x00 0x00
0x00
fldoffset[5] = 0x00, fldmask[5] = 0x00, fldvalue_dyna[5]: 0x00 0x00
0x00 0x00
fldcontrol[5].inuse = 0x0 fldcontrol[5].refcnt = 0x00 0x00 0x00
0x00
fldoffset[6] = 0x00, fldmask[6] = 0x00, fldvalue_dyna[6]: 0x00 0x00
0x00 0x00
fldcontrol[6].inuse = 0x0 fldcontrol[6].refcnt = 0x00 0x00 0x00
0x00
fldoffset[7] = 0x00, fldmask[7] = 0x00, fldvalue_dyna[7]: 0x00 0x00
0x00 0x00
fldcontrol[7].inuse = 0x0 fldcontrol[7].refcnt = 0x00 0x00 0x00
0x00
fldoffset[8] = 0x00, fldmask[8] = 0x00, fldvalue_dyna[8]: 0x00 0x00
0x00 0x00
fldcontrol[8].inuse = 0x0 fldcontrol[8].refcnt = 0x00 0x00 0x00

```
0x00
fldoffset[9] = 0x00, fldmask[9] = 0x00, fldvalue_dyna[9]:0x00 0x00
0x00 0x00
fldcontrol[9].inuse = 0x0 fldcontrol[9].refcnt = 0x00 0x00 0x00
0x00
fldoffset[10] = 0x00, fldmask[10] = 0x00, fldvalue_dyna[10]:0x00 0x00
0x00 0x00
fldcontrol[10].inuse = 0x0 fldcontrol[10].refcnt = 0x00 0x00 0x00
0x00
fldoffset[11] = 0x00, fldmask[11] = 0x00, fldvalue_dyna[11]:0x00 0x00
0x00 0x00
fldcontrol[11].inuse = 0x0 fldcontrol[11].refcnt = 0x00 0x00 0x00
0x00
fldoffset[12] = 0x00, fldmask[12] = 0x00, fldvalue_dyna[12]:0x00 0x00
0x00 0x00
fldcontrol[12].inuse = 0x0 fldcontrol[12].refcnt = 0x00 0x00 0x00
0x00
fldoffset[13] = 0x00, fldmask[13] = 0x00, fldvalue_dyna[13]:0x00 0x00
0x00 0x00
fldcontrol[13].inuse = 0x0 fldcontrol[13].refcnt = 0x00 0x00 0x00
0x00
fldoffset[14] = 0x00, fldmask[14] = 0x00, fldvalue_dyna[14]:0x00 0x00
0x00 0x00
fldcontrol[14].inuse = 0x0 fldcontrol[14].refcnt = 0x00 0x00 0x00
0x00
fldoffset[15] = 0x00, fldmask[15] = 0x00, fldvalue_dyna[15]:0x00 0x00
0x00 0x00
fldcontrol[15].inuse = 0x0 fldcontrol[15].refcnt = 0x00 0x00 0x00
0x00
fldoffset[16] = 0x00, fldmask[16] = 0x00, fldvalue_dyna[16]:0x00 0x00
0x00 0x00
fldcontrol[16].inuse = 0x0 fldcontrol[16].refcnt = 0x00 0x00 0x00
0x00
fldoffset[17] = 0x00, fldmask[17] = 0x00, fldvalue_dyna[17]:0x00 0x00
0x00 0x00
fldcontrol[17].inuse = 0x0 fldcontrol[17].refcnt = 0x00 0x00 0x00
0x00
fldoffset[18] = 0x00, fldmask[18] = 0x00, fldvalue_dyna[18]:0x00 0x00
0x00 0x00
fldcontrol[18].inuse = 0x0 fldcontrol[18].refcnt = 0x00 0x00 0x00
0x00
fldoffset[19] = 0x00, fldmask[19] = 0x00, fldvalue_dyna[19]:0x00 0x00
0x00 0x00
fldcontrol[19].inuse = 0x0 fldcontrol[19].refcnt = 0x00 0x00 0x00
0x00
```

Real fields:

```
fldoffset RAM: 0x00000005, 0x00000000, 0x00000000, 0x00000000,
0x00000000
fldmask RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000
fld value4 RAM:
0x000000ff
```

0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000

Field dirty indicator: 0x00000000

FDB reference count fdb: 0 [1 0 0 0]
FDB reference count fdb: 1 [0 0 0 0]
FDB reference count fdb: 2 [0 0 0 0]
FDB reference count fdb: 3 [0 0 0 0]
FDB reference count fdb: 4 [0 0 0 0]
FDB reference count fdb: 5 [0 0 0 0]
FDB reference count fdb: 6 [0 0 0 0]
FDB reference count fdb: 7 [0 0 0 0]
FDB reference count fdb: 8 [0 0 0 0]
FDB reference count fdb: 9 [0 0 0 0]
FDB reference count fdb: 10 [0 0 0 0]
FDB reference count fdb: 11 [0 0 0 0]
FDB reference count fdb: 12 [0 0 0 0]
FDB reference count fdb: 13 [0 0 0 0]
FDB reference count fdb: 14 [0 0 0 0]
FDB reference count fdb: 15 [0 0 0 0]
FDB reference count fdb: 16 [0 0 0 0]
FDB reference count fdb: 17 [0 0 0 0]
FDB reference count fdb: 18 [0 0 0 0]
FDB reference count fdb: 19 [0 0 0 0]

Filter counters:

- Filter counter 0: 0 (MIRROR1)
- Filter counter 1: 0 (MIRROR2)
- Filter counter 2: 0 (MIRROR3)
- Filter counter 3: 0 (MIRROR4)
- Filter counter 4: 0 (AEPORT_NON_MIRR_DROP)
- Filter counter 5: 0 (ZONING TRAP)
- Filter counter 6: 0 (FCR_EXPORT_DC)
- Filter counter 7: 0 (TIN TRAP)
- Filter counter 8: 0 (FICON CUP)
- Filter counter 9: 0 (FICON CUP DST)
- Filter counter 10: 0 (WELL KNOWN ADDR)

Filter counter 11: 0 (SIM)
Filter counter 12: 0 (UNUSED)
Filter counter 13: 0 (UNUSED)
Filter counter 14: 0 (UNUSED)
Filter counter 15: 0 (UNUSED)
Filter counter 16: 0 (PERF1)
Filter counter 17: 0 (PERF2)
Filter counter 18: 0 (PERF3)
Filter counter 19: 0 (PERF4)
Filter counter 20: 0 (PERF5)
Filter counter 21: 0 (PERF6)
Filter counter 22: 0 (PERF7)
Filter counter 23: 0 (PERF8)
Filter counter 24: 0 (PERF9)
Filter counter 25: 0 (PERF10)
Filter counter 26: 0 (PERF11)
Filter counter 27: 0 (PERF12)
Filter counter 28: 0 (OPM1)
Filter counter 29: 0 (OPM2)
Filter counter 30: 0 (IPM1)
Filter counter 31: 0 (IPM2)

ACL DATA

Logical port 28: Hard Zoning enabled, Soft Zoning disabled
Zone type: WWN Zoning
Frames with hard zone miss: 0

*** Please use filterportshow on user port 56 to display ACL hash tables and Mirroring resources of thischip.
***We show this data only for the first physical port which is an external port.

portFcPortCmdShow --slot 0 38 3
doing portFcPortCmdShow: arg1 = 3, arg2 = -2

portshow 38
portDisableReason: None
portCFlags: 0x1
portFlags: 0x20b03 PRESENT ACTIVE F_PORT G_PORT U_PORT
LOGICAL_ONLINE LOGIN NOELP ACCEPT FLOGI
LocalSwcFlags: 0x0
portType: 26.0
POD Port: Port is licensed
portState: 1 Online
Protocol: FC
portPhys: 6 In_Sync portScn: 32 F_Port
port generation number: 32
state transition count: 11

portId: 012600
portIfId: 4302001b
portWwn: 20:26:d8:1f:cc:2c:99:90
portWwn of device(s) connected:

20:08:94:90:10:e3:bd:d0

16b Area list:

Distance: normal

portSpeed: N32Gbps

FEC: Active

Credit Recovery: Inactive

Aoq: Inactive

FAA: Inactive

F_Trunk: Inactive

LE domain: 0

Peer beacon: Off

FC Fastwrite: OFF

Interrupts: 9 Link_failure: 1 Frjt:

0

Unknown: 0 Loss_of_sync: 0 Fbsy:

0

Lli: 9 Loss_of_sig: 0

Proc_rqrd: 103 Protocol_err: 0

Timed_out: 0 Invalid_word: 0

Tx_unavail: 0 Invalid_crc: 0

Delim_err: 0 Address_err: 0

Lr_in: 1 Ols_in: 1

Lr_out: 1 Ols_out: 1

portloginshow 38

| Type | PID | World Wide Name | credit | df_sz | cos | |
|------|--------|-------------------------|--------|-------|-----|--------------|
| fe | 012600 | 20:08:94:90:10:e3:bd:d0 | 255 | 2048 | 8 | scr=0x3 |
| ff | 012600 | 20:08:94:90:10:e3:bd:d0 | 0 | 0 | 8 | d_id=FFFC01 |
| ff | 012600 | 20:08:94:90:10:e3:bd:d0 | 0 | 0 | 8 | d_id=FFFFFFA |
| ff | 012600 | 20:08:94:90:10:e3:bd:d0 | 0 | 0 | 8 | d_id=FFFFFC |

portloginshow 38 -history

| Type | PID | World Wide Name | logout time |
|------|--------|-------------------------|---------------------|
| fe | 012600 | 20:08:94:90:10:e3:bd:d0 | 09/05/2024 06:39:21 |
| fe | 012600 | 20:08:94:90:10:e3:bd:d0 | 09/05/2024 07:08:44 |
| fe | 012600 | 20:08:94:90:10:e3:bd:d0 | 09/05/2024 07:38:13 |
| fe | 012600 | 20:08:94:90:10:e3:bd:d0 | 09/06/2024 07:11:49 |
| fe | 012600 | 20:08:94:90:10:e3:bd:d0 | 09/06/2024 08:28:56 |

portregshow 38

LED registers

=====

0x81cda000: c4_led_status 000000ff 0x81cda004:
c4_led_ctl 00000001

FPL registers

=====

| | | | |
|-------------|-------------------------|----------|-------------|
| 0x81cd8200: | fpl_port_config | 23298232 | |
| 0x81cd820c: | fpl_port_id_ctl | 00000005 | 0x81cd8210: |
| | fpl_port_id_addr | 00012600 | |
| 0x81cd8214: | fpl_port_speed | 00000004 | 0x81cd821c: |
| | fpl_lli_ctl | 00000100 | |
| 0x81cd8228: | fpl_lli_os_ctl | bc55bf45 | 0x81cd822c: |
| | fpl_lli_send_word | bc95b5b5 | |
| 0x81cd8230: | fpl_lli_mark_rx | 00000000 | 0x81cd8234: |
| | fpl_lli_rnd_trip_time | 00000000 | |
| 0x81cd8238: | fpl_lli_ns_status | 0a144000 | 0x81cd823c: |
| | fpl_lli_intr_status | 0a000000 | |
| 0x81cd8244: | fpl_lli_def | 00144000 | 0x81cd8254: |
| | fpl_lli_intr_enable_clr | 305e4007 | |
| 0x81cd8258: | fpl_err_intr_status | 00000100 | 0x81cd8260: |
| | fpl_err_intr_enable_clr | 00000000 | |
| 0x81cd8268: | fpl_err_first_error | 00000000 | 0x81cd826c: |
| | fpl_speed_neg_ctl | a404d3b8 | |
| 0x81cd8270: | fpl_speed_neg_stat | 0000005e | 0x81cd8274: |
| | fpl_softasn_ctl | 0000013f | |
| 0x81cd8278: | fpl_link_init_ctl | 00042d40 | 0x81cd827c: |
| | fpl_link_init_stat | 000000e0 | |
| 0x81cd8280: | fpl_aec_ctl | 00181060 | 0x81cd8284: |
| | fpl_aec_ctl2 | 04009f60 | |
| 0x81cd8288: | fpl_pcs_ctl | 00000072 | 0x81cd828c: |
| | fpl_fec_ctl | 00000604 | |
| 0x81cd8290: | fpl_fec_cor | 00000000 | 0x81cd8294: |
| | fpl_fec_uncor | 00000000 | |
| 0x81cd8298: | fpl_hss_link_ctl | 0031f040 | 0x81cd829c: |
| | fpl_afifo_link_ctl | 00000a86 | |
| 0x81cd82a0: | fpl_echo_lb_ctl | 0000028c | 0x81cd82a4: |
| | fpl_scratch | 0000032a | |
| 0x81cd82a8: | fpl_debug | 00050005 | 0x81cd82ac: |
| | fpl_misc_debug | 000007f0 | |
| 0x00000000: | SW_shadow_reg | 30040000 | 0x00000000: |
| | SW_c4_phyp->cfgptr | 00030003 | |

per-fpg (per octet) registers

=====

| | | | |
|-------------|-------------------------|----------|-------------|
| 0x8181b82c: | fpg_serdes_ctla0 | 81a37be7 | 0x8181b830: |
| | fpg_serdes_ctla1 | 81a37be7 | |
| 0x8181b834: | fpg_serdes_ctlb0 | 81a1c3c3 | 0x8181b838: |
| | fpg_serdes_ctlb1 | 81a1c3c3 | |
| 0x8181b83c: | fpg_serdes_xgmii_1ms | 00067c28 | 0x8181b840: |
| | fpg_serdes_regtimctl | 40e47946 | |
| 0x8181b844: | fpg_serdes_asnrsttimctl | 00000102 | |

HSS PLL registers

=====

| | | | |
|-------------|----------------------------|----------|-------------|
| 0x81819400: | 00_hssplla_vco_coarse_cal0 | 00000000 | 0x81819404: |
| | 01_hssplla_vco_coarse_cal1 | 00000014 | |
| 0x81819408: | 02_hssplla_vco_coarse_cal2 | 00000000 | 0x8181940c: |
| | 03_hssplla_vco_coarse_cal3 | 00000000 | |
| 0x81819410: | 04_hssplla_vco_coarse_cal4 | 00000000 | 0x81819424: |
| | 09_hssplla_power_ctl | 00000000 | |

| | | |
|--|----------|-------------|
| 0x81819428: 0A_hssplla_charge_pump_ctl | 00000004 | 0x81819438: |
| 0E_hssplla_pll_misc_ctl | 00000000 | |
| 0x8181943c: 0F_hssplla_pclk_ctl | 000000f8 | 0x81819440: |
| 10_hssplla_eyem_intv_ctl | 00000000 | |
| 0x81819444: 11_hssplla_eyem_intv_lim1 | 00000000 | 0x81819448: |
| 12_hssplla_eyem_intv_lim2 | 00000000 | |
| 0x8181944c: 13_hssplla_eyem_intv_lim3 | 00000000 | 0x81819450: |
| 14_hssplla_eyem_intv_lim4 | 00000000 | |
| 0x818194f0: 3C_hssplla_macro_tst_ctl4 | 00000000 | 0x818194f4: |
| 3D_hssplla_macro_tst_ctl3 | 00000000 | |
| 0x818194f8: 3E_hssplla_macro_tst_ctl2 | 00000000 | 0x818194fc: |
| 3F_hssplla_macro_tst_ctl1 | 00000000 | |
| 0x81819500: 00_hsspllb_vco_coarse_cal0 | 0000000a | 0x81819504: |
| 01_hsspllb_vco_coarse_cal1 | 00000014 | |
| 0x81819508: 02_hsspllb_vco_coarse_cal2 | 00000000 | 0x8181950c: |
| 03_hsspllb_vco_coarse_cal3 | 00000000 | |
| 0x81819510: 04_hsspllb_vco_coarse_cal4 | 00000000 | 0x81819524: |
| 09_hsspllb_power_ctl | 00000000 | |
| 0x81819528: 0A_hsspllb_charge_pump_ctl | 00000004 | 0x81819538: |
| 0E_hsspllb_pll_misc_ctl | 00000000 | |
| 0x8181953c: 0F_hsspllb_pclk_ctl | 000000f8 | 0x81819540: |
| 10_hsspllb_eyem_intv_ctl | 00000000 | |
| 0x81819544: 11_hsspllb_eyem_intv_lim1 | 00000000 | 0x81819548: |
| 12_hsspllb_eyem_intv_lim2 | 00000000 | |
| 0x8181954c: 13_hsspllb_eyem_intv_lim3 | 00000000 | 0x81819550: |
| 14_hsspllb_eyem_intv_lim4 | 00000000 | |
| 0x818195f0: 3C_hsspllb_macro_tst_ctl4 | 00000000 | 0x818195f4: |
| 3D_hsspllb_macro_tst_ctl3 | 00000000 | |
| 0x818195f8: 3E_hsspllb_macro_tst_ctl2 | 00000000 | 0x818195fc: |
| 3F_hsspllb_macro_tst_ctl1 | 00000000 | |

HSS TX registers

=====

| | | |
|--------------------------------------|----------|-------------|
| 0x81818500: 00_hsstx_cfg_mode_PHY | 00009f48 | 0x81818504: |
| 01_hsstx_test_ctl | 00000000 | |
| 0x81818508: 02_hsstx_coeff_ctl_INV | 00000000 | 0x8181850c: |
| 03_hsstx_drv_mode_ctl | 00000000 | |
| 0x81818510: 04_hsstx_drv_ovrd_ctl | 00000010 | 0x81818514: |
| 05_hsstx_dclk_align_ovrd | 00000080 | |
| 0x81818518: 06_hsstx_imp_cal_ovrd | 00000c0c | 0x8181851c: |
| 07_hsstx_dclk_drift_tol | 00000004 | |
| 0x81818520: 08_hsstx_tap0_coeff_TUNE | 00000000 | 0x81818524: |
| 09_hsstx_tap1_coeff_TUNE | 00000003 | |
| 0x81818528: 0A_hsstx_tap2_coeff_TUNE | 00000019 | 0x8181852c: |
| 0B_hsstx_tap3_coeff_TUNE | 00000003 | |
| 0x81818534: 0D_hsstx_pol_INV | 0000000a | 0x81818538: |
| 0E_hsstx_ae_cmd | 00000000 | |
| 0x8181853c: 0F_hsstx_ae_stat | 00000000 | 0x81818540: |
| 10_hsstx_ae_tap0_TUNE | 00000000 | |
| 0x81818544: 11_hsstx_ae_tap1_TUNE | 00000000 | 0x81818548: |
| 12_hsstx_ae_tap2_TUNE | 00000028 | |
| 0x8181854c: 13_hsstx_ae_tap3_TUNE | 00000000 | 0x81818554: |
| 15_hsstx_app_tune | 0000120e | |
| 0x81818558: 16_hsstx_analog_diag | 00000000 | 0x81818560: |

| | | | |
|---|----------|----------|-------------|
| 18_hsstx_4x_seg_app | 0000aa00 | | |
| 0x81818564: 19_hsstx_2x_seg_app | | 000000aa | 0x81818568: |
| 1A_hsstx_1x_seg_app | 0000f5e4 | | |
| 0x8181856c: 1B_hsstx_seg_4x_term_app | | 0000000f | 0x81818570: |
| 1C_hsstx_seg_2x1x_term_app | 00000001 | | |
| 0x81818574: 1D_hsstx_tap_sign_app | | 0000000a | 0x81818578: |
| 1E_hsstx_ext_addr_data | 00000001 | | |
| 0x8181857c: 1F_hsstx_ext_addr_addr | | 00000000 | 0x81818580: |
| 20_hsstx_pat_buf_bytes_1_0 | 00000000 | | |
| 0x81818584: 21_hsstx_pat_buf_bytes_3_2 | | 00000000 | 0x81818588: |
| 22_hsstx_pat_buf_bytes_5_4 | 00000000 | | |
| 0x8181858c: 23_hsstx_pat_buf_bytes_7_6 | | 00000000 | 0x8181859c: |
| 27_hsstx_8023az_ctl | 00000000 | | |
| 0x818185a0: 28_hsstx_dcc_ctl | | 000060c0 | 0x818185a4: |
| 29_hsstx_dcc_ovrd | 00001000 | | |
| 0x818185a8: 2A_hsstx_dcc_app | | 0000010b | 0x818185ac: |
| 2B_hsstx_dcc_timeout | 0000ffff | | |
| 0x818185c0: 30_hsstx_tap_sign_ovrd | | 00000000 | 0x818185c8: |
| 32_hsstx_seg_4x_ovrd | 00000000 | | |
| 0x818185cc: 33_hsstx_seg_2x_ovrd | | 00000000 | 0x818185d0: |
| 34_hsstx_seg_1x_ovrd | 00000000 | | |
| 0x818185d8: 36_hsstx_tap_seg_4x_term_ovrd | | 00000000 | 0x818185dc: |
| 37_hsstx_tap_seg_2x_term_ovrd | 00000000 | | |
| 0x818185e0: 38_hsstx_tap_seg_1x_term_ovrd | | 00000000 | 0x818185ec: |
| 3B_hsstx_mac_test_ctl5 | 00000000 | | |
| 0x818185f0: 3C_hsstx_mac_test_ctl4 | | 00000000 | 0x818185f4: |
| 3D_hsstx_mac_test_ctl3 | 00000000 | | |
| 0x818185f8: 3E_hsstx_mac_test_ctl2 | | 00000000 | 0x818185fc: |
| 3F_hsstx_mac_test_ctl1 | 000000c6 | | |

HSS RX registers

=====

| | | | |
|---------------------------------------|----------|----------|-------------|
| 0x81818700: 00_hssrx_cfg_mode_PHY | | 00009e78 | 0x81818704: |
| 01_hssrx_test_ctl | 00000000 | | |
| 0x81818708: 02_hssrx_phs_rot_ctl | | 0000cb80 | 0x8181870c: |
| 03_hssrx_phs_rot_ofs_ctl | 00004610 | | |
| 0x81818710: 04_hssrx_phs_rot_posn1 | | 00003f37 | 0x81818714: |
| 05_hssrx_phs_rot_posn2 | 00000023 | | |
| 0x81818718: 06_hssrx_phs_rot_sta_ofs1 | | 00000100 | 0x8181871c: |
| 07_hssrx_phs_rot_sta_ofs2 | 0000001f | | |
| 0x81818720: 08_hssrx_dfe_ctl_PHY | | 00002002 | 0x81818724: |
| 09_hssrx_dfe_smpl_snap1 | 00000000 | | |
| 0x81818728: 0A_hssrx_dfe_smpl_snap2 | | 00000000 | 0x8181872c: |
| 0B_hssrx_vga_ctl1 | 000041da | | |
| 0x81818730: 0C_hssrx_vga_ctl2 | | 00007a93 | 0x81818734: |
| 0D_hssrx_vga_ctl3 | 000009e4 | | |
| 0x81818738: 0E_hssrx_pwr_mgmnt_ctl | | 0000001f | 0x8181873c: |
| 0F_hssrx_iqamp_ctl1 | 00000019 | | |
| 0x81818740: 10_hssrx_iqamp_ctl2 | | 00000004 | 0x81818744: |
| 11_hssrx_dacap_dacan_sel | 00000003 | | |
| 0x81818748: 12_hssrx_dacap_dacan | | 00001de2 | 0x8181874c: |
| 13_hssrx_daca_min | 0000000d | | |
| 0x81818750: 14_hssrx_adac_ctl | | 00000000 | 0x81818754: |
| 15_hssrx_ac_cp_ctl | 000031c3 | | |

| | | |
|--|----------------|-------------|
| 0x81818758: 16_hssrx_ac_cp_val | 00008053 | 0x8181875c: |
| 17_hssrx_dfe_h1h2h3_lcl_off_ch | 00000014 | |
| 0x81818760: 18_hssrx_dfe_h1h2h3_lcl_off_val | 0000003f | 0x81818764: |
| 19_hssrx_peaked_intg | 000000ff | |
| 0x81818768: 1A_hssrx_cdr_analog_sw | 0000ce00 | 0x8181876c: |
| 1B_hssrx_peaking_amp_init_c_PHY | 00000000 | |
| 0x81818770: 1C_hssrx_dac_dpc | 00003031 | 0x81818774: |
| 1D_hssrx_ddc | 00002a01 | |
| 0x81818778: 1E_hssrx_int_stat_PHY | 0000ef9f | 0x8181877c: |
| 1F_hssrx_dfe_func_ctl1_PHY | 0000ffff | |
| 0x81818780: 20_hssrx_dfe_func_ctl2_INV | 00007eff | 0x81818784: |
| 21_hssrx_ofs_ch_dcc_qcc_idx | 00002000 | |
| 0x81818788: 22_hssrx_dfe_ofs_val | 00000805 | 0x8181878c: |
| 23_hssrx_h_coeff_bist | 00000401 | |
| 0x81818790: 24_hssrx_ac_cap_bist | 000000b2 | 0x81818794: |
| 25_hssrx_max_gain_path_idx_res | 00007816 | |
| 0x81818798: 26_hssrx_loff_ctl | 00000056 | 0x8181879c: |
| 27_hssrx_sigdet_ctl | 000021a0 | |
| 0x818187a0: 28_hssrx_ana_ctl_sw | 00000000 | 0x818187a4: |
| 29_hssrx_intg_dac_ofs | 0000aee1 | |
| 0x818187a8: 2A_hssrx_eye_ctl | 00003400 | 0x818187ac: |
| 2B_hssrx_eye_met | 00000004 | |
| 0x818187b0: 2C_hssrx_eye_met_err_cnt | 00000000 | 0x818187b4: |
| 2D_hssrx_eye_met_pdf_eyec | 00000000 | |
| 0x818187b8: 2E_hssrx_eye_met_pat_len | 0000007f | 0x818187bc: |
| 2F_hssrx_dfe_func_ctl3 | 0000dfff | |
| 0x818187c0: 30_hssrx_dfe_tap_ctl_idx_ptr | 00000008 | 0x818187c4: |
| 31_hssrx_dfe_tap | 00002515 | |
| 0x818187c8: 32_hssrx_lte_ctl_TUNE | 00000600 | 0x818187e4: |
| 39_hssrx_int_stat2 | 000041ff | |
| 0x818187e8: 3A_hssrx_ac_cpl_cur_src_adj | 00000040 | 0x818187ec: |
| 3B_hssrx_dcd_ctl | 00007c42 | |
| 0x818187f0: 3C_hssrx_dcc_ctl | 00000d41 | 0x818187f4: |
| 3D_hssrx_qcc_ctl | 00006944 | |
| 0x818187f8: 3E_hssrx_mac_test_ctl2 | 00000000 | 0x818187fc: |
| 3F_hssrx_mac_test_ctl1 | 00000000 | |
| 0x81818748: 12_hssrx_dacap_dacan[02] | 20df 1de2 | |
| 0x81818760: 18_hssrx_dfe_h1h2h3_lcl_off_va[00] | 3f3f 3f3d 023e | |
| 3f01 003f 023f 023e 013d | | |
| 0x81818760: 18_hssrx_dfe_h1h2h3_lcl_off_va[08] | 3e00 0100 0101 | |
| 013f 003d 3d02 3f01 013e | | |
| 0x81818760: 18_hssrx_dfe_h1h2h3_lcl_off_va[16] | 023c 013c 0100 | |
| 043f 003f | | |
| 0x81818788: 22_hssrx_dfe_ofs_val[00][00] | 0805 7f7f 7901 | |
| 007f 7f79 0000 | | |
| 0x81818788: 22_hssrx_dfe_ofs_val[03][00] | 0700 7f00 7c04 | |
| 0000 0102 0000 | | |
| 0x81818788: 22_hssrx_dfe_ofs_val[06][00] | 007d 0000 007d | |
| 0000 7e02 0000 | | |
| 0x81818788: 22_hssrx_dfe_ofs_val[09][00] | 0207 7f7f 0202 | |
| 0000 0a7a 0000 | | |
| 0x81818788: 22_hssrx_dfe_ofs_val[12][00] | 7b7a 0000 7d04 | |
| 0000 0003 0000 | | |
| 0x81818788: 22_hssrx_dfe_ofs_val[15][00] | 0979 7f00 0302 | |

```

7f7f 7c03 007f
0x81818788: 22_hssrx_dfe_ofs_val[18][00] 0203 7f00 027a
0000 0004 007f
0x81818788: 22_hssrx_dfe_ofs_val[21][00] 0004 007f 0004
007f 0004 007f
0x81818788: 22_hssrx_dfe_ofs_val[24][00] 7e78 0000 017f
7f00 7d7c 0000
0x81818794: 25_hssrx_max_gain_path_idx_res[00] 0054 083e 1112
18ad 20ef 28a5 308b 3816
0x81818794: 25_hssrx_max_gain_path_idx_res[08] 40bf 488a 5076
580d 6040 6828 70d7 7816
0x818187c4: 31_hssrx_dfe_tap[00] fffe 898a 2626
1100 0022 0024 2630 2513
0x818187c4: 31_hssrx_dfe_tap[08] 2515 1222 1122
0000
0x818187e8: 3A_hssrx_ac_cpl_cur_src_adj[00] 0040 0040 0040
0040
0x818187ec: 3B_hssrx_dcd_ctl[00] 7c42 5c00 7c43
5c00 7c00
0x818187f0: 3C_hssrx_dcc_ctl[00] 0d41 0d84 0d41
0d82
0x818187f4: 3D_hssrx_qcc_ctl[00] 698b 6944

```

xfipcs, fec, aec, & aet registers

=====

```

0x81cd8400: xfipcs_reg [00] 00002040 00000004 00000000
00000000 00000001 00000008 00000000 00000000
0x81cd8420: xfipcs_reg [08] 00008001 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81cd8440: xfipcs_reg [16] 00000000 00000000 00000000
00000000 00000040 00000000 00000000 00000000
0x81cd8460: xfipcs_reg [24] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81cd8480: xfipcs_reg [32] 00001005 00008000 00000000
00000000 00000000 00000000 00000000 00000000
0x81cd8620: fec_32g_128g_reg [08] 00000002 0000c003 00000000
00000000 00000000 00000000 00000000
0x81cd8648: fec_32g_128g_reg [18] 0000000b 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81cd8a00: aec_reg [00] 00000000 0000b000 0000c800
00008000 00000744 0000c510 00000010 00002496
0x81cd8c00: aet_reg [00] 000000b0 00007000 000008c4
00000000 00000009

```

bbc registers

=====

```

0x81cd9800: bbc_trc 255 0 0 0 0 0 0
0
0x81cd9840: bbc_trc 0 0 0 0 0 0 0
0
0x81cd9880: bbc_trc 0 0 0 0 0 0 0
0
0x81cd98c0: bbc_trc 0 0 0 0 0 0 0
0

```

| | | | | | | | |
|---|----------|---|---|---|---|---|----------------------|
| 0x81cd9900: bbc_trc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81cd9804: bbc_mbc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81cd9844: bbc_mbc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81cd9884: bbc_mbc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81cd98c4: bbc_mbc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81cd9904: bbc_mbc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81cd9a00: bbc_rcc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81cd9a20: bbc_rcc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81cd9a40: bbc_rcc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81cd9a60: bbc_rcc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81cd9a80: bbc_rcc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81cd9c00: bbc_rqc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81cd9c20: bbc_rqc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81cd9c40: bbc_rqc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81cd9c60: bbc_rqc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81cd9c80: bbc_rqc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81cd9d00: bbc_fbpc 00000000 | 00000000 | | | | | | 0x81cd9d04: bbc_csc |
| 0x81cd9d08: bbc_rcc_inc bbc_rqc_inc 00000000 | 00000000 | | | | | | 0x81cd9d0c: |
| 0x81cd9d10: bbc_fbpc_inc bbc_tmc_inc 00000000 | 00000000 | | | | | | 0x81cd9d14: |
| 0x81cd9d18: bbc_threshold bbc_counter_clr 00000000 | 00000010 | | | | | | 0x81cd9d1c: |
| 0x81cd9d20: bbc_debug_en 00200120 | 00000000 | | | | | | 0x81cd9d24: bbc_ctrl |
| 0x81cd9d28: bbc_rqc_rcc_thresh bbc_bb_sc_n 00000000 | 00000055 | | | | | | 0x81cd9d34: |
| 0x81cd9d38: bbc_crd_reco_debug bbc_crd_reco_debug_data 00000000 | 00000000 | | | | | | 0x81cd9d3c: |
| 0x81cd9d40: bbc_multi_frm_loss_cnt bbc_multi_rdy_loss_cnt 00000000 | 00000000 | | | | | | 0x81cd9d44: |
| 0x81cd9d48: bbc_1frm_loss_recov_cnt bbc_1rdy_loss_recov_cnt 00000000 | 00000000 | | | | | | 0x81cd9d4c: |
| 0x81cd9d58: bbc_int_status bbc_int_set 00000000 | 00000000 | | | | | | 0x81cd9d5c: |
| 0x81cd9d60: bbc_int_first bbc_frm_rdy_rx_err_addr 00000000 | 00000000 | | | | | | 0x81cd9d64: |

```

0x81cd9d68: bbc_frm_rdy_tx_err_addr 00000000 0x81cd9d6c:
bbc_trc_mbc_err_addr 00000000
0x81cd9d70: bbc_frm_rdy_rx_dbl_ecc 00000000 0x81cd9d74:
bbc_frm_rdy_tx_dbl_ecc 00000000
0x81cd9d78: bbc_trc_mbc_dbl_ecc 00000000
0x81cd9d7c: bbc_fsm_status 00001011 0x81cd9d80:
bbc_force_err 00000000
0x81cd9d84: bbc_crtd_avail0 ffffffff 0x81cd9d88:
bbc_crtd_avail1 000000ff
0x81cd9d8c: bbc_scratch 00000000

```

FPS registers

=====

```

0x81cd8004: fps_er_enc_in 00000000 0x81cd8008:
fps_er_crc 00000000
0x81cd800c: fps_er_trunc 00000000 0x81cd8010:
fps_er_toolong 00000000
0x81cd8014: fps_er_bad_eof 00000000 0x81cd8018:
fps_er_enc_out 00000000
0x81cd801c: fps_er_bad_os 00000000 0x81cd8020:
fps_er_flush 00000000
0x81cd8024: fps_er_ifg 00000000 0x81cd8038:
fps_er_crc_good_eof 00000000
0x81cd803c: fps_inv_arb 00000000 0x81cd8040:
fps_slow_sts_status 00000000
0x81cd8044: fps_tx_frm_cnt 03c07127 0x81cd8048:
fps_rx_frm_cnt 01852bf6
0x81cd8050: fps_tx_word_cnt_hi 00000006 0x81cd804c:
fps_tx_word_cnt_lo f5cdb781
0x81cd8058: fps_rx_word_cnt_hi 00000001 0x81cd8054:
fps_rx_word_cnt_lo ff075b11

```

BAL registers

=====

```

0x81cdf000: bal_desired_buf 00000014 0x81cdf004:
bal_alloc_buf 00000014
0x81cdf008: bal_busy_buf 00000002 0x81cdf00c:
bal_usable_buf 00000014
0x81cdf010: bal_max_bor_buf 00000000
0x81cdf014: bal_busy_buf_thresh 00000002

```

TXQ registers

=====

```

0x81cdb004: txq_phys_port_ctl 00eb0000
0x81cdb050: txq_link_skew 00000000
0x81cdb068: txq_cr_lk_dttm_intr_sts [00] 00000000 00000000
0x81cdb070: txq_cr_lk_dttm_intr_en [00] 00000001 00000000
0x81cdb024: txq_disc_frm_trap_cnt 00000014

```

FDS registers

=====

```

0x81cdc000: fds_rxf_ctl 0000000a 0x81cdc004:
fds_rxf_wait_thresh 00000909
0x81cdc018: fds_rxf_first_error 00000000 0x81cdc01c:

```

```

fds_rxf_first_error_info00000000
0x81cdc020: fds_rxf_inout_pkt_cnt 540b540b
0x81cdc008: fds_rxf_err_int_status 00000000 0x81cdc024:
fds_rxf_fifo_status 0048c888
0x81cdd000: fds_txf_ctl 0000003a 0x81cdd004:
fds_txf_wait_ifg_thresh 00a00106
0x81cdd008: fds_txf_err_int_status 00000000 0x81cdd024:
fds_txf_fifo_status 00088888
0x81cdd02c: fds_txf_bbc_scs 00000000

```

Logical TXQ registers

=====

```

0x81cdb000: txq_log_port_ctl 00000011 0x81cdb008:
txq_port_status 00000000
0x81cdb00c: txq_todo_flags [00] 00000000 00000000
0x81cdb014: txq_spd_match_desc [00] 00000000 395c395c 316b316b
00000000
0x81cdb024: txq_spd_match_desc [04] 00000014
0x81cdb028: txq_vc_weight [00] 25252501 19010125 3c3c3c19
25013c3c
0x81cdb038: txq_vc_weight [04] 01252525 01010101 01010101
01010101
0x81cdb048: txq_vc_weight [08] 01010101 00010101
0x81cdb054: txq_cong_dttm_ctrl 00000106
0x81cdb058: txq_cong_dttm_intr_sts [00] 00000000 00000000
0x81cdb060: txq_cong_dttm_intr_en [00] 00000000 00000000
0x81cdb078: txq_bw_limit_en_reg [00] 00000000 00000000
0x81cdb080: txq_bw_gua_en_reg [00] 00000000 00000000
0x81cdb088: txq_vc_group [00] 03030300 03030303 03030303
03030303
0x81cdb098: txq_vc_group [04] 03030303 03030303 03030303
03030303
0x81cdb0a8: txq_vc_group [08] 03030303 03030303 00000000
00000000
0x81cdb0b0: txq_bw_thresh_group [00] 00000000 00000000 00000000
00000000
0x81cdb0c0: txq_bw_thresh_group [04] 00000000 00000000 00000000
00000000
0x81cdb0d0: txq_bw_thresh_group [08] 00000000 00000000 00000000
00000000
0x81cdb0e0: txq_bw_thresh_group [12] 00000000 00000000 00000000
00000000
0x81cdb0f0: txq_bw_thresh_group [16] 00000000 00000000 00000000
00000000
0x81cdb100: txq_bw_thresh_group [20] 00000000 00000000 00000000
00000000
0x81cdb110: txq_bw_thresh_group [24] 00000000 00000000 00000000
00000000
0x81cdb120: txq_bw_thresh_group [28] 00000000 00000000 00000000
00000000
0x81cdb130: txq_bw_thresh_group [32] 00000000 00000000 00000000
00000000
0x81cdb140: txq_bw_thresh_group [36] 00000000 00000000 00000000
00000000

```

txq Congestion detection Statistics RAM

=====

| | | |
|--------------------|----------|--------------------|
| 0x810910e0: vc[0] | 00000000 | 0x810910e4: vc[1] |
| 00000000 | | |
| 0x810910e8: vc[2] | 00000000 | 0x810910ec: vc[3] |
| 00000000 | | |
| 0x810910f0: vc[4] | 00000000 | 0x810910f4: vc[5] |
| 00000000 | | |
| 0x810910f8: vc[6] | 00000000 | 0x810910fc: vc[7] |
| 00000000 | | |
| 0x81091100: vc[8] | 00000000 | 0x81091104: vc[9] |
| 00000000 | | |
| 0x81091108: vc[10] | 00000000 | 0x8109110c: vc[11] |
| 00000000 | | |
| 0x81091110: vc[12] | 00000000 | 0x81091114: vc[13] |
| 00000000 | | |
| 0x81091118: vc[14] | 00000000 | 0x8109111c: vc[15] |
| 00000000 | | |
| 0x81091120: vc[16] | 00000000 | 0x81091124: vc[17] |
| 00000000 | | |
| 0x81091128: vc[18] | 00000000 | 0x8109112c: vc[19] |
| 00000000 | | |
| 0x81091130: vc[20] | 00000000 | 0x81091134: vc[21] |
| 00000000 | | |
| 0x81091138: vc[22] | 00000000 | 0x8109113c: vc[23] |
| 00000000 | | |
| 0x81091140: vc[24] | 00000000 | 0x81091144: vc[25] |
| 00000000 | | |
| 0x81091148: vc[26] | 00000000 | 0x8109114c: vc[27] |
| 00000000 | | |
| 0x81091150: vc[28] | 00000000 | 0x81091154: vc[29] |
| 00000000 | | |
| 0x81091158: vc[30] | 00000000 | 0x8109115c: vc[31] |
| 00000000 | | |
| 0x81091160: vc[32] | 00000000 | 0x81091164: vc[33] |
| 00000000 | | |
| 0x81091168: vc[34] | 00000000 | 0x8109116c: vc[35] |
| 00000000 | | |
| 0x81091170: vc[36] | 00000000 | 0x81091174: vc[37] |
| 00000000 | | |
| 0x81091178: vc[38] | 00000000 | 0x8109117c: vc[39] |
| 00000000 | | |

Logical STS registers

=====

| | | |
|----------------------------------|----------|-------------|
| 0x815854c4: sts_ftb_type1_miss | 00000000 | |
| 0x815854c8: sts_ftb_type2_miss | 00000000 | |
| 0x815854cc: sts_ftb_type6_miss | 00000000 | |
| 0x815854d0: sts_hard_zoning_miss | 00000000 | |
| 0x815854d4: sts_lun_zoning_miss | 00000000 | |
| 0x815854dc: sts_unroutable | 00000000 | |
| 0x815824f4: sts_rte_cl2 | 00000000 | 0x815824f8: |

```

sts_rte_cl3          01852bf6          0x815824fc: sts_rte_link_ctl
00000000          0x815854e8: sts_tx_timeout          00000000

```

Logical STS filter registers

=====

```

0x81585440: stsflt_trig          [00] 00000000 00000000 00000000
00000000
0x81585450: stsflt_trig          [04] 00000000 00000000 00000000
00000000
0x81585460: stsflt_trig          [08] 00000000 00000000 00000000
00000000
0x81585470: stsflt_trig          [12] 00000000 00000000 00000000
00000000
0x81585480: stsflt_trig          [16] 00000000 00000000 00000000
00000000
0x81585490: stsflt_trig          [20] 00000000 00000000 00000000
00000000
0x815854a0: stsflt_trig          [24] 00000000 00000000 00000000
00000000
0x815854b0: stsflt_trig          [28] 00000000 00000000 00000000
00000000
0x815854c0: stsflt_trig          [32]

```

Logical STS discard registers

=====

```

0x8158373c: disc_mcast_wka          00000000          0x81583740:
disc_inv_did          00000000
0x81583744: disc_cl1_cl4          00000000          0x81583748:
disc_sid_chk_fail    00000000
0x8158374c: disc_inv_dom_egid_txpt 00000000          0x81583750:
disc_vft_hop_cnt_1   00000000
0x81583754: disc_classf          00000000          0x81583758:
disc_fcp_cdb_inv     00000000
0x8158375c: disc_vfid_trap_enabled 00000000          0x81583760:
disc_vfid_hdr_chk_fail 00000000
0x81583764: disc_shim_cksum_fail 00000000          0x81583768:
disc_fed_edit_cmd_err 00000000
0x8158376c: disc_ftb_vm_mode      00000000          0x81583770:
disc_ftb_agnt2_miss  00000000
0x81583774: disc_ecb_reserved     00000000          0x81583778:
disc_ecb_de_pad_err   00000000
0x8158377c: disc_ecb_de_tag_err   00000000          0x81583780:
disc_ecb_de_seq_err   00000000
0x81583784: disc_ecb_err          00000000          0x81583788:
disc_ftb_type4_match  00000000
0x8158378c: disc_fcp_rsp_ftb_type4 00000000          0x81583790:
disc_ftb_type5_match  00000000
0x81583794: disc_ftb_type3_match  00000000          0x81583798:
disc_els_ftb_type3    00000000
0x8158379c: disc_ftb_type1_match  00000000          0x815837a0:
disc_els_rsp_ex_port  00000000
0x815837a4: disc_inv_drp_dps      00000000          0x815837a8:
disc_did_lookup_miss  00000000
0x815837ac: disc_ftb_type2_match  00000000          0x815837b0:

```

```

disc_trpd_plogi_pdisc 00000000
0x815837b4: disc_type2_lookup_miss 00000000 0x815837b8:
disc_ftb_type6_match 00000000
0x815837bc: disc_els_rep_ex_port 00000000 0x815837c0:
disc_els_sid_lkup_bit1 00000000
0x815837c4: disc_els_sid_lkup_bit0 00000000 0x815837c8:
disc_bls_frm_trap_bit1 00000000
0x815837cc: disc_ftb_token_err 00000000 0x815837d0:
disc_asic_internal_err 00000000
0x815837d4: disc_hard_zone_miss 00000000 0x815837d8:
disc_lun_zone_miss 00000000
0x815837dc: discflt_frame_disc 00000000 0x815837e0:
discflt_parity_err 00000000
0x815837e4: disc_frame_marked_du 00000000 0x815837e8:
disc_frame_marked_to 00000000
0x815837ec: disc_lkup_rte_prty_err 00000000

```

portstatsshow 38

```

stat_wtx 29893479670 4-byte words transmitted
stat_wrx 8573556969 4-byte words received
stat_ftx 62943046 Frames transmitted
stat_frx 25504523 Frames received
stat_c2_frx 0 Class 2 frames received
stat_c3_frx 25504758 Class 3 frames received
stat_lc_rx 0 Link control frames
received
stat_mc_rx 0 Multicast frames
received
stat_mc_to 0 Multicast timeouts
stat_mc_tx 0 Multicast frames
transmitted
tim_txcrd_z 0 Time TX Credit Zero
(2.5Us ticks)
tim_txcrd_z_vc 0- 3: 0 0 0 0
tim_txcrd_z_vc 4- 7: 0 0 0 0
tim_txcrd_z_vc 8-11: 0 0 0 0
tim_txcrd_z_vc 12-15: 0 0 0 0
lat_tot_pkt_vc 0- 3: 1 1 1 1
lat_tot_pkt_vc 4- 7: 1 1 1 1
lat_tot_pkt_vc 8-11: 1 1 1 1
lat_tot_pkt_vc 12-15: 1 1 1 1
lat_hi_time_vc 0- 3: 0 0 0 0
lat_hi_time_vc 4- 7: 0 0 0 0
lat_hi_time_vc 8-11: 0 0 0 0
lat_hi_time_vc 12-15: 0 0 0 0
lat_lo_time_vc 0- 3: 1 1 1 1
lat_lo_time_vc 4- 7: 1 1 1 1
lat_lo_time_vc 8-11: 1 1 1 1
lat_lo_time_vc 12-15: 1 1 1 1
max_latency_vc 0- 3: 1 1 1 1
max_latency_vc 4- 7: 1 1 1 1
max_latency_vc 8-11: 1 1 1 1
max_latency_vc 12-15: 1 1 1 1

```



```

latency_dma_ts          09-09-2024 UTC Mon 08:47:24          TXQ
Latency DMA TimeStamp
fec_cor_detected        3896          Count of blocks that
were corrected by FEC
fec_uncor_detected      0          Count of blocks that
were left uncorrected by FEC
er_enc_in               0          Encoding errors inside
of frames
er_crc                  0          Frames with CRC errors
er_trunc                0          Frames shorter than
minimum
er_toolong              0          Frames longer than
maximum
er_bad_eof              0          Frames with bad end-of-
frame
er_enc_out              0          Encoding error outside
of frames
er_bad_os               0          Invalid ordered set
er_pcs_blk              0          PCS block errors
er_rx_c3_timeout        0          Class 3 receive frames
discarded due to timeout
er_tx_c3_timeout        0          Class 3 transmit frames
discarded due to timeout
er_unroutable           0          Frames that are
unroutable
er_unreachable          0          Frame with unreachable
destination
er_other_discard        0          Other discards
er_type1_miss           0          frames with FTB type 1
miss
er_type2_miss           0          frames with FTB type 2
miss
er_type6_miss           0          frames with FTB type 6
miss
er_zone_miss            0          frames with hard zoning
miss
er_lun_zone_miss        0          frames with LUN zoning
miss
er_crc_good_eof         0          Crc error with good eof
er_inv_arb              0          Invalid ARB
er_single_credit_loss   0          Single vcrdy/frame loss
on link
er_multi_credit_loss    0          Multiple vcrdy/frame
loss on link
other_credit_loss       0          Link timeout/complete
credit loss
phy_stats_clear_ts      09-06-2024 UTC Fri 08:30:19      Timestamp of
phy_port stats clear
lgc_stats_clear_ts      09-06-2024 UTC Fri 08:30:19      Timestamp of
lgc_port stats clear
fec_corrected_rate      1.50e-02          FEC Corrected blocks per
second

```

portstats64show 38

| | | |
|------------------------|------------|--|
| stat64_wtx | 6 | top_int : 4-byte words transmitted |
| | 4122143366 | bottom_int : 4-byte words transmitted |
| stat64_wrx | 1 | top_int : 4-byte words received |
| | 4278104305 | bottom_int : 4-byte words received |
| stat64_ftx | 0 | top_int : Frames transmitted |
| | 62939702 | bottom_int : Frames transmitted |
| stat64_frx | 0 | top_int : Frames received |
| | 25502928 | bottom_int : Frames received |
| stat64_c2_frx | 0 | top_int : Class 2 frames received |
| | 0 | bottom_int : Class 2 frames received |
| stat64_c3_frx | 0 | top_int : Class 3 frames received |
| | 25503878 | bottom_int : Class 3 frames received |
| stat64_lc_rx | 0 | top_int : Link control frames received |
| | 0 | bottom_int : Link control frames |
| received | | |
| stat64_mc_rx | 0 | top_int : Multicast frames received |
| | 0 | bottom_int : Multicast frames received |
| stat64_mc_to | 0 | top_int : Multicast timeouts |
| | 0 | bottom_int : Multicast timeouts |
| stat64_mc_tx | 0 | top_int : Multicast frames transmitted |
| | 0 | bottom_int : Multicast frames |
| transmitted | | |
| tim64_rdy_pri | 0 | top_int : Time R_RDY high priority |
| | 0 | bottom_int : Time R_RDY high priority |
| tim64_txcrd_z | 0 | top_int : Time BB_credit zero |
| | 0 | bottom_int : Time BB_credit zero |
| er64_enc_in | 0 | top_int : Encoding errors inside of |
| frames | 0 | bottom_int : Encoding errors inside of |
| frames | | |
| er64_crc | 0 | top_int : Frames with CRC errors |
| | 0 | bottom_int : Frames with CRC errors |
| er64_trunc | 0 | top_int : Frames shorter than minimum |
| | 0 | bottom_int : Frames shorter than minimum |
| er64_toolong | 0 | top_int : Frames longer than maximum |
| | 0 | bottom_int : Frames longer than maximum |
| er64_bad_eof | 0 | top_int : Frames with bad end-of-frame |
| | 0 | bottom_int : Frames with bad end-of- |
| frame | | |
| er64_enc_out | 0 | top_int : Encoding error outside of |
| frames | 0 | bottom_int : Encoding error outside of |
| frames | | |
| er64_disc_c3 | 0 | top_int : Class 3 frames discarded |
| | 0 | bottom_int : Class 3 frames discarded |
| er64_pcs_blk | 0 | top_int : PCS block errors |
| | 0 | bottom_int : PCS block errors |
| stat64_fec_uncor | 0 | top_int : FEC uncorrected errors |
| detected | 0 | bottom_int : FEC uncorrected |
| errors detected | | |
| stat64_rateTxFrame | 2052 | Tx frame rate (fr/sec) |
| stat64_rateRxFrame | 812 | Rx frame rate (fr/sec) |
| stat64_rateTxPeakFrame | 0 | Tx peak frame rate (fr/sec) |

```

stat64_rateRxPeakFrame 0          Rx peak frame rate (fr/sec)
stat64_rateTxWord      974848    Tx Word rate (words/sec)
stat64_rateRxWord      268358    Rx Word rate (words/sec)
stat64_rateTxPeakWord  0          Tx peak Word rate (words/sec)
stat64_rateRxPeakWord  0          Rx peak Word rate (words/sec)
stat64_PRJTFrames      0          top_int : Number of PRJT frames
returned to this port
                                0          bottom_int : Number of PRJT
frames returned to this port
stat64_PBSYFrames      0          top_int : Number of PBSY frames
returned to this port
                                0          bottom_int : Number of PBSY
frames returned to this port
stat64_inputBuffersFull 0          top_int : Number of occurrences
when all input buffers full
                                0          bottom_int : Number of
occurrences when all input buffers full
stat64_rxClass1Frames  0          top_int : Number of class 1
frames received
                                0          bottom_int : Number of class 1
frames received
stat64_aveTxFrameSize  475      Average Tx Frame size
stat64_aveRxFrameSize  330      Average Rx Frame size
Lr_in                  0          top_int
                                1          bottom_int
Ols_in                 0          top_int
                                1          bottom_int
Lr_out                 0          top_int
                                1          bottom_int
Ols_out                0          top_int
                                1          bottom_int
Link_failure           0          top_int
                                1          bottom_int
Invalid_CRC            0          top_int
                                0          bottom_int
Invalid_word           0          top_int
                                0          bottom_int
Protocol_err           0          top_int
                                0          bottom_int
Loss_of_sig            0          top_int
                                0          bottom_int
Loss_of_sync           0          top_int
                                0          bottom_int
er_bad_os              0          top_int : Invalid ordered set
                                0          bottom_int: Invalid ordered set

```

```

portrouteshow 38
port address ID: 0x012600
external unicast routing table:
    0: Embedded
    255: Embedded
internal unicast routing table:

```

portcamshow 38

```
-----  
Port  SID used  DID used  SID entries  DID entries  
38     28         1         040a00      012600  
         040e00  
         040c00  
         012500  
         011900  
         011100  
         011300  
         011500  
         011700  
         041500  
         041700  
         041100  
         041300  
         010c00  
         010a00  
         040b00  
         040900  
         040f00  
         040d00  
         012600  
         011000  
         011200  
         011400  
         041800  
         041400  
         041600  
         041000  
         010b00  
-----
```

SID free, DID free: (59205, 59205)

ptbufshow, ptcreditshow, ptdatashow, ptstatsshow 38

S:

S:VF Enable: 1

S:

S:C4 Global Variable:

S:-----

S:trace_stop: 0

S:

S:C4 Phy Data Pointers: c4_phyp = 0xb6aed140

S:-----

S:tnodep 0xbb84a540 pt
0x4302801b

S:proto_phyp 0xb880b5a0 phy_cfg
0xb6aee180

S:c4_chp 0x97e28000 c4_lgcp
0x97fb4000

S:c4_phy_regp 0x81cd8000 proc_dir
0xb851db40

```

S:-----
-----
S:magic_id          0xc4345678      num_port_timer      12
S:prev_if_id       0x4302001b      S:ftx                0
62943046          tov
S:initialized       1                port_idx             27
S:ui_idx           38                slot_no
0
S:blade_idx        27                sw_usr_ports         400
S:unused           0                intr_debounced
0
S:aec_status       0x1              reason_code
0
S:debug            0x00000004      debug_trc_line       0
S:rxbuf_list_head 0xffffffff      rxbuf_list_tail
0x1bce
S:isAePort         0                port_misc_data
0
S:num_fault1_rx_disc 0                num_fault2_rx_disc  0
S:p_llli_cause0    7                p_sig_regained       0
S:p_sync_regained  7                enc_out
0x0
S:cached_fps_status 0                cached_sts_status    0
S:cached_er_crc_good_eof 0
S:cached_er_bad_os 0                cached_er_too_long   0
S:cached_er_trunc  0
cached_tot_er_crc_good_eof 0
S:num_pt_excess_intr 0                num_no_fid           0
S:num_fault1_cnt   0                num_fault2_cnt
0
S:num_fault_lip    0                num_fault_llli       0
S:num_fault_rx_fifo 0                num_fault_hss        0
S:num_fault_bwait  0                lli_intr_prim
0
S:num_sw_link_to   0
be_link_err_mon_count 0
S:ecb_enc_enabled  0                ecb_comp_enabled
0
S:ecb_rsv_enc      0                ecb_rsv_comp         0
S:ecb_enc_bm       0x0              ecb_key_index
0xffffffff
S:fab_idx          0
S:num_be_lto       0                lto_count_reset_intvl
0
S:lr_count_reset_intvl 0                num_be_lr
0
S:num_fault_qsfps  0                check_lto
0
S:credit_loaded    255              num_credit_overrun
0
S:fec_enabled      0x1              fec_los_to_flag      0x1
S:phy_stats_clear_ts 1725611419      pcs_err_online
0
S:pcs_err_light_det 0                pcs_err_ignore

```

```

      0
S:pcs_blk_err          0          pcs_hiber          0
S:phy_port_status     2          ecb_enc_lr_count
      0

S:dport_mode          0          avoid_lto_det     0
S:sn_debounced        0x0       sn_started_kr_reqd 1
S:major_timer_started 0x0       ready_bm          0x0
S:parln_1_bm          0x0       parln_0_bm        0x0
S:be_los_of_sync_event_intvl
be_los_of_sync_event  0
S:errataPtenable_cntr 0          errataPoll_cntr
      0
S:jda_rx_sig_loss_det 0          jda_rx_sig_loss_cnt
      0

S:encrypt_blk_error   0
S:
S:      c4_trunk
S:=====
S:mark_ts              0x0       deskew            0x0
S:master_phyp          0x0
S:
S:adelay[00]: 0x00000000 0x00000000 0x00000000 0x00000000
S:adelay[04]: 0x00000000 0x00000000 0x00000000 0x00000000
S:
S:      c4_buf
S:=====
S:tx_csc                0          rx_csc
      0
S:ld_vc_credits         0          tx_flag           0x0
S:alloc_buffers        20         req_buffers       20
S:est_buffers           20         ld_use_est        0
S:bb_sc_n               0          rx_bb_sc_n
      0
S:data_cr               16         nondata_cr
      6
S:cr_enable             0
S:ld_nondata_cr         6          tnodep
0xbb84a620
S:tx_credits[0] 0 0 0 0 0 0 0 0
S:tx_credits[8] 0 0 0 0 0 0 0 0
S:tx_credits[16] 0 0 0 0 0 0 0 0 0 0
S:tx_credits[24] 0 0 0 0 0 0 0 0 0 0
S:tx_credits[32] 0 0 0 0 0 0 0 0 0 0
S:rx_credits[0] 0 0 0 0 0 0 0 0
S:rx_credits[8] 0 0 0 0 0 0 0 0
S:rx_credits[16] 0 0 0 0 0 0 0 0 0 0
S:rx_credits[24] 0 0 0 0 0 0 0 0 0 0
S:rx_credits[32] 0 0 0 0 0 0 0 0 0 0
S:tx_mbc[0] 0 0 0 0 0 0 0 0
S:tx_mbc[8] 0 0 0 0 0 0 0 0
S:tx_mbc[16] 0 0 0 0 0 0 0 0
S:tx_mbc[24] 0 0 0 0 0 0 0 0
S:tx_mbc[32] 0 0 0 0 0 0 0 0
S:rx_mbc[0] 0 0 0 0 0 0 0 0

```

S:rx_mbc[8] 0 0 0 0 0 0 0 0
S:rx_mbc[16] 0 0 0 0 0 0 0 0
S:rx_mbc[24] 0 0 0 0 0 0 0 0
S:rx_mbc[32] 0 0 0 0 0 0 0 0

S:

S:C4 Chip Variables: c4_phyp->c4_chp = 0x97e28000

S:-----

S:version = 2.1

S:magic_id 0xc4234567 init_state 0x8

S:reset_reg_mem 0x1

S:ch_int0_en_bm 0x0 intr0_cause 0x0

S:ch_int1_en_bm 0x0 intr1_cause 0x0

S:ch_int2_en_bm 0x0 intr2_cause 0x0

S:ch 0x43010080 ch_cfg

0xb7013ba0

S:raslog_hndl.hndl 0x0 obj_halted 0x0

S:c4_chip_regp 0x80000000 c4_fpg_regp

0x81800000

S:num_chip_timer 0x5

S:hi_task_bm 0x0 lo_task_bm 0x0

S:c4_deferq.q_head 0x0 c4_deferq.q_tail 0x0

S:c4_tmrq.q_head 0x0 c4_tmrq.q_tail 0x0

slot_no 0

S:chip_inst 0 chip_idx 0

S:pll_initialized 1

pll_serdes_initialized 1

S:init_tries 0 init_ptEnableBM

0xba01b488

S:tick_polling 0xb980c9c0 sec_polling

0xb980c960

S:bb_fid 129

S:ecb_key_bm[0] 0x0 ecb_key_bm[1] 0x0

S:ecb_key_bm[2] 0x0 ecb_key_bm[3] 0x0

S:is_chip_enc_enabled 0

is_chip_comp_enabled 0x0

S:ftb_rsrcp->ftb_flags 0x0 act_rsrcp->act_flag 0x1

S:lue_rsrcp->lue_flags[0] 0x0 lue_rsrcp-

>lue_flags[1] 0x0

S:c4_phyp[00]: 0xb6ab0000 0xb6ab2080 0xb6ab4100 0xb6ab6180

S:c4_phyp[04]: 0xb6ab9040 0xb6abb0c0 0xb6abd140 0xb6ac0000

S:c4_phyp[08]: 0xb6ac2080 0xb6ac4100 0xb6ac6180 0xb6ac9040

S:c4_phyp[12]: 0xb6acb0c0 0xb6acd140 0xb6ad0000 0xb6ad2080

S:c4_phyp[16]: 0xb6ad4100 0xb6ad6180 0xb6ad9040 0xb6adb0c0

S:c4_phyp[20]: 0xb6add140 0xb6ae0000 0xb6ae2080 0xb6ae4100

S:c4_phyp[24]: 0xb6ae6180 0xb6ae9040 0xb6aeb0c0 0xb6aed140

S:c4_phyp[28]: 0xb6af0000 0xb6af2080 0xb6af4100 0xb6af6180

S:c4_phyp[32]: 0xb6af9040 0xb6afb0c0 0xb6afd140 0xb6b00000

S:c4_phyp[36]: 0xb6b02080 0xb6b04100 0xb6b06180 0xb6b09040

S:c4_phyp[40]: 0xb6b0b0c0 0xb6b0d140 0xb6b10000 0xb6b12080

S:c4_phyp[44]: 0xb6b14100 0xb6b16180 0xb6b19040 0xb6b1b0c0

S:c4_phyp[48]: 0xb6b1d140 0xb6b20000 0xb6b22080 0xb6b24100

S:c4_phyp[52]: 0xb6b26180 0xb6b29040 0xb6b2b0c0 0xb6b2d140

S:c4_phyp[56]: 0xb6b30000 0xb6b32080 0xb6b34100 0xb6b36180

```

S:c4_phyp[60]: 0xb6b39040 0xb6b3b0c0 0xb6b3d140 0xb6b40000
S:c4_lgcp[00]: 0x97f48000 0x97f4c000 0x97f50000 0x97f54000
S:c4_lgcp[04]: 0x97f58000 0x97f5c000 0x97f60000 0x97f64000
S:c4_lgcp[08]: 0x97f68000 0x97f6c000 0x97f70000 0x97f74000
S:c4_lgcp[12]: 0x97f78000 0x97f7c000 0x97f80000 0x97f84000
S:c4_lgcp[16]: 0x97f88000 0x97f8c000 0x97f90000 0x97f94000
S:c4_lgcp[20]: 0x97f98000 0x97f9c000 0x97fa0000 0x97fa4000
S:c4_lgcp[24]: 0x97fa8000 0x97fac000 0x97fb0000 0x97fb4000
S:c4_lgcp[28]: 0x97fb8000 0x97fbc000 0x97fc0000 0x97fc4000
S:c4_lgcp[32]: 0x97fc8000 0x97fcc000 0x97fd0000 0x97fd4000
S:c4_lgcp[36]: 0x97fd8000 0x97fdc000 0x97fe0000 0x97fe4000
S:c4_lgcp[40]: 0x97fe8000 0x97fec000 0x97ff0000 0x97ff4000
S:c4_lgcp[44]: 0x97ff8000 0x97ffc000 0x8e000000 0x8e004000
S:c4_lgcp[48]: 0x8e008000 0x8e00c000 0x8e010000 0x8e014000
S:c4_lgcp[52]: 0x8e018000 0x8e01c000 0x8e020000 0x8e024000
S:c4_lgcp[56]: 0x8e028000 0x8e02c000 0x8e030000 0x8e034000
S:c4_lgcp[60]: 0x8e038000 0x8e03c000 0x8e040000 0x8e044000
S:chip_timers[00]: 0xb980c720 0xb980c780 0xb980c7e0 0xb980c840
S:chip_timers[04]: 0xb980c8a0 0xb980c900
S:disc_trap_enable_required      0x0                rxlp_disc_log_stop
      0x0
S:curr_rxlp_frm_cnt      0x0                curr_rxlp_disc_frm_cnt  0x0
S:sw_disc_frm_cnt      0x0                last_disc_frm_cnt      0x0
S:txq_nopop_pr_cnt      0x0                pollErrataDfe_ptBM
0xba01b4b0
S:ftb_rsrpc->chip_ref[FTB_REF_CHP_EC][0]      0x0
ftb_rsrpc->chip_ref[FTB_REF_CHP_EC][1] 0x0
S:ftb_rsrpc->chip_ref[FTB_REF_CHP_EC][2]      0x0
ftb_rsrpc->chip_ref[FTB_REF_CHP_NRC][0] 0x0
S:ftb_rsrpc->chip_ref[FTB_REF_CHP_NRC][1]      0x0
ftb_rsrpc->chip_ref[FTB_REF_CHP_NRC][2] 0x0
S:
S:C4 Logical Port Variables
S:-----
-----
S:c4_lgc_regp      0x81cd8000
S:c4_phyp:
S:      0xb6aed140      0x0                0x0                0x0

S:      0x0                0x0                0x0                0x0

S:master_phyp      0xb6aed140      if_id
0x4302001b
S:min_phyp      0x0                max_phyp      0x0
S:num_phy_ports      1                lgc_num      27
S:num_iu_to      0                sw_txq_bm
0
S:port_fid      128                unused      0
S:port_group      3                lgc_stats_clear_ts
1725611419
S:domain_tbl_sel      91                area_tbl_sel
27
S:egid_tbl_sel      2
S:serv_lo_bm      0x0

```



```

S:
S:Proto Phy Variables:
S:-----
-----
S:magic_id          0xc4123456      asic_phyp
0xb6aed140
S:port_id           0x4302801b      phy_cfg
0xb6aee180
S:upsm_hdl         0xb8018960      physm_hdl
0xb80186e0
S:ov_snsn_hdl      0xb80185a0      sw_snsn_hdl
0xb8018640
S:ov_lksm_hdl      0xb8018780      sw_lksm_hdl
0xb8018820
S:trksm_hdl        0xb80188c0      lr_flag          0x0
S:lr_active        0x0             qsfm_txxr_rate_sel
0x0

S:
S:UPSM            UP22: UPST_G_PORT      --> UP23: UPST_F_PORT
S:SNSM(OV)        SN06: OV_SNST_HW_LK_TRAIN --> SN04: OV_SNST_NEGOTIATED
S:SNSM(SW)        SW00: SW_SNST_STAGE_WS  --> SW00: SW_SNST_STAGE_WS
S:PHYSM           PP04: PHYST_NO_SYNC    --> PP05: PHYST_IN_SYNC
S:LKSM(OV)        LK02: OV_LKST_HW_INIT  --> LK04: OV_LKST_ACTIVE
S:LKSM(SW)        SW13: INACTIVE        --> SW13: INACTIVE
S:TRKSM           TRK0: TRKST_INIT      --> TRK0: TRKST_INIT
S:
S:physm variables:
S:-----
-----
S:proto_phy        0xb880b5a0      physm_hdl
0xb80186e0
S:force_offline    0               copper            0
S:fault_reason     0: UNKNOWN
S:phy_media_present 1
S:
S:snsn variables:
S:-----
-----
S:speed           0xa             proto_phy
0xb880b5a0
S:hw_sn_tries_left 0x63            sw_sn_tries_left 0x0
S:curr_txsp_count  0x0
S:tx_max          0x0             curr_tx_indx
0x0
S:curr_tx         0x0             curr_rxsp_count
0x0
S:rx_max         0x0             curr_rx_indx
0x0
S:curr_rx         0x0             rx_mem
0x0
S:rxsp_rec_count  0x0
S:nc_start        0x0             tx_start          0x0
S:sync_start      0x0             sync_present      0x0
S:diag_auto       0x0             diag_speed        0xff

```

```

S:striped_wd_tov          3000          hw_wd_tov
   3000
S:step                    0x0          qsfp28_speed_mode
   0x0
S:qsfp_mode0_hw_sn_tries_left  0x0
S:qsfp_mode1_hw_sn_tries_left  0x0
S:
S:lksm variables:
S:-----
-----
S:proto_phyph            0xb880b5a0    ov_lksm_hdl
0xb8018780
sw_lksm_hdl              0xb8018820
num_lf1                  0
S:hw_link_tries_left    9          sw_link_tries_left    5
S:buf_ptype              0x0          stored_entry_state    0x5
S:handshake_owner       0x0          mark_unsent
   0x0
S:busybuf_stuck         0x0          lr_wait                0x0
S:
S:trksm variables:
S:-----
-----
S:Not a trunk port
S:
S:upsm variables:
S:-----
-----
S:proto_phyph            0xb880b5a0    upsm_hdl
0xb8018960
S:bb_credits             255          port_beacon            0
S:port_diag_flag        0          force_offline
   0
S:port_fault_rsn        0: PORT_NO_FAULT
S:retry_init_rsn        0: UNKNOWN
S:linit_reason           0          linit_result           0
S:ie_fctl_mode           0          fec_in_sync_tries_left 0
S:retry_sn_fail_init    0
retry_link_fail_init    0
S:excess_lr_count       0
S:
S:c4_ch_cfg
S:-----
-----
S:c4_desc_ring_size     256          292          256          256          292
292          2          292          292
S:thresh_def            0          16          1          0
S:intr_tries            500          cmem_pattern
0xdeadbeef
S:cmem_pattern_upwd     2          cmem_init_time        16
S:cmem_init_tries      5
S:ctrl_par_thresh      2          data_par_thresh
4
S:cam_par_thresh        4          buf_loss_thresh

```

```

12
S:crit_par_thresh          2          non_crit_par_thresh
6
S:pci_abort_thresh        10          pci_err_thresh          5
S:excess_chintr_thresh    8          sw_err_thresh           20
S:err_sample_period       300        intr_sleep
20000
S:frame_timeout           2500        proxy_dev               16384
S:vf_route                 81920       qos                     2048
S:stats 2048              f_redirect   2048
S:rsp_trap                 2048        lun_zoning              20480
S:area_mode                0          ftb_max_loop[0]        0
S:ftb_max_loop[1]         6          ftb_max_loop[2]        9
S:ftb_max_loop[3]        10         ftb_max_loop[4]        10
S:ftb_max_loop[5]         5          ftb_max_loop[6]        6
S:ftb_seg_size[0]         0          ftb_seg_size[1]
16384
S:ftb_seg_size[2]         65536      ftb_seg_size[3]
16384
S:ftb_seg_size[4]         16384      ftb_seg_size[5]
65536
S:ftb_seg_size[6]         16384      ftb_seg_base[0]        0
S:ftb_seg_base[1]         0          ftb_seg_base[2]
65536
S:ftb_seg_base[3]         16384      ftb_seg_base[4]
32768
S:ftb_seg_base[5]         131072     ftb_seg_base[6]
49152
asic_err_monitor_period1  300
asic_err_monitor_period2 86400
zone_chk_to_poll_period  25
zone_chk_class2_reject_tov 220
S:
S:c4_phy_cfg
S:-----
-----
S:version = 2.1
S:pt                       0x4302801b    fab_ptr
0x9a800000
S:fabattr                  0x9a8000d4    fab_iop
0x9a800050
S:cfgbm                   0xbb84a384    port_ctrl
0xb6aee198
S:pcap.pcap_bm            0x8d215547    pcap.pcap2_bm
0x588289
S:pcap.pcap3_bm          0x1bebe0c
ui_idx                     38           S:slot_no
0
is_icl                     0           S:sw_usr_ports         400
S:neg_speed               10 8 5 0 0 0
S:my_domain               0x1          port_mode               0x0
S:hw_sn_maxtries          100         sw_sn_maxtries
0
S:hw_link_maxtries        10          sw_link_maxtries       5

```

```

S:rx_cyc_tov          28          rttov          300
S:bufrdy_tov         300         busybuf_tov    286
S:mark_tov           300         lksm_tov       3000
S:buf_dealloc_wait   4          hw_wd_tov      3000
S:hw_lk_train_tov    540        hw_lk_test_tov
    150
S:syswait_tx_12_lips 1          lip_rx_tov     55
S:al_time_tov        15         lp_tov         2000
S:intr_tries_port    500        intr_mod_debounce
    250
S:intr_lsrflt_debounce 500       intr_efifo_debounce 100
S:port_no_fid        3          excess_ptintr_thresh 8
S:port_fault1_thresh 100        port_fault1_spur_thresh 250
S:port_fault1_disc_thresh 500      losync_tov     100
port_fault1_disc_spur_thresh 1000
S:port_fault2_thresh 5          en_8g_scramble
S:port_sw_link_to    15
    1
frc_hw_sn_mode       0x1
S:enc_poll_thresh    0          fec_enable
    0
S:fec_in_sync_to     50         fec_in_sync_try_max
    4
S:port_be_lto_threshold 100       port_be_lr_threshold
    2
S:be_cr_in_sync_to   5
port_credit_overrun_thresh 10
S:jda_sfp_losig_tov  400
jda_sfp_losig_try_max 30
S:striped_wd_tov     3000
no_sync_debounce     1200
S:
S:    fab_iop
S:=====
S:fab_iop->interop_mode 0x0    fab_iop->lab_mode    0x0
S:fab_iop->fl_bbc        0x0    fab_iop->fl_fan
    0x0
S:fab_iop->fl_cls        0x4    fab_iop->fl_rscn
    0x0
S:fab_iop->domain_id_offset 0x60    fab_iop-
>mcdt_fabric_mode      0x0
S:fab_iop->mcdt_default_zone 0x0    fab_iop-
>mcdt_safe_zone        0x0
S:
S:    port_ctrl
S:=====
S:port_ctrl.port_type  1          port_ctrl.port_grp  3
S:port_ctrl.port_number 38       port_ctrl.vc_mode   1
S:
S:    port_ctrl.lcap
S:=====
S:has_serdes          0          has_media        1
S:topology            1          skip_nego        0
S:skip_pnego          0          skip_init_event   0

```

```

S:en_shim          0          speed_neg
    1
S:loop_back        0          num_speeds          5
S:fec_enable       0
S:
S:    port_ctrl.speed_list array
S:=====
S:speed_list[0].auto_neg  1    speed_list[0].lnk_speed  0x0000000a
S:speed_list[1].auto_neg  1    speed_list[1].lnk_speed  0x00000008
S:speed_list[2].auto_neg  0    speed_list[2].lnk_speed  0x00000006
S:speed_list[3].auto_neg  1    speed_list[3].lnk_speed  0x00000005
S:speed_list[4].auto_neg  0    speed_list[4].lnk_speed  0x00000003
S:speed_list[5].auto_neg  0    speed_list[5].lnk_speed  0x00000000
S:
S:    port_ctrl.cm
S:=====
S:port_ctrl.cm.num_vcs          8
S:port_ctrl.cm.min_bufs        20
S:port_ctrl.cm.cr_shar_bufs    0
S:port_ctrl.vc_alloc
S:port_ctrl.vc_alloc          2 0 4 4 4 4 1 1
S:port_ctrl.vc_alloc          0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.norm_vc_alloc
S:port_ctrl.norm_vc_alloc      4 0 16 16 16 16 1 1
S:port_ctrl.norm_vc_alloc      0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.cm.skip_bb_credit  0
S:port_ctrl.cm.use_shim_based_sublist  0
S:
S:    port_ctrl.serdes_set
S:=====
S:serdes_type          0x8
S:serdes_data_t.ibm_hss_serdes.tx_drive_power          0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b_sign     0x1
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b          0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_a          0x0
S:serdes_data_t.ibm_hss_serdes.rxeq                    0x0
S:
S:    cfgbm
S:=====
S:old_distance          0x0          gport_lockdown          0x0
S:tport                0x1          speed                    0x0
S:disable_eport        0x0          fcacc                    0x0
S:lport_lockdown       0x0          priv_lport_lockdown     0x0
0x0
S:vcxlt_linit          0x0          delay_flogi             0x0
S:isl_interop          0x0          distance                 0x0
S:BufStarvFlag         0x0          credit_sharing           0x0
S:lport_halfduplex     0x0          lport_fairness           0x0
S:soft_neg             0x0          asn_frc_hwretry         0x0
S:cr_recov             0x0          fport_buffers            0x0
S:export               0x0          export_mode              0x0
0x0

```

S:csctl_en 0x0 mirror_port 0x0
S:fault_delay 0x0 non_dfe 0x0
S:fec_configured*(0=ENAB) 0 fec_tts
0

S:port_persistently_disabled (permanently) 0 (0)

S:

S: cfg property

S:=====

S:priv_pcfg_bm 0x00000000 lgcl_pcfg_bm
0xbb84a3c4

S:fport_buffer 0x00000000

S:

S:

S:C4 Discard Cntrs: rxlp_stats = 0xb6aed4f0

S:-----

S:disc_mcast_wka 0x0 disc_inv_did 0x0

S:disc_cl1_cl4 0x0 disc_sid_chk_fail 0x0

S:disc_inv_dom_egid_txpt 0x0 disc_vft_hop_cnt_1
0x0

S:disc_classf 0x0 disc_fcp_cdb_inv 0x0

S:disc_vfid_trap_enabled 0x0

disc_vfid_hdr_chk_fail 0x0

S:disc_shim_cksum_fail 0x0 disc_fed_edit_cmd_err 0x0

S:disc_shim_cksum_fail 0x0 disc_fed_edit_cmd_err 0x0

S:disc_ftb_vm_mode 0x0 disc_ftb_agnt2_miss 0x0

S:disc_ecb_de_pad_err 0x0 disc_ecb_de_tag_err 0x0

S:disc_ecb_de_seq_err 0x0 disc_ecb_err 0x0

S:disc_ftb_type4_match 0x0 disc_fcp_rsp_ftb_type4 0x0

S:disc_fcp_rsp_ftb_type4 0x0 disc_ftb_type5_match
0x0

S:disc_ftb_type3_match 0x0 disc_els_ftb_type3 0x0

S:disc_ftb_type1_match 0x0 disc_els_rsp_ex_port 0x0

S:disc_inv_drp_dps 0x0 disc_did_lookup_miss 0x0

S:disc_ftb_type2_match 0x0 disc_trpd_plogi_pdisc 0x0

S:disc_type2_lookup_miss 0x0 disc_ftb_type6_match
0x0

S:disc_els_rep_ex_port 0x0 disc_els_sid_lkup_bit1 0x0

S:disc_els_sid_lkup_bit0 0x0

disc_bls_frm_trap_bit1 0x0

S:disc_ftb_token_err 0x0 disc_asic_internal_err 0x0

S:disc_hard_zone_miss 0x0 disc_lun_zone_miss 0x0

S:discflt_frame_disc 0x0 discflt_parity_err 0x0

S:disc_frame_marked_du 0x0 disc_frame_marked_to 0x0

E:Connection type: FE

E:Port type: F_port

E:Trunk port: No

E:Configured Speed: AUTO_SPEED_NEGO

E:Max Capable Speed: 32G

E:Current SNSM Speed: 32G

E:Hardware TX Speed: 32G (0x00000004)

E:Hardware RX Speed: 32G (0x00000040)

E:

E:Interrupts: 9 Link_failure: 1

| | | | |
|-------------------|-----|------------------|-----|
| Loss_of_sync: | 0 | Loss_of_sig: | 0 |
| E:Lli: | 9 | Invalid_word: | 0 |
| E:trapped_frm: | 103 | fwd_status_ok: | 103 |
| E:fwd_timeout: | 0 | fwd_tx_unavail: | 0 |
| E:fwd_unroutable: | 0 | fwd_zone_out: | 0 |
| E:fwd_other_err: | 0 | frm_err_discard: | 0 |
| E:Fltr listA: | 0 | Fltr listB: | 0 |
| E:Zone trap fwd: | 0 | Zone trap disc: | 0 |
| E:shim_csum: | 0 | RTE_perr: | 0 |
| E:Invalid_crc: | 0 | Delim_err: | 0 |
| E:Protocol_err: | 0 | | |
| E:Lr_in: | 1 | Lr_out: | 1 |
| E:Ols_in: | 1 | Ols_out: | 1 |

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FILTER DATA

Shadow settings:

```

Filter Enable: 0x00000420
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass: 0x00000019

```

Real settings:

Enable RAM: 0x00000420, 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass RAM: 0x00000019

Shadowed filters:

Filter 0: Not Installed (MIRROR1)(LISTA)

c4_fldenable[0] = 0x00000000 0x00000000 0x00000000
0x00000000

c4_fldnegate[0] = 0x00000000, c4_fltr_config[0] = 0x00000000

Filter 1: Not Installed (MIRROR2)(LISTA)

c4_fldenable[1] = 0x00000000 0x00000000 0x00000000
0x00000000

c4_fldnegate[1] = 0x00000000, c4_fltr_config[1] = 0x00000000

Filter 2: Not Installed (MIRROR3)(LISTA)

c4_fldenable[2] = 0x00000000 0x00000000 0x00000000
0x00000000

c4_fldnegate[2] = 0x00000000, c4_fltr_config[2] = 0x00000000

Filter 3: Not Installed (MIRROR4)(LISTA)

c4_fldenable[3] = 0x00000000 0x00000000 0x00000000
0x00000000

c4_fldnegate[3] = 0x00000000, c4_fltr_config[3] = 0x00000000

Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
c4_fldenable[4] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[4] = 0x00000000,c4_fltr_config[4] = 0x00000000

Filter 5: Installed (ZONING TRAP)(LISTA)
c4_fldenable[5] = 0x00000000 0x00000000 0x00000000
0x06007c10
c4_fldnegate[5] = 0xfd9ffffff,c4_fltr_config[5] = 0x000001c0

Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
c4_fldenable[6] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[6] = 0x00000000,c4_fltr_config[6] = 0x00000000

Filter 7: Not Installed (TIN TRAP)(LISTA)
c4_fldenable[7] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[7] = 0x00000000,c4_fltr_config[7] = 0x00000000

Filter 8: Not Installed (FICON CUP)(LISTA)
c4_fldenable[8] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[8] = 0x00000000,c4_fltr_config[8] = 0x00000000

Filter 9: Not Installed (FICON CUP DST)(LISTA)
c4_fldenable[9] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[9] = 0x00000000,c4_fltr_config[9] = 0x00000000

Filter 10: Installed (WELL KNOWN ADDR)(FORWARD)
c4_fldenable[10] = 0x00000001 0x00000000 0x00000000
0x00000000
c4_fldnegate[10] = 0xffffffff,c4_fltr_config[10] =
0x00000054

Filter 11: Not Installed (SIM)(LISTA)
c4_fldenable[11] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[11] = 0x00000000,c4_fltr_config[11] =
0x00000000

Filter 12: Not Installed (UNUSED)(LISTA)
c4_fldenable[12] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[12] = 0x00000000,c4_fltr_config[12] =
0x00000000

Filter 13: Not Installed (UNUSED)(LISTA)
c4_fldenable[13] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[13] = 0x00000000,c4_fltr_config[13] =
0x00000000

Filter 14: Not Installed (UNUSED)(LISTA)
c4_fldenable[14] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[14] = 0x00000000,c4_fltr_config[14] =
0x00000000

Filter 15: Not Installed (UNUSED)(LISTA)
c4_fldenable[15] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[15] = 0x00000000,c4_fltr_config[15] =
0x00000000

Filter 16: Not Installed (PERF1)(LISTA)
c4_fldenable[16] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[16] = 0x00000000,c4_fltr_config[16] =
0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
c4_fldenable[17] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[17] = 0x00000000,c4_fltr_config[17] =
0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
c4_fldenable[18] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[18] = 0x00000000,c4_fltr_config[18] =
0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
c4_fldenable[19] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[19] = 0x00000000,c4_fltr_config[19] =
0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
c4_fldenable[20] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[20] = 0x00000000,c4_fltr_config[20] =
0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
c4_fldenable[21] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[21] = 0x00000000,c4_fltr_config[21] =
0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
c4_fldenable[22] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[22] = 0x00000000,c4_fltr_config[22] =
0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
c4_fldenable[23] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[23] = 0x00000000,c4_fltr_config[23] =
0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
c4_fldenable[24] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[24] = 0x00000000,c4_fltr_config[24] =
0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
c4_fldenable[25] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[25] = 0x00000000,c4_fltr_config[25] =
0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
c4_fldenable[26] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[26] = 0x00000000,c4_fltr_config[26] =

```
0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
    c4_fldenable[27] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[27] = 0x00000000,c4_fltr_config[27] =
0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
    c4_fldenable[28] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[28] = 0x00000000,c4_fltr_config[28] =
0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
    c4_fldenable[29] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[29] = 0x00000000,c4_fltr_config[29] =
0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    c4_fldenable[30] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[30] = 0x00000000,c4_fltr_config[30] =
0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    c4_fldenable[31] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[31] = 0x00000000,c4_fltr_config[31] =
0x00000000
```

Real filters:

```
Filter 0: Not Installed (MIRROR1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x000e0000
Filter 5: Installed (ZONING TRAP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x06007c10,
    fld negate ram = 0x019fffff, fltr config ram = 0x000e0000
```

Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 7: Not Installed (TIN TRAP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 8: Not Installed (FICON CUP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 9: Not Installed (FICON CUP DST)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 10: Installed (WELL KNOWN ADDR)(FORWARD)
fld enable ram = 0x00000001, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x03ffffffe, fltr config ram = 0x00000054

Filter 11: Not Installed (SIM)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000054

Filter 12: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 13: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 14: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 15: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 16: Not Installed (PERF1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 17: Not Installed (PERF2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 18: Not Installed (PERF3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 19: Not Installed (PERF4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,

```
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
```

```
Filter dirty indicator: 0x00000000
Performance filters: 0
Port Mirror filters: 0 (0x0)
```

FIELD DATA

Shadowed fields:

```
fldoffset[0] = 0x05, fldmask[0] = 0x00, fldvalue_dyna[0]:0xff 0x00
0x00 0x00
fldcontrol[0].inuse = 0x1000000 fldcontrol[0].refcnt = 0x01 0x00
0x00 0x00
fldoffset[1] = 0x00, fldmask[1] = 0x00, fldvalue_dyna[1]:0x00 0x00
0x00 0x00
fldcontrol[1].inuse = 0x0 fldcontrol[1].refcnt = 0x00 0x00 0x00
0x00
fldoffset[2] = 0x00, fldmask[2] = 0x00, fldvalue_dyna[2]:0x00 0x00
0x00 0x00
fldcontrol[2].inuse = 0x0 fldcontrol[2].refcnt = 0x00 0x00 0x00
0x00
fldoffset[3] = 0x00, fldmask[3] = 0x00, fldvalue_dyna[3]:0x00 0x00
0x00 0x00
fldcontrol[3].inuse = 0x0 fldcontrol[3].refcnt = 0x00 0x00 0x00
0x00
fldoffset[4] = 0x00, fldmask[4] = 0x00, fldvalue_dyna[4]:0x00 0x00
0x00 0x00
fldcontrol[4].inuse = 0x0 fldcontrol[4].refcnt = 0x00 0x00 0x00
0x00
fldoffset[5] = 0x00, fldmask[5] = 0x00, fldvalue_dyna[5]:0x00 0x00
0x00 0x00
fldcontrol[5].inuse = 0x0 fldcontrol[5].refcnt = 0x00 0x00 0x00
0x00
fldoffset[6] = 0x00, fldmask[6] = 0x00, fldvalue_dyna[6]:0x00 0x00
0x00 0x00
fldcontrol[6].inuse = 0x0 fldcontrol[6].refcnt = 0x00 0x00 0x00
0x00
fldoffset[7] = 0x00, fldmask[7] = 0x00, fldvalue_dyna[7]:0x00 0x00
0x00 0x00
fldcontrol[7].inuse = 0x0 fldcontrol[7].refcnt = 0x00 0x00 0x00
0x00
fldoffset[8] = 0x00, fldmask[8] = 0x00, fldvalue_dyna[8]:0x00 0x00
0x00 0x00
fldcontrol[8].inuse = 0x0 fldcontrol[8].refcnt = 0x00 0x00 0x00
0x00
fldoffset[9] = 0x00, fldmask[9] = 0x00, fldvalue_dyna[9]:0x00 0x00
0x00 0x00
fldcontrol[9].inuse = 0x0 fldcontrol[9].refcnt = 0x00 0x00 0x00
0x00
fldoffset[10] = 0x00, fldmask[10] = 0x00, fldvalue_dyna[10]:0x00 0x00
0x00 0x00
fldcontrol[10].inuse = 0x0 fldcontrol[10].refcnt = 0x00 0x00 0x00
0x00
fldoffset[11] = 0x00, fldmask[11] = 0x00, fldvalue_dyna[11]:0x00 0x00
0x00 0x00
fldcontrol[11].inuse = 0x0 fldcontrol[11].refcnt = 0x00 0x00 0x00
```


0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000

Field dirty indicator: 0x00000000

FDB reference count fdb: 0 [1 0 0 0]
FDB reference count fdb: 1 [0 0 0 0]
FDB reference count fdb: 2 [0 0 0 0]
FDB reference count fdb: 3 [0 0 0 0]
FDB reference count fdb: 4 [0 0 0 0]
FDB reference count fdb: 5 [0 0 0 0]
FDB reference count fdb: 6 [0 0 0 0]
FDB reference count fdb: 7 [0 0 0 0]
FDB reference count fdb: 8 [0 0 0 0]
FDB reference count fdb: 9 [0 0 0 0]
FDB reference count fdb: 10 [0 0 0 0]
FDB reference count fdb: 11 [0 0 0 0]
FDB reference count fdb: 12 [0 0 0 0]
FDB reference count fdb: 13 [0 0 0 0]
FDB reference count fdb: 14 [0 0 0 0]
FDB reference count fdb: 15 [0 0 0 0]
FDB reference count fdb: 16 [0 0 0 0]
FDB reference count fdb: 17 [0 0 0 0]
FDB reference count fdb: 18 [0 0 0 0]
FDB reference count fdb: 19 [0 0 0 0]

Filter counters:

Filter counter 0: 0 (MIRROR1)
Filter counter 1: 0 (MIRROR2)
Filter counter 2: 0 (MIRROR3)
Filter counter 3: 0 (MIRROR4)
Filter counter 4: 0 (AEPORT_NON_MIRR_DROP)
Filter counter 5: 0 (ZONING TRAP)
Filter counter 6: 0 (FCR_EXPORT_DC)
Filter counter 7: 0 (TIN TRAP)
Filter counter 8: 0 (FICON CUP)
Filter counter 9: 0 (FICON CUP DST)
Filter counter 10: 0 (WELL KNOWN ADDR)
Filter counter 11: 0 (SIM)
Filter counter 12: 0 (UNUSED)
Filter counter 13: 0 (UNUSED)
Filter counter 14: 0 (UNUSED)
Filter counter 15: 0 (UNUSED)
Filter counter 16: 0 (PERF1)
Filter counter 17: 0 (PERF2)
Filter counter 18: 0 (PERF3)
Filter counter 19: 0 (PERF4)
Filter counter 20: 0 (PERF5)
Filter counter 21: 0 (PERF6)
Filter counter 22: 0 (PERF7)

Filter counter 23: 0 (PERF8)
Filter counter 24: 0 (PERF9)
Filter counter 25: 0 (PERF10)
Filter counter 26: 0 (PERF11)
Filter counter 27: 0 (PERF12)
Filter counter 28: 0 (OPM1)
Filter counter 29: 0 (OPM2)
Filter counter 30: 0 (IPM1)
Filter counter 31: 0 (IPM2)

ACL DATA

Logical port 27: Hard Zoning enabled, Soft Zoning disabled
Zone type: WWN Zoning
Frames with hard zone miss: 0

*** Please use filterportshow on user port 56 to display ACL hash tables and Mirroring resources of thischip.
***We show this data only for the first physical port which is an external port.

portFcPortCmdShow --slot 0 39 3
doing portFcPortCmdShow: arg1 = 3, arg2 = -2

portshow 39
portDisableReason: None
portCFlags: 0x1
portFlags: 0x1 PRESENT U_PORT
LocalSwcFlags: 0x0
portType: 26.0
POD Port: Port is licensed
portState: 2 Offline
Protocol: FC
portPhys: 4 No_Light portScn: 2 Offline
port generation number: 0
state transition count: 1

portId: 012700
portIfId: 43020019
portWwn: 20:27:d8:1f:cc:2c:99:90
portWwn of device(s) connected:
16b Area list:
Distance: normal
portSpeed: N32Gbps

FEC: Inactive
Credit Recovery: Inactive
LE domain: 0
Peer beacon: Off
FC Fastwrite: OFF
Interrupts: 0
Unknown: 0

Link_failure: 0 Frjt:
Loss_of_sync: 0 Fbsy:

```

Lli:                0          Loss_of_sig: 0
Proc_rqrd:          0          Protocol_err: 0
Timed_out:          0          Invalid_word: 0
Tx_unavail:         0          Invalid_crc: 0
Delim_err:          0          Address_err: 0
Lr_in:              0          Ols_in:      0
Lr_out:             0          Ols_out:    0

```

portloginshow 39

```

Type  PID      World Wide Name      credit df_sz cos
=====

```

portloginshow 39 -history

```

Type  PID      World Wide Name      logout time
=====

```

portregshow 39

LED registers

=====

```

0x81cca000: c4_led_status      00000000      0x81cca004:
c4_led_ctl      00000000

```

FPL registers

=====

```

0x81cc8200: fpl_port_config      23298002
0x81cc820c: fpl_port_id_ctl      00000000      0x81cc8210:
fpl_port_id_addr      00012700
0x81cc8214: fpl_port_speed      00000004      0x81cc821c:
fpl_lli_ctl      00000100
0x81cc8228: fpl_lli_os_ctl      bc94ffff      0x81cc822c:
fpl_lli_send_word      bc95b5b5
0x81cc8230: fpl_lli_mark_rx      00000000      0x81cc8234:
fpl_lli_rnd_trip_time      00000000
0x81cc8238: fpl_lli_ns_status      00130007      0x81cc823c:
fpl_lli_intr_status      00030007
0x81cc8244: fpl_lli_def      00100000      0x81cc8254:
fpl_lli_intr_enable_clr      001c0000
0x81cc8258: fpl_err_intr_status      00000000      0x81cc8260:
fpl_err_intr_enable_clr      00000000
0x81cc8268: fpl_err_first_error      00000000      0x81cc826c:
fpl_speed_neg_ctl      00000000
0x81cc8270: fpl_speed_neg_stat      00000000      0x81cc8274:
fpl_softasn_ctl      0000000f
0x81cc8278: fpl_link_init_ctl      00000000      0x81cc827c:
fpl_link_init_stat      00000000
0x81cc8280: fpl_aec_ctl      001c1060      0x81cc8284:
fpl_aec_ctl2      04009f60
0x81cc8288: fpl_pcs_ctl      00000170      0x81cc828c:
fpl_fec_ctl      00000424
0x81cc8290: fpl_fec_cor      00000000      0x81cc8294:

```

```

fpl_fec_uncor          00000000
0x81cc8298: fpl_hss_link_ctl      0031f040    0x81cc829c:
fpl_afifo_link_ctl    00000a86
0x81cc82a0: fpl_echo_lb_ctl        0000028c    0x81cc82a4:
fpl_scratch           00000121
0x81cc82a8: fpl_debug              00060005    0x81cc82ac:
fpl_misc_debug        00000800
0x00000000: SW_shadow_reg          00000000    0x00000000:
SW_c4_phyp->cfgptr     00030003

```

per-fpg (per octet) registers

=====

```

0x8181b82c: fpg_serdes_ctla0      81a37be7    0x8181b830:
fpg_serdes_ctla1      81a37be7
0x8181b834: fpg_serdes_ctlb0      81a1c3c3    0x8181b838:
fpg_serdes_ctlb1      81a1c3c3
0x8181b83c: fpg_serdes_xgmii_1ms  00067c28    0x8181b840:
fpg_serdes_regtimctl  40e47946
0x8181b844: fpg_serdes_asnrsttimctl 00000102

```

HSS PLL registers

=====

```

0x81819400: 00_hssplla_vco_coarse_cal0  00000000    0x81819404:
01_hssplla_vco_coarse_cal1    00000014
0x81819408: 02_hssplla_vco_coarse_cal2  00000000    0x8181940c:
03_hssplla_vco_coarse_cal3    00000000
0x81819410: 04_hssplla_vco_coarse_cal4  00000000    0x81819424:
09_hssplla_power_ctl          00000000
0x81819428: 0A_hssplla_charge_pump_ctl  00000004    0x81819438:
0E_hssplla_pll_misc_ctl       00000000
0x8181943c: 0F_hssplla_pclk_ctl         000000f8    0x81819440:
10_hssplla_eyem_intv_ctl       00000000
0x81819444: 11_hssplla_eyem_intv_lim1    00000000    0x81819448:
12_hssplla_eyem_intv_lim2     00000000
0x8181944c: 13_hssplla_eyem_intv_lim3    00000000    0x81819450:
14_hssplla_eyem_intv_lim4     00000000
0x818194f0: 3C_hssplla_macro_tst_ctl4    00000000    0x818194f4:
3D_hssplla_macro_tst_ctl3     00000000
0x818194f8: 3E_hssplla_macro_tst_ctl2    00000000    0x818194fc:
3F_hssplla_macro_tst_ctl1     00000000
0x81819500: 00_hssppll_vco_coarse_cal0  0000000a    0x81819504:
01_hssppll_vco_coarse_cal1    00000014
0x81819508: 02_hssppll_vco_coarse_cal2  00000000    0x8181950c:
03_hssppll_vco_coarse_cal3    00000000
0x81819510: 04_hssppll_vco_coarse_cal4  00000000    0x81819524:
09_hssppll_power_ctl          00000000
0x81819528: 0A_hssppll_charge_pump_ctl  00000004    0x81819538:
0E_hssppll_pll_misc_ctl       00000000
0x8181953c: 0F_hssppll_pclk_ctl         000000f8    0x81819540:
10_hssppll_eyem_intv_ctl       00000000
0x81819544: 11_hssppll_eyem_intv_lim1    00000000    0x81819548:
12_hssppll_eyem_intv_lim2     00000000
0x8181954c: 13_hssppll_eyem_intv_lim3    00000000    0x81819550:
14_hssppll_eyem_intv_lim4     00000000

```

| | | |
|---------------------------------------|----------|-------------|
| 0x818195f0: 3C_hsspllb_macro_tst_ctl4 | 00000000 | 0x818195f4: |
| 3D_hsspllb_macro_tst_ctl3 | 00000000 | |
| 0x818195f8: 3E_hsspllb_macro_tst_ctl2 | 00000000 | 0x818195fc: |
| 3F_hsspllb_macro_tst_ctl1 | 00000000 | |

HSS TX registers

=====

| | | |
|---|----------|-------------|
| 0x81818100: 00_hsstx_cfg_mode_PHY | 00009f48 | 0x81818104: |
| 01_hsstx_test_ctl | 00000000 | |
| 0x81818108: 02_hsstx_coeff_ctl_INV | 00000000 | 0x8181810c: |
| 03_hsstx_drv_mode_ctl | 00000000 | |
| 0x81818110: 04_hsstx_drv_ovrd_ctl | 00000010 | 0x81818114: |
| 05_hsstx_dclk_align_ovrd | 00000080 | |
| 0x81818118: 06_hsstx_imp_cal_ovrd | 00000c0c | 0x8181811c: |
| 07_hsstx_dclk_drift_tol | 00000004 | |
| 0x81818120: 08_hsstx_tap0_coeff_TUNE | 00000000 | 0x81818124: |
| 09_hsstx_tap1_coeff_TUNE | 00000003 | |
| 0x81818128: 0A_hsstx_tap2_coeff_TUNE | 00000019 | 0x8181812c: |
| 0B_hsstx_tap3_coeff_TUNE | 00000003 | |
| 0x81818134: 0D_hsstx_pol_INV | 0000000a | 0x81818138: |
| 0E_hsstx_ae_cmd | 00000000 | |
| 0x8181813c: 0F_hsstx_ae_stat | 00000000 | 0x81818140: |
| 10_hsstx_ae_tap0_TUNE | 00000000 | |
| 0x81818144: 11_hsstx_ae_tap1_TUNE | 00000000 | 0x81818148: |
| 12_hsstx_ae_tap2_TUNE | 00000028 | |
| 0x8181814c: 13_hsstx_ae_tap3_TUNE | 00000000 | 0x81818154: |
| 15_hsstx_app_tune | 0000120e | |
| 0x81818158: 16_hsstx_analog_diag | 00000000 | 0x81818160: |
| 18_hsstx_4x_seg_app | 0000aa00 | |
| 0x81818164: 19_hsstx_2x_seg_app | 000000aa | 0x81818168: |
| 1A_hsstx_1x_seg_app | 0000f5e4 | |
| 0x8181816c: 1B_hsstx_seg_4x_term_app | 0000000f | 0x81818170: |
| 1C_hsstx_seg_2x1x_term_app | 00000001 | |
| 0x81818174: 1D_hsstx_tap_sign_app | 0000000a | 0x81818178: |
| 1E_hsstx_ext_addr_data | 00000001 | |
| 0x8181817c: 1F_hsstx_ext_addr_addr | 00000000 | 0x81818180: |
| 20_hsstx_pat_buf_bytes_1_0 | 00000000 | |
| 0x81818184: 21_hsstx_pat_buf_bytes_3_2 | 00000000 | 0x81818188: |
| 22_hsstx_pat_buf_bytes_5_4 | 00000000 | |
| 0x8181818c: 23_hsstx_pat_buf_bytes_7_6 | 00000000 | 0x8181819c: |
| 27_hsstx_8023az_ctl | 00000000 | |
| 0x818181a0: 28_hsstx_dcc_ctl | 000060c0 | 0x818181a4: |
| 29_hsstx_dcc_ovrd | 00001000 | |
| 0x818181a8: 2A_hsstx_dcc_app | 00000083 | 0x818181ac: |
| 2B_hsstx_dcc_timeout | 0000ffff | |
| 0x818181c0: 30_hsstx_tap_sign_ovrd | 00000000 | 0x818181c8: |
| 32_hsstx_seg_4x_ovrd | 00000000 | |
| 0x818181cc: 33_hsstx_seg_2x_ovrd | 00000000 | 0x818181d0: |
| 34_hsstx_seg_1x_ovrd | 00000000 | |
| 0x818181d8: 36_hsstx_tap_seg_4x_term_ovrd | 00000000 | 0x818181dc: |
| 37_hsstx_tap_seg_2x_term_ovrd | 00000000 | |
| 0x818181e0: 38_hsstx_tap_seg_1x_term_ovrd | 00000000 | 0x818181ec: |
| 3B_hsstx_mac_test_ctl5 | 00000000 | |
| 0x818181f0: 3C_hsstx_mac_test_ctl4 | 00000000 | 0x818181f4: |

| | | |
|------------------------------------|----------|-------------|
| 3D_hsstx_mac_test_ctl3 | 00000000 | |
| 0x818181f8: 3E_hsstx_mac_test_ctl2 | 00000000 | 0x818181fc: |
| 3F_hsstx_mac_test_ctl1 | 000000c6 | |

HSS RX registers

=====

| | | |
|---|----------|-------------|
| 0x81818300: 00_hssrx_cfg_mode_PHY | 00009e78 | 0x81818304: |
| 01_hssrx_test_ctl | 00000000 | |
| 0x81818308: 02_hssrx_phs_rot_ctl | 0000cb80 | 0x8181830c: |
| 03_hssrx_phs_rot_ofs_ctl | 00000610 | |
| 0x81818310: 04_hssrx_phs_rot_posn1 | 00003e3c | 0x81818314: |
| 05_hssrx_phs_rot_posn2 | 0000002d | |
| 0x81818318: 06_hssrx_phs_rot_sta_ofs1 | 00000001 | 0x8181831c: |
| 07_hssrx_phs_rot_sta_ofs2 | 0000001f | |
| 0x81818320: 08_hssrx_dfe_ctl_PHY | 00002002 | 0x81818324: |
| 09_hssrx_dfe_smpl_snap1 | 00000000 | |
| 0x81818328: 0A_hssrx_dfe_smpl_snap2 | 00008000 | 0x8181832c: |
| 0B_hssrx_vga_ctl1 | 000041fe | |
| 0x81818330: 0C_hssrx_vga_ctl2 | 00007aa0 | 0x81818334: |
| 0D_hssrx_vga_ctl3 | 000009e4 | |
| 0x81818338: 0E_hssrx_pwr_mgmt_ctl | 0000001f | 0x8181833c: |
| 0F_hssrx_iqamp_ctl1 | 00000019 | |
| 0x81818340: 10_hssrx_iqamp_ctl2 | 00000006 | 0x81818344: |
| 11_hssrx_dacap_dacan_sel | 00000003 | |
| 0x81818348: 12_hssrx_dacap_dacan | 000000ff | 0x8181834c: |
| 13_hssrx_daca_min | 00000000 | |
| 0x81818350: 14_hssrx_adac_ctl | 00000000 | 0x81818354: |
| 15_hssrx_ac_cp_ctl | 000031c3 | |
| 0x81818358: 16_hssrx_ac_cp_val | 00008055 | 0x8181835c: |
| 17_hssrx_dfe_h1h2h3_lcl_off_ch | 00000014 | |
| 0x81818360: 18_hssrx_dfe_h1h2h3_lcl_off_val | 00000000 | 0x81818364: |
| 19_hssrx_peaked_intg | 000000ff | |
| 0x81818368: 1A_hssrx_cdr_analog_sw | 0000ce00 | 0x8181836c: |
| 1B_hssrx_peaking_amp_init_c_PHY | 00000000 | |
| 0x81818370: 1C_hssrx_dac_dpc | 00000040 | 0x81818374: |
| 1D_hssrx_ddc | 00000000 | |
| 0x81818378: 1E_hssrx_int_stat_PHY | 00000c0f | 0x8181837c: |
| 1F_hssrx_dfe_func_ctl1_PHY | 0000ffff | |
| 0x81818380: 20_hssrx_dfe_func_ctl2_INV | 00007eff | 0x81818384: |
| 21_hssrx_ofs_ch_dcc_qcc_idx | 00002000 | |
| 0x81818388: 22_hssrx_dfe_ofs_val | 00000704 | 0x8181838c: |
| 23_hssrx_h_coeff_bist | 00000401 | |
| 0x81818390: 24_hssrx_ac_cap_bist | 00000000 | 0x81818394: |
| 25_hssrx_max_gain_path_idx_res | 00007800 | |
| 0x81818398: 26_hssrx_loff_ctl | 00000040 | 0x8181839c: |
| 27_hssrx_sigdet_ctl | 00000080 | |
| 0x818183a0: 28_hssrx_ana_ctl_sw | 00000000 | 0x818183a4: |
| 29_hssrx_intg_dac_ofs | 0000acdb | |
| 0x818183a8: 2A_hssrx_eye_ctl | 00000000 | 0x818183ac: |
| 2B_hssrx_eye_met | 00000004 | |
| 0x818183b0: 2C_hssrx_eye_met_err_cnt | 00000000 | 0x818183b4: |
| 2D_hssrx_eye_met_pdf_eyec | 00000000 | |
| 0x818183b8: 2E_hssrx_eye_met_pat_len | 0000007f | 0x818183bc: |
| 2F_hssrx_dfe_func_ctl3 | 0000dfff | |

```

0x818183c0: 30_hssrx_dfe_tap_ctl_idx_ptr      00000008      0x818183c4:
31_hssrx_dfe_tap                        00003030
0x818183c8: 32_hssrx_lte_ctl_TUNE                  00000600      0x818183e4:
39_hssrx_int_stat2                      0000c1ff
0x818183e8: 3A_hssrx_ac_cpl_cur_src_adj           00000041      0x818183ec:
3B_hssrx_dcd_ctl                        00007c4a
0x818183f0: 3C_hssrx_dcc_ctl                      00000d41      0x818183f4:
3D_hssrx_qcc_ctl                        00006981
0x818183f8: 3E_hssrx_mac_test_ctl2                00000000      0x818183fc:
3F_hssrx_mac_test_ctl1                  00000000
0x81818348: 12_hssrx_dacap_dacan[02]              00ff 00ff
0x81818360: 18_hssrx_dfe_h1h2h3_lcl_off_va[00]    0000 0000 0000
0000 0000 0000 0000 0000
0x81818360: 18_hssrx_dfe_h1h2h3_lcl_off_va[08]    0000 0000 0000
0000 0000 0000 0000 0000
0x81818360: 18_hssrx_dfe_h1h2h3_lcl_off_va[16]    0000 0000 0000
0000 0000
0x81818388: 22_hssrx_dfe_ofs_val[00][00]          0704 7f7f 0579
7f00 0305 007f
0x81818388: 22_hssrx_dfe_ofs_val[03][00]          0906 7f7f 7c05
007f 7c7d 0000
0x81818388: 22_hssrx_dfe_ofs_val[06][00]          7b7d 0000 7e7f
0000 7d7f 0000
0x81818388: 22_hssrx_dfe_ofs_val[09][00]          057f 7f00 057a
7f00 0a02 7f7f
0x81818388: 22_hssrx_dfe_ofs_val[12][00]          7b0b 007f 7f07
007f 7d07 007f
0x81818388: 22_hssrx_dfe_ofs_val[15][00]          7f03 0000 7d7c
0000 7b03 0000
0x81818388: 22_hssrx_dfe_ofs_val[18][00]          7d7b 0000 7a7d
0000 007f 0000
0x81818388: 22_hssrx_dfe_ofs_val[21][00]          007f 0000 007f
0000 007f 0000
0x81818388: 22_hssrx_dfe_ofs_val[24][00]          7e7a 7f01 0579
7f00 017f 0000
0x81818394: 25_hssrx_max_gain_path_idx_res[00]    0055 084b 1003
1891 20d0 289a 3086 3800
0x81818394: 25_hssrx_max_gain_path_idx_res[08]    40c0 488a 5076
5800 6040 6800 70fe 7800
0x818183c4: 31_hssrx_dfe_tap[00]                  fffe 8181 0000
0000 0030 0030 3030 3030
0x818183c4: 31_hssrx_dfe_tap[08]                  3030 3030 3030
0000
0x818183e8: 3A_hssrx_ac_cpl_cur_src_adj[00]       0041 0041 0041
0041
0x818183ec: 3B_hssrx_dcd_ctl[00]                  7c4a 5c00 7c86
5c00 7c00
0x818183f0: 3C_hssrx_dcc_ctl[00]                  0d41 0d43 0d00
0d00
0x818183f4: 3D_hssrx_qcc_ctl[00]                  6942 6981

```

xfipcs, fec, aec, & aet registers

=====

```

0x81cc8400: xfipcs_reg      [00] 00002040 00000080 00000000

```

```

00000000 00000001 00000008 00000000 00000000
0x81cc8420: xfipcs_reg [08] 00008401 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81cc8440: xfipcs_reg [16] 00000000 00000000 00000000
00000000 00000040 00000000 00000000 00000000
0x81cc8460: xfipcs_reg [24] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81cc8480: xfipcs_reg [32] 00000004 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81cc8620: fec_32g_128g_reg [08] 00000000 00008003 00000000
00000000 00000000 00000000 00000000
0x81cc8648: fec_32g_128g_reg [18] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81cc8a00: aec_reg [00] 00000000 00000000 00000000
00000000 00000040 00000000 00000000 00002490
0x81cc8c00: aet_reg [00] 000000b0 00007000 000008c4
00000000 00000000

```

bbc registers

=====

```

0x81cc9800: bbc_trc 0 0 0 0 0 0 0
0
0x81cc9840: bbc_trc 0 0 0 0 0 0 0
0
0x81cc9880: bbc_trc 0 0 0 0 0 0 0
0
0x81cc98c0: bbc_trc 0 0 0 0 0 0 0
0
0x81cc9900: bbc_trc 0 0 0 0 0 0 0
0
0x81cc9804: bbc_mbc 0 0 0 0 0 0 0
0
0x81cc9844: bbc_mbc 0 0 0 0 0 0 0
0
0x81cc9884: bbc_mbc 0 0 0 0 0 0 0
0
0x81cc98c4: bbc_mbc 0 0 0 0 0 0 0
0
0x81cc9904: bbc_mbc 0 0 0 0 0 0 0
0
0x81cc9a00: bbc_rcc 0 0 0 0 0 0 0
0
0x81cc9a20: bbc_rcc 0 0 0 0 0 0 0
0
0x81cc9a40: bbc_rcc 0 0 0 0 0 0 0
0
0x81cc9a60: bbc_rcc 0 0 0 0 0 0 0
0
0x81cc9a80: bbc_rcc 0 0 0 0 0 0 0
0
0x81cc9c00: bbc_rqc 0 0 0 0 0 0 0
0
0x81cc9c20: bbc_rqc 0 0 0 0 0 0 0
0

```

| | | | | | | | |
|-------------------------------------|----------|---|---|---|---|----------------------|---|
| 0x81cc9c40: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81cc9c60: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81cc9c80: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81cc9d00: bbc_fbpc | 00000000 | | | | | 0x81cc9d04: bbc_csc | |
| 00000000 | | | | | | | |
| 0x81cc9d08: bbc_rcc_inc | 00000000 | | | | | 0x81cc9d0c: | |
| bbc_rqc_inc | 00000000 | | | | | | |
| 0x81cc9d10: bbc_fbpc_inc | 00000000 | | | | | 0x81cc9d14: | |
| bbc_tmc_inc | 00000000 | | | | | | |
| 0x81cc9d18: bbc_threshold | 00080100 | | | | | 0x81cc9d1c: | |
| bbc_counter_clr | 00000000 | | | | | | |
| 0x81cc9d20: bbc_debug_en | 00000000 | | | | | 0x81cc9d24: bbc_ctrl | |
| 00200120 | | | | | | | |
| 0x81cc9d28: bbc_rqc_rcc_thresh | 00000055 | | | | | 0x81cc9d34: | |
| bbc_bb_sc_n | 00000000 | | | | | | |
| 0x81cc9d38: bbc_crd_reco_debug | 00000000 | | | | | 0x81cc9d3c: | |
| bbc_crd_reco_debug_data | 00000000 | | | | | | |
| 0x81cc9d40: bbc_multi_frm_loss_cnt | 00000000 | | | | | 0x81cc9d44: | |
| bbc_multi_rdy_loss_cnt | 00000000 | | | | | | |
| 0x81cc9d48: bbc_1frm_loss_recov_cnt | 00000000 | | | | | 0x81cc9d4c: | |
| bbc_1rdy_loss_recov_cnt | 00000000 | | | | | | |
| 0x81cc9d58: bbc_int_status | 00000000 | | | | | 0x81cc9d5c: | |
| bbc_int_set | 00000000 | | | | | | |
| 0x81cc9d60: bbc_int_first | 00000000 | | | | | 0x81cc9d64: | |
| bbc_frm_rdy_rx_err_addr | 00000000 | | | | | | |
| 0x81cc9d68: bbc_frm_rdy_tx_err_addr | 00000000 | | | | | 0x81cc9d6c: | |
| bbc_trc_mbc_err_addr | 00000000 | | | | | | |
| 0x81cc9d70: bbc_frm_rdy_rx_dbl_ecc | 00000000 | | | | | 0x81cc9d74: | |
| bbc_frm_rdy_tx_dbl_ecc | 00000000 | | | | | | |
| 0x81cc9d78: bbc_trc_mbc_dbl_ecc | 00000000 | | | | | | |
| 0x81cc9d7c: bbc_fsm_status | 00001011 | | | | | 0x81cc9d80: | |
| bbc_force_err | 00000000 | | | | | | |
| 0x81cc9d84: bbc_crdt_avail0 | 00000000 | | | | | 0x81cc9d88: | |
| bbc_crdt_avail1 | 00000000 | | | | | | |
| 0x81cc9d8c: bbc_scratch | 00000000 | | | | | | |

FPS registers

=====

| | | | | | | | |
|----------------------------|----------|--|--|--|--|-------------|--|
| 0x81cc8004: fps_er_enc_in | 00000000 | | | | | 0x81cc8008: | |
| fps_er_crc | 00000000 | | | | | | |
| 0x81cc800c: fps_er_trunc | 00000000 | | | | | 0x81cc8010: | |
| fps_er_toolong | 00000000 | | | | | | |
| 0x81cc8014: fps_er_bad_eof | 00000000 | | | | | 0x81cc8018: | |
| fps_er_enc_out | 00000000 | | | | | | |
| 0x81cc801c: fps_er_bad_os | 00000000 | | | | | 0x81cc8020: | |
| fps_er_flush | 00000000 | | | | | | |
| 0x81cc8024: fps_er_ifg | 00000000 | | | | | 0x81cc8038: | |
| fps_er_crc_good_eof | 00000000 | | | | | | |
| 0x81cc803c: fps_inv_arb | 00000000 | | | | | 0x81cc8040: | |
| fps_slow_sts_status | 00000000 | | | | | | |
| 0x81cc8044: fps_tx_frm_cnt | 00000000 | | | | | 0x81cc8048: | |


```

fps_rx_frm_cnt          00000000
0x81cc8050: fps_tx_word_cnt_hi      00000000    0x81cc804c:
fps_tx_word_cnt_lo      00000000
0x81cc8058: fps_rx_word_cnt_hi      00000000    0x81cc8054:
fps_rx_word_cnt_lo      00000000

```

BAL registers

=====

```

0x81ccf000: bal_desired_buf          00000000    0x81ccf004:
bal_alloc_buf           00000000
0x81ccf008: bal_busy_buf              00000000    0x81ccf00c:
bal_usable_buf          00000000
0x81ccf010: bal_max_bor_buf            00000000
0x81ccf014: bal_busy_buf_thresh      00000002

```

TXQ registers

=====

```

0x81ccb004: txq_phys_port_ctl          00410000
0x81ccb050: txq_link_skew              00000000
0x81ccb068: txq_cr_lk_dttm_intr_sts [00] 00000000 00000000
0x81ccb070: txq_cr_lk_dttm_intr_en [00] 00000000 00000000
0x81ccb024: txq_disc_frm_trap_cnt      00000014

```

FDS registers

=====

```

0x81ccc000: fds_rxf_ctl                00000002    0x81ccc004:
fds_rxf_wait_thresh     00000909
0x81ccc018: fds_rxf_first_error        00000000    0x81ccc01c:
fds_rxf_first_error_info 00000000
0x81ccc020: fds_rxf_inout_pkt_cnt      00000000
0x81ccc008: fds_rxf_err_int_status     00000000    0x81ccc024:
fds_rxf_fifo_status     00888888
0x81ccd000: fds_txf_ctl                0000003a    0x81ccd004:
fds_txf_wait_ifg_thresh 00a00106
0x81ccd008: fds_txf_err_int_status     00000000    0x81ccd024:
fds_txf_fifo_status     00088888
0x81ccd02c: fds_txf_bbc_scs           00000000

```

Logical TXQ registers

=====

```

0x81ccb000: txq_log_port_ctl          00000002    0x81ccb008:
txq_port_status         00000000
0x81ccb00c: txq_todo_flags            [00] 00000000 00000000
0x81ccb014: txq_spd_match_desc        [00] 00000000 00000000 00000000
00000000
0x81ccb024: txq_spd_match_desc        [04] 00000014
0x81ccb028: txq_vc_weight            [00] 01010101 01010101 01010101
01010101
0x81ccb038: txq_vc_weight            [04] 01010101 01010101 01010101
01010101
0x81ccb048: txq_vc_weight            [08] 01010101 00010101
0x81ccb054: txq_cong_dttm_ctrl        00000106
0x81ccb058: txq_cong_dttm_intr_sts [00] 00000000 00000000
0x81ccb060: txq_cong_dttm_intr_en [00] 00000000 00000000

```

| | | | |
|---------------------------------|------|----------|-------------------|
| 0x81ccb078: txq_bw_limit_en_reg | [00] | 00000000 | 00000000 |
| 0x81ccb080: txq_bw_gua_en_reg | [00] | 00000000 | 00000000 |
| 0x81ccb088: txq_vc_group | [00] | 03030300 | 03030303 03030303 |
| 03030303 | | | |
| 0x81ccb098: txq_vc_group | [04] | 03030303 | 03030303 03030303 |
| 03030303 | | | |
| 0x81ccb0a8: txq_vc_group | [08] | 03030303 | 03030303 00000000 |
| 00000000 | | | |
| 0x81ccb0b0: txq_bw_thresh_group | [00] | 00000000 | 00000000 00000000 |
| 00000000 | | | |
| 0x81ccb0c0: txq_bw_thresh_group | [04] | 00000000 | 00000000 00000000 |
| 00000000 | | | |
| 0x81ccb0d0: txq_bw_thresh_group | [08] | 00000000 | 00000000 00000000 |
| 00000000 | | | |
| 0x81ccb0e0: txq_bw_thresh_group | [12] | 00000000 | 00000000 00000000 |
| 00000000 | | | |
| 0x81ccb0f0: txq_bw_thresh_group | [16] | 00000000 | 00000000 00000000 |
| 00000000 | | | |
| 0x81ccb100: txq_bw_thresh_group | [20] | 00000000 | 00000000 00000000 |
| 00000000 | | | |
| 0x81ccb110: txq_bw_thresh_group | [24] | 00000000 | 00000000 00000000 |
| 00000000 | | | |
| 0x81ccb120: txq_bw_thresh_group | [28] | 00000000 | 00000000 00000000 |
| 00000000 | | | |
| 0x81ccb130: txq_bw_thresh_group | [32] | 00000000 | 00000000 00000000 |
| 00000000 | | | |
| 0x81ccb140: txq_bw_thresh_group | [36] | 00000000 | 00000000 00000000 |
| 00000000 | | | |

txq Congestion detection Statistics RAM

=====

| | | |
|--------------------|----------|--------------------|
| 0x81090fa0: vc[0] | 00000000 | 0x81090fa4: vc[1] |
| 00000000 | | |
| 0x81090fa8: vc[2] | 00000000 | 0x81090fac: vc[3] |
| 00000000 | | |
| 0x81090fb0: vc[4] | 00000000 | 0x81090fb4: vc[5] |
| 00000000 | | |
| 0x81090fb8: vc[6] | 00000000 | 0x81090fbc: vc[7] |
| 00000000 | | |
| 0x81090fc0: vc[8] | 00000000 | 0x81090fc4: vc[9] |
| 00000000 | | |
| 0x81090fc8: vc[10] | 00000000 | 0x81090fcc: vc[11] |
| 00000000 | | |
| 0x81090fd0: vc[12] | 00000000 | 0x81090fd4: vc[13] |
| 00000000 | | |
| 0x81090fd8: vc[14] | 00000000 | 0x81090fdc: vc[15] |
| 00000000 | | |
| 0x81090fe0: vc[16] | 00000000 | 0x81090fe4: vc[17] |
| 00000000 | | |
| 0x81090fe8: vc[18] | 00000000 | 0x81090fec: vc[19] |
| 00000000 | | |
| 0x81090ff0: vc[20] | 00000000 | 0x81090ff4: vc[21] |
| 00000000 | | |
| 0x81090ff8: vc[22] | 00000000 | 0x81090ffc: vc[23] |

```

00000000
0x81091000: vc[24]      00000000      0x81091004: vc[25]
00000000
0x81091008: vc[26]      00000000      0x8109100c: vc[27]
00000000
0x81091010: vc[28]      00000000      0x81091014: vc[29]
00000000
0x81091018: vc[30]      00000000      0x8109101c: vc[31]
00000000
0x81091020: vc[32]      00000000      0x81091024: vc[33]
00000000
0x81091028: vc[34]      00000000      0x8109102c: vc[35]
00000000
0x81091030: vc[36]      00000000      0x81091034: vc[37]
00000000
0x81091038: vc[38]      00000000      0x8109103c: vc[39]
00000000

```

Logical STS registers

```

=====
0x81585344: sts_ftb_type1_miss      00000000
0x81585348: sts_ftb_type2_miss      00000000
0x8158534c: sts_ftb_type6_miss      00000000
0x81585350: sts_hard_zoning_miss    00000000
0x81585354: sts_lun_zoning_miss     00000000
0x8158535c: sts_unroutable                 00000000
0x81582374: sts_rte_cl2                 00000000      0x81582378:
sts_rte_cl3                 00000000      0x8158237c: sts_rte_link_ctl
00000000      0x81585368: sts_tx_timeout           00000000

```

Logical STS filter registers

```

=====
0x815852c0: stsflt_trig      [00] 00000000 00000000 00000000
00000000
0x815852d0: stsflt_trig      [04] 00000000 00000000 00000000
00000000
0x815852e0: stsflt_trig      [08] 00000000 00000000 00000000
00000000
0x815852f0: stsflt_trig      [12] 00000000 00000000 00000000
00000000
0x81585300: stsflt_trig      [16] 00000000 00000000 00000000
00000000
0x81585310: stsflt_trig      [20] 00000000 00000000 00000000
00000000
0x81585320: stsflt_trig      [24] 00000000 00000000 00000000
00000000
0x81585330: stsflt_trig      [28] 00000000 00000000 00000000
00000000
0x81585340: stsflt_trig      [32]

```

Logical STS discard registers

```

=====
0x81583454: disc_mcast_wka      00000000      0x81583458:

```

```

disc_inv_did          00000000
0x8158345c: disc_cl1_cl4          00000000    0x81583460:
disc_sid_chk_fail    00000000
0x81583464: disc_inv_dom_egid_txpt 00000000    0x81583468:
disc_vft_hop_cnt_1   00000000
0x8158346c: disc_classf          00000000    0x81583470:
disc_fcp_cdb_inv     00000000
0x81583474: disc_vfid_trap_enabled 00000000    0x81583478:
disc_vfid_hdr_chk_fail 00000000
0x8158347c: disc_shim_cksum_fail  00000000    0x81583480:
disc_fed_edit_cmd_err 00000000
0x81583484: disc_ftb_vm_mode      00000000    0x81583488:
disc_ftb_agnt2_miss  00000000
0x8158348c: disc_ecb_reserved    00000000    0x81583490:
disc_ecb_de_pad_err   00000000
0x81583494: disc_ecb_de_tag_err   00000000    0x81583498:
disc_ecb_de_seq_err   00000000
0x8158349c: disc_ecb_err          00000000    0x815834a0:
disc_ftb_type4_match  00000000
0x815834a4: disc_fcp_rsp_ftb_type4 00000000    0x815834a8:
disc_ftb_type5_match  00000000
0x815834ac: disc_ftb_type3_match  00000000    0x815834b0:
disc_els_ftb_type3    00000000
0x815834b4: disc_ftb_type1_match  00000000    0x815834b8:
disc_els_rsp_ex_port  00000000
0x815834bc: disc_inv_drp_dps      00000000    0x815834c0:
disc_did_lookup_miss  00000000
0x815834c4: disc_ftb_type2_match  00000000    0x815834c8:
disc_trpd_plogi_pdisc 00000000
0x815834cc: disc_type2_lookup_miss 00000000    0x815834d0:
disc_ftb_type6_match  00000000
0x815834d4: disc_els_rep_ex_port  00000000    0x815834d8:
disc_els_sid_lkup_bit1 00000000
0x815834dc: disc_els_sid_lkup_bit0 00000000    0x815834e0:
disc_bls_frm_trap_bit1 00000000
0x815834e4: disc_ftb_token_err    00000000    0x815834e8:
disc_asic_internal_err 00000000
0x815834ec: disc_hard_zone_miss   00000000    0x815834f0:
disc_lun_zone_miss    00000000
0x815834f4: discflt_frame_disc    00000000    0x815834f8:
discflt_parity_err    00000000
0x815834fc: disc_frame_marked_du  00000000    0x81583500:
disc_frame_marked_to  00000000
0x81583504: disc_lkup_rte_prty_err 00000000

```

portstatsshow 39

```

stat_wtx          0          4-byte words transmitted
stat_wrx          0          4-byte words received
stat_ftx          0          Frames transmitted
stat_frx          0          Frames received
stat_c2_frx       0          Class 2 frames received
stat_c3_frx       0          Class 3 frames received
stat_lc_rx        0          Link control frames

```

| | | | | | |
|------------------------------|------------|-----|-----|----------|-------------------------|
| received | | | | | |
| stat_mc_rx | 0 | | | | Multicast frames |
| received | | | | | |
| stat_mc_to | 0 | | | | Multicast timeouts |
| stat_mc_tx | 0 | | | | Multicast frames |
| transmitted | | | | | |
| tim_txcrd_z | 0 | | | | Time TX Credit Zero |
| (2.5Us ticks) | | | | | |
| tim_txcrd_z_vc 0- 3: | 0 | 0 | 0 | 0 | |
| tim_txcrd_z_vc 4- 7: | 0 | 0 | 0 | 0 | |
| tim_txcrd_z_vc 8-11: | 0 | 0 | 0 | 0 | |
| tim_txcrd_z_vc 12-15: | 0 | 0 | 0 | 0 | |
| lat_tot_pkt_vc 0- 3: | 1 | 1 | 1 | 1 | |
| lat_tot_pkt_vc 4- 7: | 1 | 1 | 1 | 1 | |
| lat_tot_pkt_vc 8-11: | 1 | 1 | 1 | 1 | |
| lat_tot_pkt_vc 12-15: | 1 | 1 | 1 | 1 | |
| lat_hi_time_vc 0- 3: | 0 | 0 | 0 | 0 | |
| lat_hi_time_vc 4- 7: | 0 | 0 | 0 | 0 | |
| lat_hi_time_vc 8-11: | 0 | 0 | 0 | 0 | |
| lat_hi_time_vc 12-15: | 0 | 0 | 0 | 0 | |
| lat_lo_time_vc 0- 3: | 1 | 1 | 1 | 1 | |
| lat_lo_time_vc 4- 7: | 1 | 1 | 1 | 1 | |
| lat_lo_time_vc 8-11: | 1 | 1 | 1 | 1 | |
| lat_lo_time_vc 12-15: | 1 | 1 | 1 | 1 | |
| max_latency_vc 0- 3: | 1 | 1 | 1 | 1 | |
| max_latency_vc 4- 7: | 1 | 1 | 1 | 1 | |
| max_latency_vc 8-11: | 1 | 1 | 1 | 1 | |
| max_latency_vc 12-15: | 1 | 1 | 1 | 1 | |
| latency_dma_ts | 09-09-2024 | UTC | Mon | 08:47:24 | TXQ |
| Latency DMA TimeStamp | | | | | |
| fec_cor_detected | 0 | | | | Count of blocks that |
| were corrected by FEC | | | | | |
| fec_uncor_detected | 0 | | | | Count of blocks that |
| were left uncorrected by FEC | | | | | |
| er_enc_in | 0 | | | | Encoding errors inside |
| of frames | | | | | |
| er_crc | 0 | | | | Frames with CRC errors |
| er_trunc | 0 | | | | Frames shorter than |
| minimum | | | | | |
| er_toolong | 0 | | | | Frames longer than |
| maximum | | | | | |
| er_bad_eof | 0 | | | | Frames with bad end-of- |
| frame | | | | | |
| er_enc_out | 0 | | | | Encoding error outside |
| of frames | | | | | |
| er_bad_os | 0 | | | | Invalid ordered set |
| er_pcs_blk | 0 | | | | PCS block errors |
| er_rx_c3_timeout | 0 | | | | Class 3 receive frames |
| discarded due to timeout | | | | | |
| er_tx_c3_timeout | 0 | | | | Class 3 transmit frames |
| discarded due to timeout | | | | | |
| er_unroutable | 0 | | | | Frames that are |
| unroutable | | | | | |
| er_unreachable | 0 | | | | Frame with unreachable |

| | | | |
|-----------------------|-----------------------------|--|--------------------------|
| destination | | | |
| er_other_discard | 0 | | Other discards |
| er_type1_miss | 0 | | frames with FTB type 1 |
| miss | | | |
| er_type2_miss | 0 | | frames with FTB type 2 |
| miss | | | |
| er_type6_miss | 0 | | frames with FTB type 6 |
| miss | | | |
| er_zone_miss | 0 | | frames with hard zoning |
| miss | | | |
| er_lun_zone_miss | 0 | | frames with LUN zoning |
| miss | | | |
| er_crc_good_eof | 0 | | Crc error with good eof |
| er_inv_arb | 0 | | Invalid ARB |
| er_single_credit_loss | 0 | | Single vcrdy/frame loss |
| on link | | | |
| er_multi_credit_loss | 0 | | Multiple vcrdy/frame |
| loss on link | | | |
| other_credit_loss | 0 | | Link timeout/complete |
| credit loss | | | |
| phy_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | | Timestamp of |
| phy_port stats clear | | | |
| lgc_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | | Timestamp of |
| lgc_port stats clear | | | |
| fec_corrected_rate | 0 | | FEC Corrected blocks per |
| second | | | |

portstats64show 39

| | | |
|---------------|---|--|
| stat64_wtx | 0 | top_int : 4-byte words transmitted |
| | 0 | bottom_int : 4-byte words transmitted |
| stat64_wrx | 0 | top_int : 4-byte words received |
| | 0 | bottom_int : 4-byte words received |
| stat64_ftx | 0 | top_int : Frames transmitted |
| | 0 | bottom_int : Frames transmitted |
| stat64_frx | 0 | top_int : Frames received |
| | 0 | bottom_int : Frames received |
| stat64_c2_frx | 0 | top_int : Class 2 frames received |
| | 0 | bottom_int : Class 2 frames received |
| stat64_c3_frx | 0 | top_int : Class 3 frames received |
| | 0 | bottom_int : Class 3 frames received |
| stat64_lc_rx | 0 | top_int : Link control frames received |
| | 0 | bottom_int : Link control frames |
| received | | |
| stat64_mc_rx | 0 | top_int : Multicast frames received |
| | 0 | bottom_int : Multicast frames received |
| stat64_mc_to | 0 | top_int : Multicast timeouts |
| | 0 | bottom_int : Multicast timeouts |
| stat64_mc_tx | 0 | top_int : Multicast frames transmitted |
| | 0 | bottom_int : Multicast frames |
| transmitted | | |
| tim64_rdy_pri | 0 | top_int : Time R_RDY high priority |
| | 0 | bottom_int : Time R_RDY high priority |
| tim64_txcrd_z | 0 | top_int : Time BB_credit zero |
| | 0 | bottom_int : Time BB_credit zero |

| | | |
|---|---|--|
| er64_enc_in | 0 | top_int : Encoding errors inside of |
| frames | 0 | bottom_int : Encoding errors inside of |
| frames | | |
| er64_crc | 0 | top_int : Frames with CRC errors |
| | 0 | bottom_int : Frames with CRC errors |
| er64_trunc | 0 | top_int : Frames shorter than minimum |
| | 0 | bottom_int : Frames shorter than minimum |
| er64_toolong | 0 | top_int : Frames longer than maximum |
| | 0 | bottom_int : Frames longer than maximum |
| er64_bad_eof | 0 | top_int : Frames with bad end-of-frame |
| | 0 | bottom_int : Frames with bad end-of- |
| frame | | |
| er64_enc_out | 0 | top_int : Encoding error outside of |
| frames | 0 | bottom_int : Encoding error outside of |
| frames | | |
| er64_disc_c3 | 0 | top_int : Class 3 frames discarded |
| | 0 | bottom_int : Class 3 frames discarded |
| er64_pcs_blk | 0 | top_int : PCS block errors |
| | 0 | bottom_int : PCS block errors |
| stat64_rateTxFrame | 0 | Tx frame rate (fr/sec) |
| stat64_rateRxFrame | 0 | Rx frame rate (fr/sec) |
| stat64_rateTxPeakFrame | 0 | Tx peak frame rate (fr/sec) |
| stat64_rateRxPeakFrame | 0 | Rx peak frame rate (fr/sec) |
| stat64_rateTxWord | 0 | Tx Word rate (words/sec) |
| stat64_rateRxWord | 0 | Rx Word rate (words/sec) |
| stat64_rateTxPeakWord | 0 | Tx peak Word rate (words/sec) |
| stat64_rateRxPeakWord | 0 | Rx peak Word rate (words/sec) |
| stat64_PRJTFrames | 0 | top_int : Number of PRJT frames |
| returned to this port | 0 | bottom_int : Number of PRJT |
| frames returned to this port | | |
| stat64_PBSYFrames | 0 | top_int : Number of PBSY frames |
| returned to this port | 0 | bottom_int : Number of PBSY |
| frames returned to this port | | |
| stat64_inputBuffersFull | 0 | top_int : Number of occurrences |
| when all input buffers full | 0 | bottom_int : Number of |
| occurrences when all input buffers full | | |
| stat64_rxClass1Frames | 0 | top_int : Number of class 1 |
| frames received | 0 | bottom_int : Number of class 1 |
| frames received | | |
| stat64_aveTxFrameSize | 0 | Average Tx Frame size |
| stat64_aveRxFrameSize | 0 | Average Rx Frame size |
| Lr_in | 0 | top_int |
| | 0 | bottom_int |
| 0ls_in | 0 | top_int |
| | 0 | bottom_int |
| Lr_out | 0 | top_int |
| | 0 | bottom_int |
| 0ls_out | 0 | top_int |

```

Link_failure      0          bottom_int
                  0          top_int
Invalid_CRC       0          bottom_int
                  0          top_int
Invalid_word      0          bottom_int
                  0          top_int
Protocol_err      0          bottom_int
                  0          top_int
Loss_of_sig       0          top_int
                  0          bottom_int
Loss_of_sync      0          top_int
                  0          bottom_int
er_bad_os         0          top_int : Invalid ordered set
                  0          bottom_int: Invalid ordered set

```

```

portrouteshow 39
port address ID: 0x012700
external unicast routing table:
  0: Embedded
 255: Embedded
internal unicast routing table:
  0: Embedded

```

portcamshow 39

```

-----
Port  SID used  DID used  SID entries  DID entries
39    0         0         000000      000000
-----

```

ptbufshow, ptcreditshow, ptdatashow, ptstatsshow 39

```

S:
S:VF Enable:          1
S:
S:C4 Global Variable:
S:-----
-----
S:trace_stop:        0
S:
S:C4 Phy Data Pointers: c4_phyp = 0xb6ae9040
S:-----
-----
S:tnodep              0xbb848000      pt
  0x43028019
S:proto_phyp          0xb880aea0      phy_cfg
0xb6aea080
S:c4_chp              0x97e28000      c4_lgcp
0x97fac000
S:c4_phy_regp         0x81cc8000      proc_dir
0xb851cd20
S:-----
-----
S:magic_id            0xc4345678      num_port_timer      12

```


| | | | |
|----------------------------|------------|-----------------------|-----|
| S:prev_if_id | 0x43020019 | S:ftx | 0 |
| tov | 0 | | |
| S:initialized | 1 | port_idx | 25 |
| S:ui_idx | 39 | slot_no | |
| 0 | | | |
| S:blade_idx | 25 | sw_usr_ports | 400 |
| S:unused | 0 | intr_debounced | |
| 0 | | | |
| S:aec_status | 0x0 | reason_code | |
| 0 | | | |
| S:debug | 0x00000004 | debug_trc_line | 0 |
| S:rxbuf_list_head | 0xffffffff | rxbuf_list_tail | |
| 0xffffffff | | | |
| S:isAePort | 0 | port_misc_data | |
| 0 | | | |
| S:num_fault1_rx_disc | 0 | num_fault2_rx_disc | 0 |
| S:p_llli_cause0 | 0 | p_sig_regained | 0 |
| S:p_sync_regained | 0 | enc_out | |
| 0x0 | | | |
| S:cached_fps_status | 0 | cached_sts_status | 0 |
| S:cached_er_crc_good_eof | 0 | | |
| S:cached_er_bad_os | 0 | cached_er_too_long | 0 |
| S:cached_er_trunc | 0 | | |
| cached_tot_er_crc_good_eof | 0 | | |
| S:num_pt_excess_intr | 0 | num_no_fid | 0 |
| S:num_fault1_cnt | 0 | num_fault2_cnt | |
| 0 | | | |
| S:num_fault_lip | 0 | num_fault_llli | 0 |
| S:num_fault_rx_fifo | 0 | num_fault_hss | 0 |
| S:num_fault_bwait | 0 | llli_intr_prim | |
| 0 | | | |
| S:num_sw_link_to | 0 | | |
| be_link_err_mon_count | 0 | | |
| S:ecb_enc_enabled | 0 | ecb_comp_enabled | |
| 0 | | | |
| S:ecb_rsv_enc | 0 | ecb_rsv_comp | 0 |
| S:ecb_enc_bm | 0x0 | ecb_key_index | |
| 0xffffffff | | | |
| S:fab_idx | 0 | | |
| S:num_be_lto | 0 | lto_count_reset_intvl | |
| 0 | | | |
| S:lr_count_reset_intvl | 0 | num_be_lr | |
| 0 | | | |
| S:num_fault_qsfp | 0 | check_lto | |
| 0 | | | |
| S:credit_loaded | 0 | num_credit_overrun | |
| 0 | | | |
| S:fec_enabled | 0x0 | fec_los_to_flag | 0x0 |
| S:phy_stats_clear_ts | 1725611419 | pcs_err_online | |
| 0 | | | |
| S:pcs_err_light_det | 0 | pcs_err_ignore | |
| 0 | | | |
| S:pcs_blk_err | 0 | pcs_hiber | 0 |
| S:phy_port_status | 0 | ecb_enc_lr_count | |

```

0
S:dport_mode 0 avoid_lto_det 0
S:sn_debounced 0x0 sn_started_kr_reqd 0
S:major_timer_started 0x0 ready_bm 0x0
S:parln_1_bm 0x0 parln_0_bm 0x0
S:be_los_of_sync_event_intvl 0
be_los_of_sync_event 0
S:errataPtenable_cntr 0 errataPoll_cntr
0
S:jda_rx_sig_loss_det 0 jda_rx_sig_loss_cnt
0
S:encrypt_blk_error 0
S:
S: c4_trunk
S:=====
S:mark_ts 0x0 deskew 0x0
S:master_phyp 0x0
S:
S:adelay[00]: 0x00000000 0x00000000 0x00000000 0x00000000
S:adelay[04]: 0x00000000 0x00000000 0x00000000 0x00000000
S:
S: c4_buf
S:=====
S:tx_csc 0 rx_csc
0
S:ld_vc_credits 0 tx_flag 0x0
S:alloc_buffers 0 req_buffers 0
S:est_buffers 20 ld_use_est 0
S:bb_sc_n 0 rx_bb_sc_n
0
S:data_cr 5 nondata_cr
6
S:cr_enable 0
S:ld_nondata_cr 6 tnodep
0xbb8480e0
S:tx_credits[0] 0 0 0 0 0 0 0 0
S:tx_credits[8] 0 0 0 0 0 0 0 0
S:tx_credits[16] 0 0 0 0 0 0 0 0 0
S:tx_credits[24] 0 0 0 0 0 0 0 0 0
S:tx_credits[32] 0 0 0 0 0 0 0 0 0
S:rx_credits[0] 0 0 0 0 0 0 0 0
S:rx_credits[8] 0 0 0 0 0 0 0 0
S:rx_credits[16] 0 0 0 0 0 0 0 0 0
S:rx_credits[24] 0 0 0 0 0 0 0 0 0
S:rx_credits[32] 0 0 0 0 0 0 0 0 0
S:tx_mbc[0] 0 0 0 0 0 0 0 0
S:tx_mbc[8] 0 0 0 0 0 0 0 0
S:tx_mbc[16] 0 0 0 0 0 0 0 0
S:tx_mbc[24] 0 0 0 0 0 0 0 0
S:tx_mbc[32] 0 0 0 0 0 0 0 0
S:rx_mbc[0] 0 0 0 0 0 0 0 0
S:rx_mbc[8] 0 0 0 0 0 0 0 0
S:rx_mbc[16] 0 0 0 0 0 0 0 0
S:rx_mbc[24] 0 0 0 0 0 0 0 0

```

```

S:rx_mbc[32]    0    0    0    0    0    0    0    0
S:
S:C4 Chip Variables: c4_phyp->c4_chp = 0x97e28000
S:-----
-----
S:version = 2.1
S:magic_id      0xc4234567      init_state      0x8
S:reset_reg_mem 0x1
S:ch_int0_en_bm 0x0      intr0_cause     0x0
S:ch_int1_en_bm 0x0      intr1_cause     0x0
S:ch_int2_en_bm 0x0      intr2_cause     0x0
S:ch            0x43010080      ch_cfg
0xb7013ba0
S:raslog_hndl.hndl 0x0      obj_halted      0x0
S:c4_chip_regp  0x80000000      c4_fpg_regp
0x81800000
S:num_chip_timer 0x5
S:hi_task_bm    0x0      lo_task_bm      0x0
S:c4_deferq.q_head 0x0      c4_deferq.q_tail 0x0
S:c4_tmrq.q_head 0x0      c4_tmrq.q_tail  0x0
slot_no        0
S:chip_inst     0      chip_idx        0
S:pll_initialized          1
pll_serdes_initialized 1
S:init_tries     0      init_ptEnableBM
0xba01b488
S:tick_polling  0xb980c9c0      sec_polling
0xb980c960
S:bb_fid        129
S:ecb_key_bm[0] 0x0      ecb_key_bm[1]   0x0
S:ecb_key_bm[2] 0x0      ecb_key_bm[3]   0x0
S:is_chip_enc_enabled          0
is_chip_comp_enabled 0x0
S:ftb_rsrcp->ftb_flags 0x0      act_rsrcp->act_flag 0x1
S:lue_rsrcp->lue_flags[0] 0x0      lue_rsrcp-
>lue_flags[1] 0x0
S:c4_phyp[00]: 0xb6ab0000 0xb6ab2080 0xb6ab4100 0xb6ab6180
S:c4_phyp[04]: 0xb6ab9040 0xb6abb0c0 0xb6abd140 0xb6ac0000
S:c4_phyp[08]: 0xb6ac2080 0xb6ac4100 0xb6ac6180 0xb6ac9040
S:c4_phyp[12]: 0xb6acb0c0 0xb6acd140 0xb6ad0000 0xb6ad2080
S:c4_phyp[16]: 0xb6ad4100 0xb6ad6180 0xb6ad9040 0xb6adb0c0
S:c4_phyp[20]: 0xb6add140 0xb6ae0000 0xb6ae2080 0xb6ae4100
S:c4_phyp[24]: 0xb6ae6180 0xb6ae9040 0xb6aeb0c0 0xb6aed140
S:c4_phyp[28]: 0xb6af0000 0xb6af2080 0xb6af4100 0xb6af6180
S:c4_phyp[32]: 0xb6af9040 0xb6afb0c0 0xb6afd140 0xb6b00000
S:c4_phyp[36]: 0xb6b02080 0xb6b04100 0xb6b06180 0xb6b09040
S:c4_phyp[40]: 0xb6b0b0c0 0xb6b0d140 0xb6b10000 0xb6b12080
S:c4_phyp[44]: 0xb6b14100 0xb6b16180 0xb6b19040 0xb6b1b0c0
S:c4_phyp[48]: 0xb6b1d140 0xb6b20000 0xb6b22080 0xb6b24100
S:c4_phyp[52]: 0xb6b26180 0xb6b29040 0xb6b2b0c0 0xb6b2d140
S:c4_phyp[56]: 0xb6b30000 0xb6b32080 0xb6b34100 0xb6b36180
S:c4_phyp[60]: 0xb6b39040 0xb6b3b0c0 0xb6b3d140 0xb6b40000
S:c4_lgcp[00]: 0x97f48000 0x97f4c000 0x97f50000 0x97f54000
S:c4_lgcp[04]: 0x97f58000 0x97f5c000 0x97f60000 0x97f64000

```

```

S:c4_lgcp[08]: 0x97f68000 0x97f6c000 0x97f70000 0x97f74000
S:c4_lgcp[12]: 0x97f78000 0x97f7c000 0x97f80000 0x97f84000
S:c4_lgcp[16]: 0x97f88000 0x97f8c000 0x97f90000 0x97f94000
S:c4_lgcp[20]: 0x97f98000 0x97f9c000 0x97fa0000 0x97fa4000
S:c4_lgcp[24]: 0x97fa8000 0x97fac000 0x97fb0000 0x97fb4000
S:c4_lgcp[28]: 0x97fb8000 0x97fbc000 0x97fc0000 0x97fc4000
S:c4_lgcp[32]: 0x97fc8000 0x97fcc000 0x97fd0000 0x97fd4000
S:c4_lgcp[36]: 0x97fd8000 0x97fdc000 0x97fe0000 0x97fe4000
S:c4_lgcp[40]: 0x97fe8000 0x97fec000 0x97ff0000 0x97ff4000
S:c4_lgcp[44]: 0x97ff8000 0x97ffc000 0x8e000000 0x8e004000
S:c4_lgcp[48]: 0x8e008000 0x8e00c000 0x8e010000 0x8e014000
S:c4_lgcp[52]: 0x8e018000 0x8e01c000 0x8e020000 0x8e024000
S:c4_lgcp[56]: 0x8e028000 0x8e02c000 0x8e030000 0x8e034000
S:c4_lgcp[60]: 0x8e038000 0x8e03c000 0x8e040000 0x8e044000
S:chip_timers[00]: 0xb980c720 0xb980c780 0xb980c7e0 0xb980c840
S:chip_timers[04]: 0xb980c8a0 0xb980c900
S:disc_trap_enable_required      0x0          rxlp_disc_log_stop
          0x0
S:curr_rxlp_frm_cnt      0x0          curr_rxlp_disc_frm_cnt  0x0
S:sw_disc_frm_cnt      0x0          last_disc_frm_cnt      0x0
S:txq_nopop_pr_cnt      0x0          pollErrataDfe_ptBM
0xba01b4b0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][0]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][1] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][2]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][0] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][1]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][2] 0x0
S:
S:C4 Logical Port Variables
S:-----
-----
S:c4_lgc_regp      0x81cc8000
S:c4_phyp:
S:      0xb6ae9040      0x0          0x0          0x0

S:      0x0          0x0          0x0          0x0

S:master_phyp      0xb6ae9040      if_id
0x43020019
S:min_phyp      0x0          max_phyp      0x0
S:num_phy_ports      1          lgc_num      25
S:num_iu_to      0          sw_txq_bm
0
S:port_fid      128          unused      0
S:port_group      3          lgc_stats_clear_ts
1725611419
S:domain_tbl_sel      0          area_tbl_sel
0
S:egid_tbl_sel      0
S:serv_lo_bm      0x0
S:
S:Proto Phy Variables:
S:-----

```

```

-----
S:magic_id          0xc4123456      asic_phyp
0xb6ae9040
S:port_id          0x43028019      phy_cfg
      0xb6aea080
S:upsm_hdl         0xb8017dc0      physm_hdl
0xb8017b40
S:ov_sns_hdl       0xb8017a00      sw_sns_hdl
0xb8017aa0
S:ov_lks_hdl       0xb8017be0      sw_lks_hdl
0xb8017c80
S:trks_hdl         0xb8017d20      lr_flag          0x0
S:lr_active        0x0          qsf_txr_rate_sel
      0x0
S:
S:UPSM            UP00: UPST_PORT_DISABLED  --> UP01:
UPST_START_PORT_INIT
S:SNSM(OV)        SN00: OV_SNST_STOPPED      --> SN00: OV_SNST_STOPPED
S:SNSM(SW)        SW00: SW_SNST_STAGE_WS     --> SW00: SW_SNST_STAGE_WS
S:PHYSM           UNKNOWN      --> PP03: PHYST_NO_SIGNAL
S:LKSM(OV)        LK00: OV_LKST_INACTIVE     --> LK00: OV_LKST_INACTIVE
S:LKSM(SW)        SW13: INACTIVE            --> SW13: INACTIVE
S:TRKSM           TRK0: TRKST_INIT          --> TRK0: TRKST_INIT
S:
S:physm variables:
S:-----
-----
S:proto_phyp       0xb880aea0      physm_hdl
0xb8017b40
S:force_offline    0          copper          0
S:fault_reason     0: UNKNOWN
S:phy_media_present 1
S:
S:sns variables:
S:-----
-----
S:speed            0xff          proto_phyp
0xb880aea0
S:hw_sn_tries_left 0x0          sw_sn_tries_left  0x0
S:curr_txsp_count  0x0
S:tx_max           0x0          curr_tx_indx
      0x0
S:curr_tx          0x0          curr_rxsp_count
      0x0
S:rx_max           0x0          curr_rx_indx
      0x0
S:curr_rx          0x0          rx_mem
      0x0
S:rxsp_rec_count  0x0
S:nc_start         0x0          tx_start          0x0
S:sync_start       0x0          sync_present      0x0
S:diag_auto        0x0          diag_speed        0xff
S:striped_wd_tov  3000          hw_wd_tov
      3000

```

```

S:step          0x0          qsf28_speed_mode
      0x0
S:qsf28_mode0_hw_sn_tries_left    0x0
S:qsf28_mode1_hw_sn_tries_left    0x0
S:
S:lksm variables:
S:-----
-----
S:proto_phy    0xb880aea0    ov_lksm_hdl
0xb8017be0
sw_lksm_hdl    0xb8017c80
num_lf1        0
S:hw_link_tries_left    0          sw_link_tries_left    0
S:buf_ptype    0x0          stored_entry_state    0x6
S:handshake_owner    0x0          mark_unsent
      0x0
S:busybuf_stuck    0x0          lr_wait          0x0
S:
S:trksm variables:
S:-----
-----
S:Not a trunk port
S:
S:upsm variables:
S:-----
-----
S:proto_phy    0xb880aea0    upsm_hdl
0xb8017dc0
S:bb_credits    0          port_beacon          0
S:port_diag_flag    0          force_offline
      0
S:port_fault_rsn    0: PORT_NO_FAULT
S:retry_init_rsn    0: UNKNOWN
S:limit_reason    0          limit_result          0
S:ie_fctl_mode    0          fec_in_sync_tries_left    0
S:retry_sn_fail_init    0
retry_link_fail_init    0
S:excess_lr_count    0
S:
S:c4_ch_cfg
S:-----
-----
S:c4_desc_ring_size    256    292    256    256    292
292    2    292
S:thresh_def    0    16    1    0
S:intr_tries    500          cmem_pattern
0xdeadbeef
S:cmem_pattern_upwd    2          cmem_init_time          16
S:cmem_init_tries    5
S:ctrl_par_thresh    2          data_par_thresh
4
S:cam_par_thresh    4          buf_loss_thresh
12
S:crit_par_thresh    2          non_crit_par_thresh

```

```

        6
S:pci_abort_thresh      10          pci_err_thresh      5
S:excess_chintr_thresh  8          sw_err_thresh      20
S:err_sample_period    300        intr_sleep
20000
S:frame_timeout        2500        proxy_dev          16384
S:vf_route             81920       qos                2048
S:stats                2048        f_redirect         2048
S:rsp_trap             2048        lun_zoning         20480
S:area_mode            0          ftb_max_loop[0]   0
S:ftb_max_loop[1]     6          ftb_max_loop[2]   9
S:ftb_max_loop[3]    10          ftb_max_loop[4]  10
S:ftb_max_loop[5]     5          ftb_max_loop[6]   6
S:ftb_seg_size[0]     0          ftb_seg_size[1]  16384
S:ftb_seg_size[2]    65536       ftb_seg_size[3]  16384
S:ftb_seg_size[4]    16384       ftb_seg_size[5]  65536
S:ftb_seg_size[6]    16384       ftb_seg_base[0]  0
S:ftb_seg_base[1]    0          ftb_seg_base[2]  65536
S:ftb_seg_base[3]    16384       ftb_seg_base[4]  32768
S:ftb_seg_base[5]    131072      ftb_seg_base[6]  49152
asic_err_monitor_period1 300
asic_err_monitor_period2 86400
zone_chk_to_poll_period 25
zone_chk_class2_reject_tov 220
S:
S:c4_phy_cfg
S:-----
-----
S:version = 2.1
S:pt                   0x43028019      fab_ptr
0x9a800000
S:fabattr              0x9a8000d4      fab_iop
0x9a800050
S:cfgbm                0xbb847e04      port_ctrl
0xb6aea098
S:pcap.pcap_bm         0x8d215547      pcap.pcap2_bm
0x588289
S:pcap.pcap3_bm        0x1bebe0c
ui_idx                 39              S:slot_no
0
is_icl                 0              S:sw_usr_ports   400
S:neg_speed            0 0 0 0 0 0
S:my_domain            0x1             port_mode         0x0
S:hw_sn_maxtries      100            sw_sn_maxtries
0
S:hw_link_maxtries    10             sw_link_maxtries 5
S:rx_cyc_tov          28             rttov            300
S:bufrdy_tov          300            busybuf_tov      286

```

```

S:mark_tov          300          lksm_tov           3000
S:buf_dealloc_wait  4           hw_wd_tov          3000
S:hw_lk_train_tov   540          hw_lk_test_tov
    150
S:syswait_tx_12_lips 1           lip_rx_tov         55
S:al_time_tov       15          lp_tov             2000
S:intr_tries_port   500          intr_mod_debounce
    250
S:intr_lsrflt_debounce 500        intr_efifo_debounce 100
S:port_no_fid       3           excess_ptintr_thresh 8
S:port_fault1_thresh 100        port_fault1_spur_thresh 250
S:port_fault1_disc_thresh 500
port_fault1_disc_spur_thresh 1000
S:port_fault2_thresh 5           losync_tov         100
S:port_sw_link_to   15          en_8g_scramble
    1
frc_hw_sn_mode      0x1
S:enc_poll_thresh   0           fec_enable
    0
S:fec_in_sync_to    50          fec_in_sync_try_max
    4
S:port_be_lto_threshold 100        port_be_lr_threshold
    2
S:be_cr_in_sync_to  5
port_credit_overrun_thresh 10
S:jda_sfp_losig_tov 400
jda_sfp_losig_try_max 30
S:striped_wd_tov    3000
no_sync_debounce    1200
S:
S:    fab_iop
S:=====
S:fab_iop->interop_mode 0x0        fab_iop->lab_mode    0x0
S:fab_iop->fl_bbc      0x0          fab_iop->fl_fan
    0x0
S:fab_iop->fl_cls      0x4          fab_iop->fl_rscn
    0x0
S:fab_iop->domain_id_offset 0x60        fab_iop-
>mcdt_fabric_mode    0x0
S:fab_iop->mcdt_default_zone 0x0          fab_iop-
>mcdt_safe_zone      0x0
S:
S:    port_ctrl
S:=====
S:port_ctrl.port_type 1           port_ctrl.port_grp  3
S:port_ctrl.port_number 39        port_ctrl.vc_mode    1
S:
S:    port_ctrl.lcap
S:=====
S:has_serdes         0           has_media           1
S:topology           1           skip_nego           0
S:skip_pnego         0           skip_init_event     0
S:en_shim            0           speed_neg
    1

```



```

S:loop_back          0          num_speeds          5
S:fec_enable         0
S:
S:    port_ctrl.speed_list array
S:=====
S:speed_list[0].auto_neg  1    speed_list[0].lnk_speed  0x0000000a
S:speed_list[1].auto_neg  1    speed_list[1].lnk_speed  0x00000008
S:speed_list[2].auto_neg  0    speed_list[2].lnk_speed  0x00000006
S:speed_list[3].auto_neg  1    speed_list[3].lnk_speed  0x00000005
S:speed_list[4].auto_neg  0    speed_list[4].lnk_speed  0x00000003
S:speed_list[5].auto_neg  0    speed_list[5].lnk_speed  0x00000000
S:
S:    port_ctrl.cm
S:=====
S:port_ctrl.cm.num_vcs          8
S:port_ctrl.cm.min_bufs        8
S:port_ctrl.cm.cr_shar_bufs    0
S:port_ctrl.vc_alloc
S:port_ctrl.vc_alloc          2 0 1 1 1 1 1 1
S:port_ctrl.vc_alloc          0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.norm_vc_alloc
S:port_ctrl.norm_vc_alloc      4 0 5 5 5 5 1 1
S:port_ctrl.norm_vc_alloc      0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.cm.skip_bb_credit          0
S:port_ctrl.cm.use_shim_based_sublist          0
S:
S:    port_ctrl.serdes_set
S:=====
S:serdes_type          0x8
S:serdes_data_t.ibm_hss_serdes.tx_drive_power          0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b_sign      0x1
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b          0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_a          0x0
S:serdes_data_t.ibm_hss_serdes.rxeq                    0x0
S:
S:    cfgbm
S:=====
S:old_distance          0x0          gport_lockdown          0x0
S:tport                0x1          speed                    0x0
S:disable_eport        0x0          fcacc                    0x0
S:lport_lockdown       0x0          0x0          priv_lport_lockdown
0x0
S:vcxlt_linit          0x0          delay_flogi              0x0
S:isl_interop          0x0          distance                  0x0
S:BufStarvFlag         0x0          credit_sharing            0x0
S:lport_halfduplex     0x0          lport_fairness            0x0
S:soft_neg             0x0          asn_frc_hwretry           0x0
S:cr_recov             0x0          fport_buffers             0x0
S:export               0x0          0x0          export_mode
0x0
S:csctl_en             0x0          mirror_port               0x0
S:fault_delay          0x0          non_dfe                   0x0

```

```

S: fec_configured*(0=ENAB)      0      fec_tts
  0
S: port_persistently_disabled (permanently) 0 (0)
S:
S:      cfg property
S:=====
S:priv_pcfg_bm      0x00000000      lgcl_pcfg_bm
0xbb847e44
S:fport_buffer      0x00000000
S:
S:
S:C4 Discard Cntrs: rxlp_stats = 0xb6ae93f0
S:-----
-----
S:disc_mcast_wka      0x0      disc_inv_did      0x0
S:disc_cl1_cl4      0x0      disc_sid_chk_fail      0x0
S:disc_inv_dom_egid_txpt      0x0      disc_vft_hop_cnt_1
0x0
S:disc_classf      0x0      disc_fcp_cdb_inv      0x0
S:disc_vfid_trap_enabled      0x0
disc_vfid_hdr_chk_fail 0x0
S:disc_shim_cksum_fail 0x0      disc_fed_edit_cmd_err      0x0
S:disc_shim_cksum_fail 0x0      disc_fed_edit_cmd_err      0x0
S:disc_ftb_vm_mode      0x0      disc_ftb_agnt2_miss      0x0
S:disc_ecb_de_pad_err      0x0      disc_ecb_de_tag_err      0x0
S:disc_ecb_de_seq_err      0x0      disc_ecb_err      0x0
S:disc_ftb_type4_match 0x0      disc_fcp_rsp_ftb_type4      0x0
S:disc_fcp_rsp_ftb_type4      0x0      disc_ftb_type5_match
0x0
S:disc_ftb_type3_match 0x0      disc_els_ftb_type3      0x0
S:disc_ftb_type1_match 0x0      disc_els_rsp_ex_port      0x0
S:disc_inv_drp_dps      0x0      disc_did_lookup_miss      0x0
S:disc_ftb_type2_match 0x0      disc_trpd_plogi_pdisc      0x0
S:disc_type2_lookup_miss      0x0      disc_ftb_type6_match
0x0
S:disc_els_rep_ex_port 0x0      disc_els_sid_lkup_bit1      0x0
S:disc_els_sid_lkup_bit0      0x0
disc_bls_frm_trap_bit1 0x0
S:disc_ftb_token_err      0x0      disc_asic_internal_err      0x0
S:disc_hard_zone_miss      0x0      disc_lun_zone_miss      0x0
S:disc_flt_frame_disc      0x0      disc_flt_parity_err      0x0
S:disc_frame_marked_du      0x0      disc_frame_marked_to      0x0
E:Connection type: FE
E:Port type: F_port
E:Trunk port: No
E:Configured Speed: AUTO_SPEED_NEGO
E:Max Capable Speed: 32G
E:Current SNSM Speed: UNDEFINED
E:Hardware TX Speed: 32G (0x00000004)
E:Hardware RX Speed: 32G (0x00000040)
E:
E:Interrupts:      0      Link_failure:      0
Loss_of_sync:      0      Loss_of_sig:      0
E:Lli:      0      Invalid_word:      0

```

| | | | |
|-------------------|---|------------------|---|
| E:trapped_frm: | 0 | fwd_status_ok: | 0 |
| E:fwd_timeout: | 0 | fwd_tx_unavail: | 0 |
| E:fwd_unroutable: | 0 | fwd_zone_out: | 0 |
| E:fwd_other_err: | 0 | frm_err_discard: | 0 |
| E:Fltr listA: | 0 | Fltr listB: | 0 |
| E:Zone trap fwd: | 0 | Zone trap disc: | 0 |
| E:shim_csum: | 0 | RTE_perr: | 0 |
| E:Invalid_crc: | 0 | Delim_err: | 0 |
| E:Protocol_err: | 0 | | |
| E:Lr_in: | 0 | Lr_out: | 0 |
| E:Ols_in: | 0 | Ols_out: | 0 |

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FILTER DATA

Shadow settings:

```

Filter Enable: 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass: 0x00000000

```

Real settings:

```

Enable RAM: 0x00000000, 0x00000000

```

Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass RAM: 0x00000000

Shadowed filters:

Filter 0: Not Installed (MIRROR1)(LISTA)
c4_fldenable[0] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[0] = 0x00000000,c4_fltr_config[0] = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
c4_fldenable[1] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[1] = 0x00000000,c4_fltr_config[1] = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
c4_fldenable[2] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[2] = 0x00000000,c4_fltr_config[2] = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
c4_fldenable[3] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[3] = 0x00000000,c4_fltr_config[3] = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
c4_fldenable[4] = 0x00000000 0x00000000 0x00000000

```
0x00000000
    c4_fldnegate[4] = 0x00000000,c4_fltr_config[4] = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
    c4_fldenable[5] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[5] = 0x00000000,c4_fltr_config[5] = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
    c4_fldenable[6] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[6] = 0x00000000,c4_fltr_config[6] = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
    c4_fldenable[7] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[7] = 0x00000000,c4_fltr_config[7] = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
    c4_fldenable[8] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[8] = 0x00000000,c4_fltr_config[8] = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
    c4_fldenable[9] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[9] = 0x00000000,c4_fltr_config[9] = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
    c4_fldenable[10] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[10] = 0x00000000,c4_fltr_config[10] =
0x00000000
Filter 11: Not Installed (SIM)(LISTA)
    c4_fldenable[11] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[11] = 0x00000000,c4_fltr_config[11] =
0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
    c4_fldenable[12] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[12] = 0x00000000,c4_fltr_config[12] =
0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
    c4_fldenable[13] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[13] = 0x00000000,c4_fltr_config[13] =
0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
    c4_fldenable[14] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[14] = 0x00000000,c4_fltr_config[14] =
0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
    c4_fldenable[15] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[15] = 0x00000000,c4_fltr_config[15] =
0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
    c4_fldenable[16] = 0x00000000 0x00000000 0x00000000
```

```
0x00000000
    c4_fldnegate[16] = 0x00000000,c4_fltr_config[16] =
0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
    c4_fldenable[17] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[17] = 0x00000000,c4_fltr_config[17] =
0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
    c4_fldenable[18] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[18] = 0x00000000,c4_fltr_config[18] =
0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
    c4_fldenable[19] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[19] = 0x00000000,c4_fltr_config[19] =
0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
    c4_fldenable[20] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[20] = 0x00000000,c4_fltr_config[20] =
0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
    c4_fldenable[21] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[21] = 0x00000000,c4_fltr_config[21] =
0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
    c4_fldenable[22] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[22] = 0x00000000,c4_fltr_config[22] =
0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
    c4_fldenable[23] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[23] = 0x00000000,c4_fltr_config[23] =
0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
    c4_fldenable[24] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[24] = 0x00000000,c4_fltr_config[24] =
0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
    c4_fldenable[25] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[25] = 0x00000000,c4_fltr_config[25] =
0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
    c4_fldenable[26] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[26] = 0x00000000,c4_fltr_config[26] =
0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
```

```
    c4_fldenable[27] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[27] = 0x00000000,c4_fltr_config[27] =
0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
    c4_fldenable[28] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[28] = 0x00000000,c4_fltr_config[28] =
0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
    c4_fldenable[29] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[29] = 0x00000000,c4_fltr_config[29] =
0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    c4_fldenable[30] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[30] = 0x00000000,c4_fltr_config[30] =
0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    c4_fldenable[31] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[31] = 0x00000000,c4_fltr_config[31] =
0x00000000
```

Real filters:

```
Filter 0: Not Installed (MIRROR1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
```

0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 11: Not Installed (SIM)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 20: Not Installed (PERF5)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter dirty indicator: 0x00000000
Performance filters: 0
Port Mirror filters: 0 (0x0)

FIELD DATA

Shadowed fields:

```
fldoffset[0] = 0x00, fldmask[0] = 0x00, fldvalue_dyna[0]:0x00 0x00
0x00 0x00
fldcontrol[0].inuse = 0x0  fldcontrol[0].refcnt = 0x00 0x00 0x00
0x00
fldoffset[1] = 0x00, fldmask[1] = 0x00, fldvalue_dyna[1]:0x00 0x00
0x00 0x00
fldcontrol[1].inuse = 0x0  fldcontrol[1].refcnt = 0x00 0x00 0x00
0x00
fldoffset[2] = 0x00, fldmask[2] = 0x00, fldvalue_dyna[2]:0x00 0x00
0x00 0x00
fldcontrol[2].inuse = 0x0  fldcontrol[2].refcnt = 0x00 0x00 0x00
0x00
fldoffset[3] = 0x00, fldmask[3] = 0x00, fldvalue_dyna[3]:0x00 0x00
0x00 0x00
fldcontrol[3].inuse = 0x0  fldcontrol[3].refcnt = 0x00 0x00 0x00
0x00
fldoffset[4] = 0x00, fldmask[4] = 0x00, fldvalue_dyna[4]:0x00 0x00
0x00 0x00
fldcontrol[4].inuse = 0x0  fldcontrol[4].refcnt = 0x00 0x00 0x00
0x00
fldoffset[5] = 0x00, fldmask[5] = 0x00, fldvalue_dyna[5]:0x00 0x00
0x00 0x00
fldcontrol[5].inuse = 0x0  fldcontrol[5].refcnt = 0x00 0x00 0x00
0x00
fldoffset[6] = 0x00, fldmask[6] = 0x00, fldvalue_dyna[6]:0x00 0x00
0x00 0x00
fldcontrol[6].inuse = 0x0  fldcontrol[6].refcnt = 0x00 0x00 0x00
0x00
fldoffset[7] = 0x00, fldmask[7] = 0x00, fldvalue_dyna[7]:0x00 0x00
0x00 0x00
fldcontrol[7].inuse = 0x0  fldcontrol[7].refcnt = 0x00 0x00 0x00
0x00
fldoffset[8] = 0x00, fldmask[8] = 0x00, fldvalue_dyna[8]:0x00 0x00
0x00 0x00
fldcontrol[8].inuse = 0x0  fldcontrol[8].refcnt = 0x00 0x00 0x00
0x00
fldoffset[9] = 0x00, fldmask[9] = 0x00, fldvalue_dyna[9]:0x00 0x00
0x00 0x00
fldcontrol[9].inuse = 0x0  fldcontrol[9].refcnt = 0x00 0x00 0x00
0x00
fldoffset[10] = 0x00, fldmask[10] = 0x00, fldvalue_dyna[10]:0x00 0x00
0x00 0x00
fldcontrol[10].inuse = 0x0  fldcontrol[10].refcnt = 0x00 0x00 0x00
0x00
fldoffset[11] = 0x00, fldmask[11] = 0x00, fldvalue_dyna[11]:0x00 0x00
0x00 0x00
fldcontrol[11].inuse = 0x0  fldcontrol[11].refcnt = 0x00 0x00 0x00
0x00
fldoffset[12] = 0x00, fldmask[12] = 0x00, fldvalue_dyna[12]:0x00 0x00
```


0x00000000
0x00000000
0x00000000
0x00000000
0x00000000

Field dirty indicator: 0x00000000

FDB reference count fdb: 0 [0 0 0 0]
FDB reference count fdb: 1 [0 0 0 0]
FDB reference count fdb: 2 [0 0 0 0]
FDB reference count fdb: 3 [0 0 0 0]
FDB reference count fdb: 4 [0 0 0 0]
FDB reference count fdb: 5 [0 0 0 0]
FDB reference count fdb: 6 [0 0 0 0]
FDB reference count fdb: 7 [0 0 0 0]
FDB reference count fdb: 8 [0 0 0 0]
FDB reference count fdb: 9 [0 0 0 0]
FDB reference count fdb: 10 [0 0 0 0]
FDB reference count fdb: 11 [0 0 0 0]
FDB reference count fdb: 12 [0 0 0 0]
FDB reference count fdb: 13 [0 0 0 0]
FDB reference count fdb: 14 [0 0 0 0]
FDB reference count fdb: 15 [0 0 0 0]
FDB reference count fdb: 16 [0 0 0 0]
FDB reference count fdb: 17 [0 0 0 0]
FDB reference count fdb: 18 [0 0 0 0]
FDB reference count fdb: 19 [0 0 0 0]

Filter counters:

Filter counter 0: 0 (MIRROR1)
Filter counter 1: 0 (MIRROR2)
Filter counter 2: 0 (MIRROR3)
Filter counter 3: 0 (MIRROR4)
Filter counter 4: 0 (AEPORT_NON_MIRR_DROP)
Filter counter 5: 0 (ZONING TRAP)
Filter counter 6: 0 (FCR_EXPORT_DC)
Filter counter 7: 0 (TIN TRAP)
Filter counter 8: 0 (FICON CUP)
Filter counter 9: 0 (FICON CUP DST)
Filter counter 10: 0 (WELL KNOWN ADDR)
Filter counter 11: 0 (SIM)
Filter counter 12: 0 (UNUSED)
Filter counter 13: 0 (UNUSED)
Filter counter 14: 0 (UNUSED)
Filter counter 15: 0 (UNUSED)
Filter counter 16: 0 (PERF1)
Filter counter 17: 0 (PERF2)
Filter counter 18: 0 (PERF3)
Filter counter 19: 0 (PERF4)
Filter counter 20: 0 (PERF5)
Filter counter 21: 0 (PERF6)
Filter counter 22: 0 (PERF7)
Filter counter 23: 0 (PERF8)
Filter counter 24: 0 (PERF9)

Filter counter 25: 0 (PERF10)
Filter counter 26: 0 (PERF11)
Filter counter 27: 0 (PERF12)
Filter counter 28: 0 (OPM1)
Filter counter 29: 0 (OPM2)
Filter counter 30: 0 (IPM1)
Filter counter 31: 0 (IPM2)

ACL DATA

Logical port 25: Hard Zoning disabled, Soft Zoning disabled
Zone type: WWN Zoning
Frames with hard zone miss: 0

*** Please use filterportshow on user port 56 to display ACL hash tables and Mirroring resources of thischip.
***We show this data only for the first physical port which is an external port.

portFcPortCmdShow --slot 0 40 3
doing portFcPortCmdShow: arg1 = 3, arg2 = -2

portshow 40
portDisableReason: None
portCFlags: 0x1
portFlags: 0x1 PRESENT U_PORT
LocalSwcFlags: 0x0
portType: 26.0
POD Port: Port is licensed
portState: 2 Offline
Protocol: FC
portPhys: 4 No_Light portScn: 2 Offline
port generation number: 0
state transition count: 1

portId: 012800
portIfId: 43020016
portWwn: 20:28:d8:1f:cc:2c:99:90
portWwn of device(s) connected:
16b Area list:
Distance: normal
portSpeed: N32Gbps

FEC: Inactive
Credit Recovery: Inactive
LE domain: 0
Peer beacon: Off
FC Fastwrite: OFF

| | | | | |
|-------------|---|---------------|---|-------|
| Interrupts: | 0 | Link_failure: | 0 | Frjt: |
| 0 | | | | |
| Unknown: | 0 | Loss_of_sync: | 0 | Fbsy: |
| 0 | | | | |
| Lli: | 0 | Loss_of_sig: | 0 | |
| Proc_rqrd: | 0 | Protocol_err: | 0 | |

```

Timed_out:      0          Invalid_word: 0
Tx_unavail:    0          Invalid_crc:  0
Delim_err:     0          Address_err:  0
Lr_in:         0          0ls_in:     0
Lr_out:        0          0ls_out:    0

```

portloginshow 40

```

Type  PID      World Wide Name      credit df_sz cos
=====

```

portloginshow 40 -history

```

Type  PID      World Wide Name      logout time
=====

```

portregshow 40

LED registers

=====

```

0x81cb2000: c4_led_status      00000000      0x81cb2004:
c4_led_ctl      00000000

```

FPL registers

=====

```

0x81cb0200: fpl_port_config      23298002
0x81cb020c: fpl_port_id_ctl      00000000      0x81cb0210:
fpl_port_id_addr      00012800
0x81cb0214: fpl_port_speed      00000004      0x81cb021c:
fpl_lli_ctl      00000100
0x81cb0228: fpl_lli_os_ctl      bc94ffff      0x81cb022c:
fpl_lli_send_word      bc95b5b5
0x81cb0230: fpl_lli_mark_rx      00000000      0x81cb0234:
fpl_lli_rnd_trip_time      00000000
0x81cb0238: fpl_lli_ns_status      00130007      0x81cb023c:
fpl_lli_intr_status      00030007
0x81cb0244: fpl_lli_def      00100000      0x81cb0254:
fpl_lli_intr_enable_clr      001c0000
0x81cb0258: fpl_err_intr_status      00000000      0x81cb0260:
fpl_err_intr_enable_clr      00000000
0x81cb0268: fpl_err_first_error      00000000      0x81cb026c:
fpl_speed_neg_ctl      00000000
0x81cb0270: fpl_speed_neg_stat      00000000      0x81cb0274:
fpl_softasn_ctl      0000000f
0x81cb0278: fpl_link_init_ctl      00000000      0x81cb027c:
fpl_link_init_stat      00000000
0x81cb0280: fpl_aec_ctl      001c1060      0x81cb0284:
fpl_aec_ctl2      04009f60
0x81cb0288: fpl_pcs_ctl      00000170      0x81cb028c:
fpl_fec_ctl      00000424
0x81cb0290: fpl_fec_cor      00000000      0x81cb0294:
fpl_fec_uncor      00000000
0x81cb0298: fpl_hss_link_ctl      0031f040      0x81cb029c:

```

```

fpl_afifo_link_ctl      00000a86
0x81cb02a0: fpl_echo_lb_ctl      0000028c      0x81cb02a4:
fpl_scratch            00000121
0x81cb02a8: fpl_debug              00060005      0x81cb02ac:
fpl_misc_debug         00000800
0x00000000: SW_shadow_reg            00000000      0x00000000:
SW_c4_phyp->cfgptr     00030003

```

per-fpg (per octet) registers

```

=====
0x8181382c: fpg_serdes_ctla0      81a37be7      0x81813830:
fpg_serdes_ctla1      81a37be7
0x81813834: fpg_serdes_ctlb0      81a1c3c3      0x81813838:
fpg_serdes_ctlb1      81a1c3c3
0x8181383c: fpg_serdes_xgmii_1ms 00067c28      0x81813840:
fpg_serdes_regtimctl  40e47946
0x81813844: fpg_serdes_asnrsttimctl 00000102

```

HSS PLL registers

```

=====
0x81813400: 00_hssplla_vco_coarse_cal0      00000000      0x81813404:
01_hssplla_vco_coarse_cal1      00000014
0x81813408: 02_hssplla_vco_coarse_cal2      00000000      0x8181340c:
03_hssplla_vco_coarse_cal3      00000000
0x81813410: 04_hssplla_vco_coarse_cal4      00000000      0x81813424:
09_hssplla_power_ctl            00000000
0x81813428: 0A_hssplla_charge_pump_ctl      00000004      0x81813438:
0E_hssplla_pll_misc_ctl        00000000
0x8181343c: 0F_hssplla_pclk_ctl              000000f8      0x81813440:
10_hssplla_eyem_intv_ctl        00000000
0x81813444: 11_hssplla_eyem_intv_lim1          00000000      0x81813448:
12_hssplla_eyem_intv_lim2        00000000
0x8181344c: 13_hssplla_eyem_intv_lim3          00000000      0x81813450:
14_hssplla_eyem_intv_lim4        00000000
0x818134f0: 3C_hssplla_macro_tst_ctl4          00000000      0x818134f4:
3D_hssplla_macro_tst_ctl3        00000000
0x818134f8: 3E_hssplla_macro_tst_ctl2          00000000      0x818134fc:
3F_hssplla_macro_tst_ctl1        00000000
0x81813500: 00_hssppll_vco_coarse_cal0          0000000a      0x81813504:
01_hssppll_vco_coarse_cal1        00000014
0x81813508: 02_hssppll_vco_coarse_cal2          00000000      0x8181350c:
03_hssppll_vco_coarse_cal3        00000000
0x81813510: 04_hssppll_vco_coarse_cal4          00000000      0x81813524:
09_hssppll_power_ctl            00000000
0x81813528: 0A_hssppll_charge_pump_ctl          00000004      0x81813538:
0E_hssppll_pll_misc_ctl          00000000
0x8181353c: 0F_hssppll_pclk_ctl              000000f8      0x81813540:
10_hssppll_eyem_intv_ctl        00000000
0x81813544: 11_hssppll_eyem_intv_lim1          00000000      0x81813548:
12_hssppll_eyem_intv_lim2        00000000
0x8181354c: 13_hssppll_eyem_intv_lim3          00000000      0x81813550:
14_hssppll_eyem_intv_lim4        00000000
0x818135f0: 3C_hssppll_macro_tst_ctl4          00000000      0x818135f4:
3D_hssppll_macro_tst_ctl3        00000000

```

0x818135f8: 3E_hsspllb_macro_tst_ctl2 00000000 0x818135fc:
3F_hsspllb_macro_tst_ctl1 00000000

HSS TX registers

=====

0x81812400: 00_hsstx_cfg_mode_PHY 00009f48 0x81812404:
01_hsstx_test_ctl 00000000
0x81812408: 02_hsstx_coeff_ctl_INV 00000000 0x8181240c:
03_hsstx_drv_mode_ctl 00000000
0x81812410: 04_hsstx_drv_ovrd_ctl 00000010 0x81812414:
05_hsstx_dclk_align_ovrd 00000080
0x81812418: 06_hsstx_imp_cal_ovrd 00000c0c 0x8181241c:
07_hsstx_dclk_drift_tol 00000004
0x81812420: 08_hsstx_tap0_coeff_TUNE 00000000 0x81812424:
09_hsstx_tap1_coeff_TUNE 00000003
0x81812428: 0A_hsstx_tap2_coeff_TUNE 00000019 0x8181242c:
0B_hsstx_tap3_coeff_TUNE 00000003
0x81812434: 0D_hsstx_pol_INV 0000000a 0x81812438:
0E_hsstx_ae_cmd 00000000
0x8181243c: 0F_hsstx_ae_stat 00000000 0x81812440:
10_hsstx_ae_tap0_TUNE 00000000
0x81812444: 11_hsstx_ae_tap1_TUNE 00000000 0x81812448:
12_hsstx_ae_tap2_TUNE 00000028
0x8181244c: 13_hsstx_ae_tap3_TUNE 00000000 0x81812454:
15_hsstx_app_tune 0000120e
0x81812458: 16_hsstx_analog_diag 00000000 0x81812460:
18_hsstx_4x_seg_app 0000aa00
0x81812464: 19_hsstx_2x_seg_app 000000aa 0x81812468:
1A_hsstx_1x_seg_app 0000f5e4
0x8181246c: 1B_hsstx_seg_4x_term_app 0000000f 0x81812470:
1C_hsstx_seg_2x1x_term_app 00000001
0x81812474: 1D_hsstx_tap_sign_app 0000000a 0x81812478:
1E_hsstx_ext_addr_data 00000001
0x8181247c: 1F_hsstx_ext_addr_addr 00000000 0x81812480:
20_hsstx_pat_buf_bytes_1_0 00000000
0x81812484: 21_hsstx_pat_buf_bytes_3_2 00000000 0x81812488:
22_hsstx_pat_buf_bytes_5_4 00000000
0x8181248c: 23_hsstx_pat_buf_bytes_7_6 00000000 0x8181249c:
27_hsstx_8023az_ctl 00000000
0x818124a0: 28_hsstx_dcc_ctl 000060c0 0x818124a4:
29_hsstx_dcc_ovrd 00000000
0x818124a8: 2A_hsstx_dcc_app 00000101 0x818124ac:
2B_hsstx_dcc_timeout 0000ffff
0x818124c0: 30_hsstx_tap_sign_ovrd 00000000 0x818124c8:
32_hsstx_seg_4x_ovrd 00000000
0x818124cc: 33_hsstx_seg_2x_ovrd 00000000 0x818124d0:
34_hsstx_seg_1x_ovrd 00000000
0x818124d8: 36_hsstx_tap_seg_4x_term_ovrd 00000000 0x818124dc:
37_hsstx_tap_seg_2x_term_ovrd 00000000
0x818124e0: 38_hsstx_tap_seg_1x_term_ovrd 00000000 0x818124ec:
3B_hsstx_mac_test_ctl5 00000000
0x818124f0: 3C_hsstx_mac_test_ctl4 00000000 0x818124f4:
3D_hsstx_mac_test_ctl3 00000000
0x818124f8: 3E_hsstx_mac_test_ctl2 00000000 0x818124fc:

3F_hsstx_mac_test_ctl1 000000c6

HSS RX registers

=====

| | | |
|---|----------|-------------|
| 0x81812600: 00_hssrx_cfg_mode_PHY | 00009e78 | 0x81812604: |
| 01_hssrx_test_ctl 00000000 | | |
| 0x81812608: 02_hssrx_phs_rot_ctl | 0000cb80 | 0x8181260c: |
| 03_hssrx_phs_rot_ofs_ctl 00005610 | | |
| 0x81812610: 04_hssrx_phs_rot_posn1 | 00001513 | 0x81812614: |
| 05_hssrx_phs_rot_posn2 0000003f | | |
| 0x81812618: 06_hssrx_phs_rot_sta_ofs1 | 00000001 | 0x8181261c: |
| 07_hssrx_phs_rot_sta_ofs2 0000001f | | |
| 0x81812620: 08_hssrx_dfe_ctl_PHY | 00002002 | 0x81812624: |
| 09_hssrx_dfe_smpl_snap1 00000000 | | |
| 0x81812628: 0A_hssrx_dfe_smpl_snap2 | 00008000 | 0x8181262c: |
| 0B_hssrx_vga_ctl1 00004001 | | |
| 0x81812630: 0C_hssrx_vga_ctl2 | 00007aa0 | 0x81812634: |
| 0D_hssrx_vga_ctl3 000009e4 | | |
| 0x81812638: 0E_hssrx_pwr_mgmt_ctl | 0000001f | 0x8181263c: |
| 0F_hssrx_iqamp_ctl1 00000018 | | |
| 0x81812640: 10_hssrx_iqamp_ctl2 | 00000004 | 0x81812644: |
| 11_hssrx_dacap_dacan_sel 00000003 | | |
| 0x81812648: 12_hssrx_dacap_dacan | 0000ffff | 0x8181264c: |
| 13_hssrx_daca_min 00000000 | | |
| 0x81812650: 14_hssrx_adac_ctl | 00000000 | 0x81812654: |
| 15_hssrx_ac_cp_ctl 000031c3 | | |
| 0x81812658: 16_hssrx_ac_cp_val | 0000004c | 0x8181265c: |
| 17_hssrx_dfe_h1h2h3_lcl_off_ch 00000014 | | |
| 0x81812660: 18_hssrx_dfe_h1h2h3_lcl_off_val | 00000000 | 0x81812664: |
| 19_hssrx_peaked_intg 000000ff | | |
| 0x81812668: 1A_hssrx_cdr_analog_sw | 0000ce00 | 0x8181266c: |
| 1B_hssrx_peaking_amp_init_c_PHY 00000000 | | |
| 0x81812670: 1C_hssrx_dac_dpc | 00000040 | 0x81812674: |
| 1D_hssrx_ddc 00000000 | | |
| 0x81812678: 1E_hssrx_int_stat_PHY | 00000c0f | 0x8181267c: |
| 1F_hssrx_dfe_func_ctl1_PHY 0000ffff | | |
| 0x81812680: 20_hssrx_dfe_func_ctl2_INV | 00007eff | 0x81812684: |
| 21_hssrx_ofs_ch_dcc_qcc_idx 00002000 | | |
| 0x81812688: 22_hssrx_dfe_ofs_val | 00000301 | 0x8181268c: |
| 23_hssrx_h_coeff_bist 0000040f | | |
| 0x81812690: 24_hssrx_ac_cap_bist | 000000b3 | 0x81812694: |
| 25_hssrx_max_gain_path_idx_res 00007800 | | |
| 0x81812698: 26_hssrx_loff_ctl | 00000040 | 0x8181269c: |
| 27_hssrx_sigdet_ctl 00004e80 | | |
| 0x818126a0: 28_hssrx_ana_ctl_sw | 00000000 | 0x818126a4: |
| 29_hssrx_intg_dac_ofs 0000dde6 | | |
| 0x818126a8: 2A_hssrx_eye_ctl | 00000000 | 0x818126ac: |
| 2B_hssrx_eye_met 00000004 | | |
| 0x818126b0: 2C_hssrx_eye_met_err_cnt | 00000000 | 0x818126b4: |
| 2D_hssrx_eye_met_pdf_eyec 00000000 | | |
| 0x818126b8: 2E_hssrx_eye_met_pat_len | 0000007f | 0x818126bc: |
| 2F_hssrx_dfe_func_ctl3 0000dfff | | |
| 0x818126c0: 30_hssrx_dfe_tap_ctl_idx_ptr | 00000008 | 0x818126c4: |
| 31_hssrx_dfe_tap 00003030 | | |

```

0x818126c8: 32_hssrx_lte_ctl_TUNE          00000600    0x818126e4:
39_hssrx_int_stat2                0000c1ff
0x818126e8: 3A_hssrx_ac_cpl_cur_src_adj      00000041    0x818126ec:
3B_hssrx_dcd_ctl                   00007c4a
0x818126f0: 3C_hssrx_dcc_ctl                 00000d81    0x818126f4:
3D_hssrx_qcc_ctl                   00006985
0x818126f8: 3E_hssrx_mac_test_ctl2           00000000    0x818126fc:
3F_hssrx_mac_test_ctl1             00000000
0x81812648: 12_hssrx_dacap_dacan[02]         00ff ffff
0x81812660: 18_hssrx_dfe_h1h2h3_lcl_off_va[00] 0000 0000    0000
0000 0000 0000 0000 0000
0x81812660: 18_hssrx_dfe_h1h2h3_lcl_off_va[08] 0000 0000    0000
0000 0000 0000 0000 0000
0x81812660: 18_hssrx_dfe_h1h2h3_lcl_off_va[16] 0000 0000    0000
0000 0000
0x81812688: 22_hssrx_dfe_ofs_val[00][00]      0301 0000    7f07
007f 7f7f 0000
0x81812688: 22_hssrx_dfe_ofs_val[03][00]      7e7d 0000    0701
0000 7b7d 0000
0x81812688: 22_hssrx_dfe_ofs_val[06][00]      010a 007f    017f
0000 7f05 0000
0x81812688: 22_hssrx_dfe_ofs_val[09][00]      7d79 0000    7901
0000 7b7a 0000
0x81812688: 22_hssrx_dfe_ofs_val[12][00]      7b7d 0000    7d00
0000 7d00 0000
0x81812688: 22_hssrx_dfe_ofs_val[15][00]      7e01 0000    0206
0000 037f 0000
0x81812688: 22_hssrx_dfe_ofs_val[18][00]      0309 0000    7d7f
0000 0001 007f
0x81812688: 22_hssrx_dfe_ofs_val[21][00]      0001 007f    0001
007f 0001 007f
0x81812688: 22_hssrx_dfe_ofs_val[24][00]      787e 0000    007a
0000 7b7f 0000
0x81812694: 25_hssrx_max_gain_path_idx_res[00] 0058 084e    1105
1890 20ef 28af 3097 3800
0x81812694: 25_hssrx_max_gain_path_idx_res[08] 40df 489f    5086
5802 6044 6800 70fe 7800
0x818126c4: 31_hssrx_dfe_tap[00]              fffe 8181    0000
0000 0030 0030 3030 3030
0x818126c4: 31_hssrx_dfe_tap[08]              3030 3030    3030
0000
0x818126e8: 3A_hssrx_ac_cpl_cur_src_adj[00]    0041 0041    0041
0041
0x818126ec: 3B_hssrx_dcd_ctl[00]              7c4a 5c00    7c86
5c00 7c00
0x818126f0: 3C_hssrx_dcc_ctl[00]              0d81 0d83    0d81
0d42
0x818126f4: 3D_hssrx_qcc_ctl[00]              6948 6985

```

xfipcs, fec, aec, & aet registers

=====

```

0x81cb0400: xfipcs_reg [00] 00002040 00000080 00000000
00000000 00000001 00000008 00000000 00000000
0x81cb0420: xfipcs_reg [08] 00008401 00000000 00000000

```

```

00000000 00000000 00000000 00000000 00000000
0x81cb0440: xfipcs_reg [16] 00000000 00000000 00000000
00000000 00000040 00000000 00000000 00000000
0x81cb0460: xfipcs_reg [24] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81cb0480: xfipcs_reg [32] 00000004 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81cb0620: fec_32g_128g_reg [08] 00000000 00008003 00000000
00000000 00000000 00000000 00000000
0x81cb0648: fec_32g_128g_reg [18] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81cb0a00: aec_reg [00] 00000000 00000000 00000000
00000000 00000040 00000000 00000000 00002490
0x81cb0c00: aet_reg [00] 000000b0 00007000 000008c4
00000000 00000000

```

bbc registers

=====

```

0x81cb1800: bbc_trc 0 0 0 0 0 0 0
0
0x81cb1840: bbc_trc 0 0 0 0 0 0 0
0
0x81cb1880: bbc_trc 0 0 0 0 0 0 0
0
0x81cb18c0: bbc_trc 0 0 0 0 0 0 0
0
0x81cb1900: bbc_trc 0 0 0 0 0 0 0
0
0x81cb1804: bbc_mbc 0 0 0 0 0 0 0
0
0x81cb1844: bbc_mbc 0 0 0 0 0 0 0
0
0x81cb1884: bbc_mbc 0 0 0 0 0 0 0
0
0x81cb18c4: bbc_mbc 0 0 0 0 0 0 0
0
0x81cb1904: bbc_mbc 0 0 0 0 0 0 0
0
0x81cb1a00: bbc_rcc 0 0 0 0 0 0 0
0
0x81cb1a20: bbc_rcc 0 0 0 0 0 0 0
0
0x81cb1a40: bbc_rcc 0 0 0 0 0 0 0
0
0x81cb1a60: bbc_rcc 0 0 0 0 0 0 0
0
0x81cb1a80: bbc_rcc 0 0 0 0 0 0 0
0
0x81cb1c00: bbc_rqc 0 0 0 0 0 0 0
0
0x81cb1c20: bbc_rqc 0 0 0 0 0 0 0
0
0x81cb1c40: bbc_rqc 0 0 0 0 0 0 0
0

```

| | | | | | | | |
|-------------------------------------|----------|---|---|---|---|----------------------|---|
| 0x81cb1c60: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81cb1c80: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81cb1d00: bbc_fbpc | 00000000 | | | | | 0x81cb1d04: bbc_csc | |
| 00000000 | | | | | | | |
| 0x81cb1d08: bbc_rcc_inc | 00000000 | | | | | 0x81cb1d0c: | |
| bbc_rqc_inc | 00000000 | | | | | | |
| 0x81cb1d10: bbc_fbpc_inc | 00000000 | | | | | 0x81cb1d14: | |
| bbc_tmc_inc | 00000000 | | | | | | |
| 0x81cb1d18: bbc_threshold | 00080100 | | | | | 0x81cb1d1c: | |
| bbc_counter_clr | 00000000 | | | | | | |
| 0x81cb1d20: bbc_debug_en | 00000000 | | | | | 0x81cb1d24: bbc_ctrl | |
| 00200120 | | | | | | | |
| 0x81cb1d28: bbc_rqc_rcc_thresh | 00000055 | | | | | 0x81cb1d34: | |
| bbc_bb_sc_n | 00000000 | | | | | | |
| 0x81cb1d38: bbc_crd_reco_debug | 00000000 | | | | | 0x81cb1d3c: | |
| bbc_crd_reco_debug_data | 00000000 | | | | | | |
| 0x81cb1d40: bbc_multi_frm_loss_cnt | 00000000 | | | | | 0x81cb1d44: | |
| bbc_multi_rdy_loss_cnt | 00000000 | | | | | | |
| 0x81cb1d48: bbc_1frm_loss_recov_cnt | 00000000 | | | | | 0x81cb1d4c: | |
| bbc_1rdy_loss_recov_cnt | 00000000 | | | | | | |
| 0x81cb1d58: bbc_int_status | 00000000 | | | | | 0x81cb1d5c: | |
| bbc_int_set | 00000000 | | | | | | |
| 0x81cb1d60: bbc_int_first | 00000000 | | | | | 0x81cb1d64: | |
| bbc_frm_rdy_rx_err_addr | 00000000 | | | | | | |
| 0x81cb1d68: bbc_frm_rdy_tx_err_addr | 00000000 | | | | | 0x81cb1d6c: | |
| bbc_trc_mbc_err_addr | 00000000 | | | | | | |
| 0x81cb1d70: bbc_frm_rdy_rx_dbl_ecc | 00000000 | | | | | 0x81cb1d74: | |
| bbc_frm_rdy_tx_dbl_ecc | 00000000 | | | | | | |
| 0x81cb1d78: bbc_trc_mbc_dbl_ecc | 00000000 | | | | | | |
| 0x81cb1d7c: bbc_fsm_status | 00001011 | | | | | 0x81cb1d80: | |
| bbc_force_err | 00000000 | | | | | | |
| 0x81cb1d84: bbc_crdt_avail0 | 00000000 | | | | | 0x81cb1d88: | |
| bbc_crdt_avail1 | 00000000 | | | | | | |
| 0x81cb1d8c: bbc_scratch | 00000000 | | | | | | |

FPS registers

=====

| | | | | | | | |
|--------------------------------|----------|--|--|--|--|-------------|--|
| 0x81cb0004: fps_er_enc_in | 00000000 | | | | | 0x81cb0008: | |
| fps_er_crc | 00000000 | | | | | | |
| 0x81cb000c: fps_er_trunc | 00000000 | | | | | 0x81cb0010: | |
| fps_er_toolong | 00000000 | | | | | | |
| 0x81cb0014: fps_er_bad_eof | 00000000 | | | | | 0x81cb0018: | |
| fps_er_enc_out | 00000000 | | | | | | |
| 0x81cb001c: fps_er_bad_os | 00000000 | | | | | 0x81cb0020: | |
| fps_er_flush | 00000000 | | | | | | |
| 0x81cb0024: fps_er_ifg | 00000000 | | | | | 0x81cb0038: | |
| fps_er_crc_good_eof | 00000000 | | | | | | |
| 0x81cb003c: fps_inv_arb | 00000000 | | | | | 0x81cb0040: | |
| fps_slow_sts_status | 00000000 | | | | | | |
| 0x81cb0044: fps_tx_frm_cnt | 00000000 | | | | | 0x81cb0048: | |
| fps_rx_frm_cnt | 00000000 | | | | | | |
| 0x81cb0050: fps_tx_word_cnt_hi | 00000000 | | | | | 0x81cb004c: | |

```

fps_tx_word_cnt_lo      00000000
0x81cb0058: fps_rx_word_cnt_hi  00000000  0x81cb0054:
fps_rx_word_cnt_lo      00000000

```

BAL registers

=====

```

0x81cb7000: bal_desired_buf      00000000  0x81cb7004:
bal_alloc_buf          00000000
0x81cb7008: bal_busy_buf        00000000  0x81cb700c:
bal_usable_buf         00000000
0x81cb7010: bal_max_bor_buf      00000000
0x81cb7014: bal_busy_buf_thresh  00000002

```

TXQ registers

=====

```

0x81cb3004: txq_phys_port_ctl    00460000
0x81cb3050: txq_link_skew          00000000
0x81cb3068: txq_cr_lk_dttm_intr_sts [00] 00000000 00000000
0x81cb3070: txq_cr_lk_dttm_intr_en  [00] 00000000 00000000
0x81cb3024: txq_disc_frm_trap_cnt  00000014

```

FDS registers

=====

```

0x81cb4000: fds_rxf_ctl            00000002  0x81cb4004:
fds_rxf_wait_thresh   00000909
0x81cb4018: fds_rxf_first_error    00000000  0x81cb401c:
fds_rxf_first_error_info 00000000
0x81cb4020: fds_rxf_inout_pkt_cnt    00000000
0x81cb4008: fds_rxf_err_int_status  00000000  0x81cb4024:
fds_rxf_fifo_status    00888888
0x81cb5000: fds_txf_ctl            0000003a  0x81cb5004:
fds_txf_wait_ifg_thresh 00a00106
0x81cb5008: fds_txf_err_int_status  00000000  0x81cb5024:
fds_txf_fifo_status    00088888
0x81cb502c: fds_txf_bbc_scs      00000000

```

Logical TXQ registers

=====

```

0x81cb3000: txq_log_port_ctl    00000002  0x81cb3008:
txq_port_status       00000000
0x81cb300c: txq_todo_flags        [00] 00000000 00000000
0x81cb3014: txq_spd_match_desc    [00] 00000000 00000000 00000000
00000000
0x81cb3024: txq_spd_match_desc    [04] 00000014
0x81cb3028: txq_vc_weight        [00] 01010101 01010101 01010101
01010101
0x81cb3038: txq_vc_weight        [04] 01010101 01010101 01010101
01010101
0x81cb3048: txq_vc_weight        [08] 01010101 00010101
0x81cb3054: txq_cong_dttm_ctrl    00000106
0x81cb3058: txq_cong_dttm_intr_sts [00] 00000000 00000000
0x81cb3060: txq_cong_dttm_intr_en  [00] 00000000 00000000
0x81cb3078: txq_bw_limit_en_reg    [00] 00000000 00000000
0x81cb3080: txq_bw_gua_en_reg      [00] 00000000 00000000

```

| | | | | |
|---|------|----------|----------|----------|
| 0x81cb3088: txq_vc_group 03030303 | [00] | 03030300 | 03030303 | 03030303 |
| 0x81cb3098: txq_vc_group 03030303 | [04] | 03030303 | 03030303 | 03030303 |
| 0x81cb30a8: txq_vc_group 00000000 | [08] | 03030303 | 03030303 | 00000000 |
| 0x81cb30b0: txq_bw_thresh_group 00000000 | [00] | 00000000 | 00000000 | 00000000 |
| 0x81cb30c0: txq_bw_thresh_group 00000000 | [04] | 00000000 | 00000000 | 00000000 |
| 0x81cb30d0: txq_bw_thresh_group 00000000 | [08] | 00000000 | 00000000 | 00000000 |
| 0x81cb30e0: txq_bw_thresh_group 00000000 | [12] | 00000000 | 00000000 | 00000000 |
| 0x81cb30f0: txq_bw_thresh_group 00000000 | [16] | 00000000 | 00000000 | 00000000 |
| 0x81cb3100: txq_bw_thresh_group 00000000 | [20] | 00000000 | 00000000 | 00000000 |
| 0x81cb3110: txq_bw_thresh_group 00000000 | [24] | 00000000 | 00000000 | 00000000 |
| 0x81cb3120: txq_bw_thresh_group 00000000 | [28] | 00000000 | 00000000 | 00000000 |
| 0x81cb3130: txq_bw_thresh_group 00000000 | [32] | 00000000 | 00000000 | 00000000 |
| 0x81cb3140: txq_bw_thresh_group 00000000 | [36] | 00000000 | 00000000 | 00000000 |

txq Congestion detection Statistics RAM

=====

| | | |
|--------------------|----------|--------------------|
| 0x81090dc0: vc[0] | 00000000 | 0x81090dc4: vc[1] |
| 00000000 | | |
| 0x81090dc8: vc[2] | 00000000 | 0x81090dcc: vc[3] |
| 00000000 | | |
| 0x81090dd0: vc[4] | 00000000 | 0x81090dd4: vc[5] |
| 00000000 | | |
| 0x81090dd8: vc[6] | 00000000 | 0x81090ddc: vc[7] |
| 00000000 | | |
| 0x81090de0: vc[8] | 00000000 | 0x81090de4: vc[9] |
| 00000000 | | |
| 0x81090de8: vc[10] | 00000000 | 0x81090dec: vc[11] |
| 00000000 | | |
| 0x81090df0: vc[12] | 00000000 | 0x81090df4: vc[13] |
| 00000000 | | |
| 0x81090df8: vc[14] | 00000000 | 0x81090dfc: vc[15] |
| 00000000 | | |
| 0x81090e00: vc[16] | 00000000 | 0x81090e04: vc[17] |
| 00000000 | | |
| 0x81090e08: vc[18] | 00000000 | 0x81090e0c: vc[19] |
| 00000000 | | |
| 0x81090e10: vc[20] | 00000000 | 0x81090e14: vc[21] |
| 00000000 | | |
| 0x81090e18: vc[22] | 00000000 | 0x81090e1c: vc[23] |
| 00000000 | | |
| 0x81090e20: vc[24] | 00000000 | 0x81090e24: vc[25] |

```

00000000
0x81090e28: vc[26]      00000000      0x81090e2c: vc[27]
00000000
0x81090e30: vc[28]      00000000      0x81090e34: vc[29]
00000000
0x81090e38: vc[30]      00000000      0x81090e3c: vc[31]
00000000
0x81090e40: vc[32]      00000000      0x81090e44: vc[33]
00000000
0x81090e48: vc[34]      00000000      0x81090e4c: vc[35]
00000000
0x81090e50: vc[36]      00000000      0x81090e54: vc[37]
00000000
0x81090e58: vc[38]      00000000      0x81090e5c: vc[39]
00000000

```

Logical STS registers

```

=====
0x81585104: sts_ftb_type1_miss      00000000
0x81585108: sts_ftb_type2_miss      00000000
0x8158510c: sts_ftb_type6_miss      00000000
0x81585110: sts_hard_zoning_miss    00000000
0x81585114: sts_lun_zoning_miss     00000000
0x8158511c: sts_unroutable          00000000
0x81582134: sts_rte_cl2            00000000      0x81582138:
sts_rte_cl3      00000000      0x8158213c: sts_rte_link_ctl
00000000      0x81585128: sts_tx_timeout      00000000

```

Logical STS filter registers

```

=====
0x81585080: stsflt_trig      [00] 00000000 00000000 00000000
00000000
0x81585090: stsflt_trig      [04] 00000000 00000000 00000000
00000000
0x815850a0: stsflt_trig      [08] 00000000 00000000 00000000
00000000
0x815850b0: stsflt_trig      [12] 00000000 00000000 00000000
00000000
0x815850c0: stsflt_trig      [16] 00000000 00000000 00000000
00000000
0x815850d0: stsflt_trig      [20] 00000000 00000000 00000000
00000000
0x815850e0: stsflt_trig      [24] 00000000 00000000 00000000
00000000
0x815850f0: stsflt_trig      [28] 00000000 00000000 00000000
00000000
0x81585100: stsflt_trig      [32]

```

Logical STS discard registers

```

=====
0x81582ff8: disc_mcast_wka      00000000      0x81582ffc:
disc_inv_did      00000000
0x81583000: disc_cl1_cl4          00000000      0x81583004:

```

```

disc_sid_chk_fail      00000000
0x81583008: disc_inv_dom_egid_txpt 00000000 0x8158300c:
disc_vft_hop_cnt_1    00000000
0x81583010: disc_classf      00000000 0x81583014:
disc_fcp_cdb_inv      00000000
0x81583018: disc_vfid_trap_enabled 00000000 0x8158301c:
disc_vfid_hdr_chk_fail 00000000
0x81583020: disc_shim_cksum_fail 00000000 0x81583024:
disc_fed_edit_cmd_err 00000000
0x81583028: disc_ftb_vm_mode    00000000 0x8158302c:
disc_ftb_agnt2_miss   00000000
0x81583030: disc_ecb_reserved   00000000 0x81583034:
disc_ecb_de_pad_err   00000000
0x81583038: disc_ecb_de_tag_err  00000000 0x8158303c:
disc_ecb_de_seq_err   00000000
0x81583040: disc_ecb_err        00000000 0x81583044:
disc_ftb_type4_match  00000000
0x81583048: disc_fcp_rsp_ftb_type4 00000000 0x8158304c:
disc_ftb_type5_match  00000000
0x81583050: disc_ftb_type3_match 00000000 0x81583054:
disc_els_ftb_type3    00000000
0x81583058: disc_ftb_type1_match 00000000 0x8158305c:
disc_els_rsp_ex_port  00000000
0x81583060: disc_inv_drp_dps    00000000 0x81583064:
disc_did_lookup_miss  00000000
0x81583068: disc_ftb_type2_match 00000000 0x8158306c:
disc_trpd_plogi_pdisc 00000000
0x81583070: disc_type2_lookup_miss 00000000 0x81583074:
disc_ftb_type6_match  00000000
0x81583078: disc_els_rep_ex_port 00000000 0x8158307c:
disc_els_sid_lkup_bit1 00000000
0x81583080: disc_els_sid_lkup_bit0 00000000 0x81583084:
disc_bls_frm_trap_bit1 00000000
0x81583088: disc_ftb_token_err   00000000 0x8158308c:
disc_asic_internal_err 00000000
0x81583090: disc_hard_zone_miss  00000000 0x81583094:
disc_lun_zone_miss    00000000
0x81583098: discflt_frame_disc   00000000 0x8158309c:
discflt_parity_err    00000000
0x815830a0: disc_frame_marked_du 00000000 0x815830a4:
disc_frame_marked_to  00000000
0x815830a8: disc_lkup_rte_prty_err 00000000

```

portstatsshow 40

```

stat_wtx      0      4-byte words transmitted
stat_wrx      0      4-byte words received
stat_ftx      0      Frames transmitted
stat_frx      0      Frames received
stat_c2_frx   0      Class 2 frames received
stat_c3_frx   0      Class 3 frames received
stat_lc_rx    0      Link control frames
received
stat_mc_rx    0      Multicast frames

```


| | | | | | |
|------------------------------|------------|-----|-----|-------------------------|-----|
| received | | | | | |
| stat_mc_to | 0 | | | Multicast timeouts | |
| stat_mc_tx | 0 | | | Multicast frames | |
| transmitted | | | | | |
| tim_txcrd_z | 0 | | | Time TX Credit Zero | |
| (2.5Us ticks) | | | | | |
| tim_txcrd_z_vc 0- 3: | 0 | 0 | 0 | 0 | 0 |
| tim_txcrd_z_vc 4- 7: | 0 | 0 | 0 | 0 | 0 |
| tim_txcrd_z_vc 8-11: | 0 | 0 | 0 | 0 | 0 |
| tim_txcrd_z_vc 12-15: | 0 | 0 | 0 | 0 | 0 |
| lat_tot_pkt_vc 0- 3: | 1 | 1 | 1 | 1 | 1 |
| lat_tot_pkt_vc 4- 7: | 1 | 1 | 1 | 1 | 1 |
| lat_tot_pkt_vc 8-11: | 1 | 1 | 1 | 1 | 1 |
| lat_tot_pkt_vc 12-15: | 1 | 1 | 1 | 1 | 1 |
| lat_hi_time_vc 0- 3: | 0 | 0 | 0 | 0 | 0 |
| lat_hi_time_vc 4- 7: | 0 | 0 | 0 | 0 | 0 |
| lat_hi_time_vc 8-11: | 0 | 0 | 0 | 0 | 0 |
| lat_hi_time_vc 12-15: | 0 | 0 | 0 | 0 | 0 |
| lat_lo_time_vc 0- 3: | 1 | 1 | 1 | 1 | 1 |
| lat_lo_time_vc 4- 7: | 1 | 1 | 1 | 1 | 1 |
| lat_lo_time_vc 8-11: | 1 | 1 | 1 | 1 | 1 |
| lat_lo_time_vc 12-15: | 1 | 1 | 1 | 1 | 1 |
| max_latency_vc 0- 3: | 1 | 1 | 1 | 1 | 1 |
| max_latency_vc 4- 7: | 1 | 1 | 1 | 1 | 1 |
| max_latency_vc 8-11: | 1 | 1 | 1 | 1 | 1 |
| max_latency_vc 12-15: | 1 | 1 | 1 | 1 | 1 |
| latency_dma_ts | 09-09-2024 | UTC | Mon | 08:47:24 | TXQ |
| Latency DMA TimeStamp | | | | | |
| fec_cor_detected | 0 | | | Count of blocks that | |
| were corrected by FEC | | | | | |
| fec_uncor_detected | 0 | | | Count of blocks that | |
| were left uncorrected by FEC | | | | | |
| er_enc_in | 0 | | | Encoding errors inside | |
| of frames | | | | | |
| er_crc | 0 | | | Frames with CRC errors | |
| er_trunc | 0 | | | Frames shorter than | |
| minimum | | | | | |
| er_toolong | 0 | | | Frames longer than | |
| maximum | | | | | |
| er_bad_eof | 0 | | | Frames with bad end-of- | |
| frame | | | | | |
| er_enc_out | 0 | | | Encoding error outside | |
| of frames | | | | | |
| er_bad_os | 0 | | | Invalid ordered set | |
| er_pcs_blk | 0 | | | PCS block errors | |
| er_rx_c3_timeout | 0 | | | Class 3 receive frames | |
| discarded due to timeout | | | | | |
| er_tx_c3_timeout | 0 | | | Class 3 transmit frames | |
| discarded due to timeout | | | | | |
| er_unroutable | 0 | | | Frames that are | |
| unroutable | | | | | |
| er_unreachable | 0 | | | Frame with unreachable | |
| destination | | | | | |
| er_other_discard | 0 | | | Other discards | |

| | | |
|-----------------------|-----------------------------|--------------------------|
| er_type1_miss | 0 | frames with FTB type 1 |
| miss | | |
| er_type2_miss | 0 | frames with FTB type 2 |
| miss | | |
| er_type6_miss | 0 | frames with FTB type 6 |
| miss | | |
| er_zone_miss | 0 | frames with hard zoning |
| miss | | |
| er_lun_zone_miss | 0 | frames with LUN zoning |
| miss | | |
| er_crc_good_eof | 0 | Crc error with good eof |
| er_inv_arb | 0 | Invalid ARB |
| er_single_credit_loss | 0 | Single vcrdy/frame loss |
| on link | | |
| er_multi_credit_loss | 0 | Multiple vcrdy/frame |
| loss on link | | |
| other_credit_loss | 0 | Link timeout/complete |
| credit loss | | |
| phy_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | Timestamp of |
| phy_port stats clear | | |
| lgc_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | Timestamp of |
| lgc_port stats clear | | |
| fec_corrected_rate | 0 | FEC Corrected blocks per |
| second | | |

portstats64show 40

| | | |
|---------------|---|--|
| stat64_wtx | 0 | top_int : 4-byte words transmitted |
| | 0 | bottom_int : 4-byte words transmitted |
| stat64_wrx | 0 | top_int : 4-byte words received |
| | 0 | bottom_int : 4-byte words received |
| stat64_ftx | 0 | top_int : Frames transmitted |
| | 0 | bottom_int : Frames transmitted |
| stat64_frx | 0 | top_int : Frames received |
| | 0 | bottom_int : Frames received |
| stat64_c2_frx | 0 | top_int : Class 2 frames received |
| | 0 | bottom_int : Class 2 frames received |
| stat64_c3_frx | 0 | top_int : Class 3 frames received |
| | 0 | bottom_int : Class 3 frames received |
| stat64_lc_rx | 0 | top_int : Link control frames received |
| | 0 | bottom_int : Link control frames |
| received | | |
| stat64_mc_rx | 0 | top_int : Multicast frames received |
| | 0 | bottom_int : Multicast frames received |
| stat64_mc_to | 0 | top_int : Multicast timeouts |
| | 0 | bottom_int : Multicast timeouts |
| stat64_mc_tx | 0 | top_int : Multicast frames transmitted |
| | 0 | bottom_int : Multicast frames |
| transmitted | | |
| tim64_rdy_pri | 0 | top_int : Time R_RDY high priority |
| | 0 | bottom_int : Time R_RDY high priority |
| tim64_txcrd_z | 0 | top_int : Time BB_credit zero |
| | 0 | bottom_int : Time BB_credit zero |
| er64_enc_in | 0 | top_int : Encoding errors inside of |
| frames | | |

| | | |
|---|---|--|
| frames | 0 | bottom_int : Encoding errors inside of |
| er64_crc | 0 | top_int : Frames with CRC errors |
| | 0 | bottom_int : Frames with CRC errors |
| er64_trunc | 0 | top_int : Frames shorter than minimum |
| | 0 | bottom_int : Frames shorter than minimum |
| er64_toolong | 0 | top_int : Frames longer than maximum |
| | 0 | bottom_int : Frames longer than maximum |
| er64_bad_eof | 0 | top_int : Frames with bad end-of-frame |
| | 0 | bottom_int : Frames with bad end-of- |
| frame | | |
| er64_enc_out | 0 | top_int : Encoding error outside of |
| frames | 0 | bottom_int : Encoding error outside of |
| frames | | |
| er64_disc_c3 | 0 | top_int : Class 3 frames discarded |
| | 0 | bottom_int : Class 3 frames discarded |
| er64_pcs_blk | 0 | top_int : PCS block errors |
| | 0 | bottom_int : PCS block errors |
| stat64_rateTxFrame | 0 | Tx frame rate (fr/sec) |
| stat64_rateRxFrame | 0 | Rx frame rate (fr/sec) |
| stat64_rateTxPeakFrame | 0 | Tx peak frame rate (fr/sec) |
| stat64_rateRxPeakFrame | 0 | Rx peak frame rate (fr/sec) |
| stat64_rateTxWord | 0 | Tx Word rate (words/sec) |
| stat64_rateRxWord | 0 | Rx Word rate (words/sec) |
| stat64_rateTxPeakWord | 0 | Tx peak Word rate (words/sec) |
| stat64_rateRxPeakWord | 0 | Rx peak Word rate (words/sec) |
| stat64_PRJTFrames | 0 | top_int : Number of PRJT frames |
| returned to this port | 0 | bottom_int : Number of PRJT |
| frames returned to this port | | |
| stat64_PBSYFrames | 0 | top_int : Number of PBSY frames |
| returned to this port | 0 | bottom_int : Number of PBSY |
| frames returned to this port | | |
| stat64_inputBuffersFull | 0 | top_int : Number of occurrences |
| when all input buffers full | 0 | bottom_int : Number of |
| occurrences when all input buffers full | | |
| stat64_rxClass1Frames | 0 | top_int : Number of class 1 |
| frames received | 0 | bottom_int : Number of class 1 |
| frames received | | |
| stat64_aveTxFrameSize | 0 | Average Tx Frame size |
| stat64_aveRxFrameSize | 0 | Average Rx Frame size |
| Lr_in | 0 | top_int |
| | 0 | bottom_int |
| Ols_in | 0 | top_int |
| | 0 | bottom_int |
| Lr_out | 0 | top_int |
| | 0 | bottom_int |
| Ols_out | 0 | top_int |
| | 0 | bottom_int |
| Link_failure | 0 | top_int |

```

Invalid_CRC      0          bottom_int
                 0          top_int
Invalid_word     0          bottom_int
                 0          top_int
Protocol_err     0          bottom_int
                 0          top_int
Loss_of_sig      0          bottom_int
                 0          top_int
Loss_of_sync    0          top_int
                 0          bottom_int
er_bad_os        0          top_int : Invalid ordered set
                 0          bottom_int: Invalid ordered set

```

```

portrouteshow 40
port address ID: 0x012800
external unicast routing table:
  0: Embedded
 255: Embedded
internal unicast routing table:
  0: Embedded

```

```
portcamshow 40
```

```

-----
Port  SID used  DID used  SID entries  DID entries
40    0         0         000000      000000
-----

```

```
ptbufshow, ptcreditshow, ptdatashow, ptstatsshow 40
```

```

S:
S:VF Enable:          1
S:
S:C4 Global Variable:
S:-----

```

```

S:trace_stop:        0
S:
S:C4 Phy Data Pointers: c4_phyp = 0xb6ae2080
S:-----

```

```

S:tnodep              0xbb8447e0      pt
   0x43028016
S:proto_phyp          0xb880a480      phy_cfg
0xb6ae30c0
S:c4_chp              0x97e28000      c4_lgcp
0x97fa0000
S:c4_phy_regp         0x81cb0000      proc_dir
0xb851b820
S:-----

```

```

S:magic_id            0xc4345678      num_port_timer      12
S:prev_if_id          0x43020016      S:ftx                0
   tov                0

```

| | | | |
|----------------------------|------------|-----------------------|-----|
| S:initialized | 1 | port_idx | 22 |
| S:ui_idx | 40 | slot_no | |
| 0 | | | |
| S:blade_idx | 22 | sw_usr_ports | 400 |
| S:unused | 0 | intr_debounced | |
| 0 | | | |
| S:aec_status | 0x0 | reason_code | |
| 0 | | | |
| S:debug | 0x00000004 | debug_trc_line | 0 |
| S:rxbuf_list_head | 0xffffffff | rxbuf_list_tail | |
| 0xffffffff | | | |
| S:isAePort | 0 | port_misc_data | |
| 0 | | | |
| S:num_fault1_rx_disc | 0 | num_fault2_rx_disc | 0 |
| S:p_lli_cause0 | 0 | p_sig_regained | 0 |
| S:p_sync_regained | 0 | enc_out | |
| 0x0 | | | |
| S:cached_fps_status | 0 | cached_sts_status | 0 |
| S:cached_er_crc_good_eof | 0 | | |
| S:cached_er_bad_os | 0 | cached_er_too_long | 0 |
| S:cached_er_trunc | 0 | | |
| cached_tot_er_crc_good_eof | 0 | | |
| S:num_pt_excess_intr | 0 | num_no_fid | 0 |
| S:num_fault1_cnt | 0 | num_fault2_cnt | |
| 0 | | | |
| S:num_fault_lip | 0 | num_fault_lli | 0 |
| S:num_fault_rx_fifo | 0 | num_fault_hss | 0 |
| S:num_fault_bwait | 0 | lli_intr_prim | |
| 0 | | | |
| S:num_sw_link_to | 0 | | |
| be_link_err_mon_count | 0 | | |
| S:ecb_enc_enabled | 0 | ecb_comp_enabled | |
| 0 | | | |
| S:ecb_rsv_enc | 0 | ecb_rsv_comp | 0 |
| S:ecb_enc_bm | 0x0 | ecb_key_index | |
| 0xffffffff | | | |
| S:fab_idx | 0 | | |
| S:num_be_lto | 0 | lto_count_reset_intvl | |
| 0 | | | |
| S:lr_count_reset_intvl | 0 | num_be_lr | |
| 0 | | | |
| S:num_fault_qsfp | 0 | check_lto | |
| 0 | | | |
| S:credit_loaded | 0 | num_credit_overrun | |
| 0 | | | |
| S:fec_enabled | 0x0 | fec_los_to_flag | 0x0 |
| S:phy_stats_clear_ts | 1725611419 | pcs_err_online | |
| 0 | | | |
| S:pcs_err_light_det | 0 | pcs_err_ignore | |
| 0 | | | |
| S:pcs_blk_err | 0 | pcs_hiber | 0 |
| S:phy_port_status | 0 | ecb_enc_lr_count | |
| 0 | | | |
| S:dport_mode | 0 | avoid_lto_det | 0 |

```

S:sn_debounced          0x0          sn_started_kr_reqd      0
S:major_timer_started   0x0          ready_bm                0x0
S:parln_1_bm            0x0          parln_0_bm              0x0
S:be_los_of_sync_event_intvl 0
be_los_of_sync_event    0
S:errataPtenable_cntr  0          errataPoll_cntr
0
S:jda_rx_sig_loss_det   0          jda_rx_sig_loss_cnt
0
S:encrypt_blk_error     0
S:
S:      c4_trunk
S:=====
S:mark_ts                0x0          deskew                  0x0
S:master_phyp            0x0
S:
S:adelay[00]: 0x00000000 0x00000000 0x00000000 0x00000000
S:adelay[04]: 0x00000000 0x00000000 0x00000000 0x00000000
S:
S:      c4_buf
S:=====
S:tx_csc                  0          rx_csc
0
S:ld_vc_credits           0          tx_flag                 0x0
S:alloc_buffers           0          req_buffers             0
S:est_buffers             20         ld_use_est              0
S:bb_sc_n                 0          rx_bb_sc_n
0
S:data_cr                 5          nondata_cr
6
S:cr_enable               0
S:ld_nondata_cr          6          tnodep
0xbb8448c0
S:tx_credits[0] 0 0 0 0 0 0 0 0
S:tx_credits[8] 0 0 0 0 0 0 0 0
S:tx_credits[16] 0 0 0 0 0 0 0 0 0 0
S:tx_credits[24] 0 0 0 0 0 0 0 0 0 0
S:tx_credits[32] 0 0 0 0 0 0 0 0 0 0
S:rx_credits[0] 0 0 0 0 0 0 0 0
S:rx_credits[8] 0 0 0 0 0 0 0 0
S:rx_credits[16] 0 0 0 0 0 0 0 0 0 0
S:rx_credits[24] 0 0 0 0 0 0 0 0 0 0
S:rx_credits[32] 0 0 0 0 0 0 0 0 0 0
S:tx_mbc[0] 0 0 0 0 0 0 0 0
S:tx_mbc[8] 0 0 0 0 0 0 0 0
S:tx_mbc[16] 0 0 0 0 0 0 0 0
S:tx_mbc[24] 0 0 0 0 0 0 0 0
S:tx_mbc[32] 0 0 0 0 0 0 0 0
S:rx_mbc[0] 0 0 0 0 0 0 0 0
S:rx_mbc[8] 0 0 0 0 0 0 0 0
S:rx_mbc[16] 0 0 0 0 0 0 0 0
S:rx_mbc[24] 0 0 0 0 0 0 0 0
S:rx_mbc[32] 0 0 0 0 0 0 0 0
S:

```

S:C4 Chip Variables: c4_phyp->c4_chp = 0x97e28000

S:-----

S:version = 2.1
S:magic_id 0xc4234567 init_state 0x8
S:reset_reg_mem 0x1
S:ch_int0_en_bm 0x0 intr0_cause 0x0
S:ch_int1_en_bm 0x0 intr1_cause 0x0
S:ch_int2_en_bm 0x0 intr2_cause 0x0
S:ch 0x43010080 ch_cfg
0xb7013ba0
S:raslog_hndl.hndl 0x0 obj_halted 0x0
S:c4_chip_regp 0x80000000 c4_fpg_regp
0x81800000
S:num_chip_timer 0x5
S:hi_task_bm 0x0 lo_task_bm 0x0
S:c4_deferq.q_head 0x0 c4_deferq.q_tail 0x0
S:c4_tmrq.q_head 0x0 c4_tmrq.q_tail 0x0
slot_no 0
S:chip_inst 0 chip_idx 0
S:pll_initialized 1
pll_serdes_initialized 1
S:init_tries 0 init_ptEnableBM
0xba01b488
S:tick_polling 0xb980c9c0 sec_polling
0xb980c960
S:bb_fid 129
S:ecb_key_bm[0] 0x0 ecb_key_bm[1] 0x0
S:ecb_key_bm[2] 0x0 ecb_key_bm[3] 0x0
S:is_chip_enc_enabled 0
is_chip_comp_enabled 0x0
S:ftb_rsrcp->ftb_flags 0x0 act_rsrcp->act_flag 0x1
S:lue_rsrcp->lue_flags[0] 0x0 lue_rsrcp->
>lue_flags[1] 0x0
S:c4_phyp[00]: 0xb6ab0000 0xb6ab2080 0xb6ab4100 0xb6ab6180
S:c4_phyp[04]: 0xb6ab9040 0xb6abb0c0 0xb6abd140 0xb6ac0000
S:c4_phyp[08]: 0xb6ac2080 0xb6ac4100 0xb6ac6180 0xb6ac9040
S:c4_phyp[12]: 0xb6acb0c0 0xb6acd140 0xb6ad0000 0xb6ad2080
S:c4_phyp[16]: 0xb6ad4100 0xb6ad6180 0xb6ad9040 0xb6adb0c0
S:c4_phyp[20]: 0xb6add140 0xb6ae0000 0xb6ae2080 0xb6ae4100
S:c4_phyp[24]: 0xb6ae6180 0xb6ae9040 0xb6aeb0c0 0xb6aed140
S:c4_phyp[28]: 0xb6af0000 0xb6af2080 0xb6af4100 0xb6af6180
S:c4_phyp[32]: 0xb6af9040 0xb6afb0c0 0xb6afd140 0xb6b00000
S:c4_phyp[36]: 0xb6b02080 0xb6b04100 0xb6b06180 0xb6b09040
S:c4_phyp[40]: 0xb6b0b0c0 0xb6b0d140 0xb6b10000 0xb6b12080
S:c4_phyp[44]: 0xb6b14100 0xb6b16180 0xb6b19040 0xb6b1b0c0
S:c4_phyp[48]: 0xb6b1d140 0xb6b20000 0xb6b22080 0xb6b24100
S:c4_phyp[52]: 0xb6b26180 0xb6b29040 0xb6b2b0c0 0xb6b2d140
S:c4_phyp[56]: 0xb6b30000 0xb6b32080 0xb6b34100 0xb6b36180
S:c4_phyp[60]: 0xb6b39040 0xb6b3b0c0 0xb6b3d140 0xb6b40000
S:c4_lgcp[00]: 0x97f48000 0x97f4c000 0x97f50000 0x97f54000
S:c4_lgcp[04]: 0x97f58000 0x97f5c000 0x97f60000 0x97f64000
S:c4_lgcp[08]: 0x97f68000 0x97f6c000 0x97f70000 0x97f74000
S:c4_lgcp[12]: 0x97f78000 0x97f7c000 0x97f80000 0x97f84000

```

S:c4_lgcp[16]: 0x97f88000 0x97f8c000 0x97f90000 0x97f94000
S:c4_lgcp[20]: 0x97f98000 0x97f9c000 0x97fa0000 0x97fa4000
S:c4_lgcp[24]: 0x97fa8000 0x97fac000 0x97fb0000 0x97fb4000
S:c4_lgcp[28]: 0x97fb8000 0x97fbc000 0x97fc0000 0x97fc4000
S:c4_lgcp[32]: 0x97fc8000 0x97fcc000 0x97fd0000 0x97fd4000
S:c4_lgcp[36]: 0x97fd8000 0x97fdc000 0x97fe0000 0x97fe4000
S:c4_lgcp[40]: 0x97fe8000 0x97fec000 0x97ff0000 0x97ff4000
S:c4_lgcp[44]: 0x97ff8000 0x97ffc000 0x8e000000 0x8e004000
S:c4_lgcp[48]: 0x8e008000 0x8e00c000 0x8e010000 0x8e014000
S:c4_lgcp[52]: 0x8e018000 0x8e01c000 0x8e020000 0x8e024000
S:c4_lgcp[56]: 0x8e028000 0x8e02c000 0x8e030000 0x8e034000
S:c4_lgcp[60]: 0x8e038000 0x8e03c000 0x8e040000 0x8e044000
S:chip_timers[00]: 0xb980c720 0xb980c780 0xb980c7e0 0xb980c840
S:chip_timers[04]: 0xb980c8a0 0xb980c900
S:disc_trap_enable_required      0x0          rxlp_disc_log_stop
          0x0
S:curr_rxlp_frm_cnt      0x0          curr_rxlp_disc_frm_cnt  0x0
S:sw_disc_frm_cnt      0x0          last_disc_frm_cnt      0x0
S:txq_nopop_pr_cnt      0x0          pollErrataDfe_ptBM
0xba01b4b0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][0]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][1] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][2]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][0] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][1]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][2] 0x0
S:
S:C4 Logical Port Variables
S:-----
-----
S:c4_lgc_regp      0x81cb0000
S:c4_phyp:
S:      0xb6ae2080      0x0          0x0          0x0

S:      0x0          0x0          0x0          0x0

S:master_phyp      0xb6ae2080      if_id
0x43020016
S:min_phyp      0x0          max_phyp      0x0
S:num_phy_ports      1          lgc_num      22
S:num_iu_to      0          sw_txq_bm
0
S:port_fid      128          unused      0
S:port_group      2          lgc_stats_clear_ts
1725611419
S:domain_tbl_sel      0          area_tbl_sel
0
S:egid_tbl_sel      0
S:serv_lo_bm      0x0
S:
S:Proto Phy Variables:
S:-----
-----
S:magic_id      0xc4123456      asic_phyp

```



```

0xb6ae2080
S:port_id                0x43028016        phy_cfg
    0xb6ae30c0
S:upsm_hdl               0xb8016c80        physm_hdl
0xb8016a00
S:ov_snsn_hdl           0xb80168c0        sw_snsn_hdl
0xb8016960
S:ov_lksm_hdl           0xb8016aa0        sw_lksm_hdl
0xb8016b40
S:trksm_hdl             0xb8016be0        lr_flag            0x0
S:lr_active             0x0                qsfm_txxrx_rate_sel
    0x0

S:
S:UPSM      UP00: UPST_PORT_DISABLED    --> UP01:
UPST_START_PORT_INIT
S:SNSM(OV)  SN00: OV_SNST_STOPPED        --> SN00: OV_SNST_STOPPED
S:SNSM(SW)  SW00: SW_SNST_STAGE_WS      --> SW00: SW_SNST_STAGE_WS
S:PHYSM     UNKNOWN                     --> PP03: PHYST_NO_SIGNAL
S:LKSM(OV)  LK00: OV_LKST_INACTIVE      --> LK00: OV_LKST_INACTIVE
S:LKSM(SW)  SW13: INACTIVE              --> SW13: INACTIVE
S:TRKSM     TRK0: TRKST_INIT            --> TRK0: TRKST_INIT
S:
S:physm variables:
S:-----
-----
S:proto_phyp           0xb880a480        physm_hdl
0xb8016a00
S:force_offline        0                copper                0
S:fault_reason         0: UNKNOWN
S:phy_media_present    1
S:
S:snsn variables:
S:-----
-----
S:speed                0xff             proto_phyp
0xb880a480
S:hw_sn_tries_left     0x0              sw_sn_tries_left      0x0
S:curr_txsp_count      0x0              curr_tx_indx
S:tx_max               0x0              curr_rxsp_count
    0x0
S:curr_tx              0x0              curr_rx_indx
    0x0
S:rx_max               0x0              rx_mem
    0x0
S:curr_rx              0x0
    0x0
S:rxsp_rec_count      0x0
S:nc_start             0x0              tx_start                0x0
S:sync_start          0x0              sync_present            0x0
S:diag_auto           0x0              diag_speed              0xff
S:striped_wd_tov      3000             hw_wd_tov
    3000
S:step                 0x0              qsfm28_speed_mode
    0x0

```

```

S:qsfm_mode0_hw_sn_tries_left      0x0
S:qsfm_mode1_hw_sn_tries_left      0x0
S:
S:lksm variables:
S:-----
-----
S:proto_phyph      0xb880a480      ov_lksm_hdl
0xb8016aa0
sw_lksm_hdl      0xb8016b40
num_lf1          0
S:hw_link_tries_left      0      sw_link_tries_left      0
S:buf_ptype      0x0      stored_entry_state      0x6
S:handshake_owner      0x0      mark_unsent
      0x0
S:busybuf_stuck      0x0      lr_wait      0x0
S:
S:trksm variables:
S:-----
-----
S:Not a trunk port
S:
S:upsm variables:
S:-----
-----
S:proto_phyph      0xb880a480      upsm_hdl
0xb8016c80
S:bb_credits      0      port_beacon      0
S:port_diag_flag      0      force_offline
      0
S:port_fault_rsn      0: PORT_NO_FAULT
S:retry_init_rsn      0: UNKNOWN
S:linit_reason      0      linit_result      0
S:ie_fctl_mode      0      fec_in_sync_tries_left      0
S:retry_sn_fail_init      0
retry_link_fail_init      0
S:excess_lr_count      0
S:
S:c4_ch_cfg
S:-----
-----
S:c4_desc_ring_size      256      292      256      256      292
292      2      292      292
S:thresh_def      0      16      1      0
S:intr_tries      500      cmem_pattern
0xdeadbeef
S:cmem_pattern_upwd      2      cmem_init_time      16
S:cmem_init_tries      5
S:ctrl_par_thresh      2      data_par_thresh
4
S:cam_par_thresh      4      buf_loss_thresh
12
S:crit_par_thresh      2      non_crit_par_thresh
6
S:pci_abort_thresh      10      pci_err_thresh      5

```

```

S:excess_chintr_thresh 8 sw_err_thresh 20
S:err_sample_period 300 intr_sleep
20000
S:frame_timeout 2500 proxy_dev 16384
S:vf_route 81920 qos 2048
S:stats 2048 f_redirect 2048
S:rsp_trap 2048 lun_zoning 20480
S:area_mode 0 ftb_max_loop[0] 0
S:ftb_max_loop[1] 6 ftb_max_loop[2] 9
S:ftb_max_loop[3] 10 ftb_max_loop[4] 10
S:ftb_max_loop[5] 5 ftb_max_loop[6] 6
S:ftb_seg_size[0] 0 ftb_seg_size[1]
16384
S:ftb_seg_size[2] 65536 ftb_seg_size[3]
16384
S:ftb_seg_size[4] 16384 ftb_seg_size[5]
65536
S:ftb_seg_size[6] 16384 ftb_seg_base[0] 0
S:ftb_seg_base[1] 0 ftb_seg_base[2]
65536
S:ftb_seg_base[3] 16384 ftb_seg_base[4]
32768
S:ftb_seg_base[5] 131072 ftb_seg_base[6]
49152
asic_err_monitor_period1 300
asic_err_monitor_period2 86400
zone_chk_to_poll_period 25
zone_chk_class2_reject_tov 220
S:
S:c4_phy_cfg
S:-----
-----
S:version = 2.1
S:pt 0x43028016 fab_ptr
0x9a800000
S:fabattr 0x9a8000d4 fab_iop
0x9a800050
S:cfgbm 0xbb844624 port_ctrl
0xb6ae30d8
S:pcap.pcap_bm 0x8d215547 pcap.pcap2_bm
0x588289
S:pcap.pcap3_bm 0x1bebe0c
ui_idx 40 S:slot_no
0
is_icl 0 S:sw_usr_ports 400
S:neg_speed 0 0 0 0 0 0
S:my_domain 0x1 port_mode 0x0
S:hw_sn_maxtries 100 sw_sn_maxtries
0
S:hw_link_maxtries 10 sw_link_maxtries 5
S:rx_cyc_tov 28 rttov 300
S:bufrdy_tov 300 busybuf_tov 286
S:mark_tov 300 lksm_tov 3000
S:buf_dealloc_wait 4 hw_wd_tov 3000

```

```

S:hw_lk_train_tov          540          hw_lk_test_tov
   150
S:syswait_tx_12_lips      1          lip_rx_tov          55
S:al_time_tov            15          lp_tov              2000
S:intr_tries_port        500          intr_mod_debounce
   250
S:intr_lsrflt_debounce    500          intr_efifo_debounce  100
S:port_no_fid            3          excess_ptintr_thresh  8
S:port_fault1_thresh     100          port_fault1_spur_thresh 250
S:port_fault1_disc_thresh 500
port_fault1_disc_spur_thresh 1000
S:port_fault2_thresh     5          losync_tov          100
S:port_sw_link_to        15          en_8g_scramble
   1
frc_hw_sn_mode           0x1
S:enc_poll_thresh        0          fec_enable
   0
S:fec_in_sync_to         50          fec_in_sync_try_max
   4
S:port_be_lto_threshold  100          port_be_lr_threshold
   2
S:be_cr_in_sync_to       5
port_credit_overrun_thresh 10
S:jda_sfp_losig_tov      400
jda_sfp_losig_try_max    30
S:striped_wd_tov         3000
no_sync_debounce         1200
S:
S:      fab_iop
S:=====
S:fab_iop->interop_mode  0x0          fab_iop->lab_mode      0x0
S:fab_iop->fl_bbc        0x0          fab_iop->fl_fan
   0x0
S:fab_iop->fl_cls        0x4          fab_iop->fl_rscn
   0x0
S:fab_iop->domain_id_offset 0x60          fab_iop-
>mcdt_fabric_mode        0x0
S:fab_iop->mcdt_default_zone 0x0          fab_iop-
>mcdt_safe_zone          0x0
S:
S:      port_ctrl
S:=====
S:port_ctrl.port_type    1          port_ctrl.port_grp    2
S:port_ctrl.port_number  40          port_ctrl.vc_mode      1
S:
S:      port_ctrl.lcap
S:=====
S:has_serdes             0          has_media              1
S:topology               1          skip_nego              0
S:skip_pnego             0          skip_init_event        0
S:en_shim                0          speed_neg
   1
S:loop_back              0          num_speeds             5
S:fec_enable             0

```

```

S:
S:      port_ctrl.speed_list array
S:=====
S:speed_list[0].auto_neg  1      speed_list[0].lnk_speed  0x0000000a
S:speed_list[1].auto_neg  1      speed_list[1].lnk_speed  0x00000008
S:speed_list[2].auto_neg  0      speed_list[2].lnk_speed  0x00000006
S:speed_list[3].auto_neg  1      speed_list[3].lnk_speed  0x00000005
S:speed_list[4].auto_neg  0      speed_list[4].lnk_speed  0x00000003
S:speed_list[5].auto_neg  0      speed_list[5].lnk_speed  0x00000000
S:
S:      port_ctrl.cm
S:=====
S:port_ctrl.cm.num_vcs      8
S:port_ctrl.cm.min_bufs    8
S:port_ctrl.cm.cr_shar_bufs 0
S:port_ctrl.vc_alloc
S:port_ctrl.vc_alloc      2 0 1 1 1 1 1 1
S:port_ctrl.vc_alloc      0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.norm_vc_alloc
S:port_ctrl.norm_vc_alloc  4 0 5 5 5 5 1 1
S:port_ctrl.norm_vc_alloc  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.cm.skip_bb_credit      0
S:port_ctrl.cm.use_shim_based_sublist 0
S:
S:      port_ctrl.serdes_set
S:=====
S:serdes_type      0x8
S:serdes_data_t.ibm_hss_serdes.tx_drive_power      0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b_sign 0x1
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b      0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_a      0x0
S:serdes_data_t.ibm_hss_serdes.rxeq      0x0
S:
S:      cfgbm
S:=====
S:old_distance      0x0      gport_lockdown      0x0
S:tport      0x1      speed      0x0
S:disable_eport      0x0      fcacc      0x0
S:lport_lockdown      0x0      0x0      priv_lport_lockdown
0x0
S:vcxlt_linit      0x0      delay_flogi      0x0
S:isl_interop      0x0      distance      0x0
S:BufStarvFlag      0x0      credit_sharing      0x0
S:lport_halfduplex      0x0      lport_fairness      0x0
S:soft_neg      0x0      asn_frc_hwretry      0x0
S:cr_recov      0x0      fport_buffers      0x0
S:export      0x0      0x0      export_mode
0x0
S:csctl_en      0x0      mirror_port      0x0
S:fault_delay      0x0      non_dfe      0x0
S:fec_configured*(0=ENAB)      0      fec_tts
0

```

S:port_persistently_disabled (permanently) 0 (0)

S:

S: cfg property

S:=====

S:priv_pcfg_bm 0x00000000 lgcl_pcfg_bm
0xbb844664

S:fport_buffer 0x00000000

S:

S:

S:C4 Discard Cntrs: rxlp_stats = 0xb6ae2430

S:-----

S:disc_mcast_wka 0x0 disc_inv_did 0x0
S:disc_cl1_cl4 0x0 disc_sid_chk_fail 0x0
S:disc_inv_dom_egid_txpt 0x0 disc_vft_hop_cnt_1
0x0
S:disc_classf 0x0 disc_fcp_cdb_inv 0x0
S:disc_vfid_trap_enabled 0x0
disc_vfid_hdr_chk_fail 0x0
S:disc_shim_cksum_fail 0x0 disc_fed_edit_cmd_err 0x0
S:disc_shim_cksum_fail 0x0 disc_fed_edit_cmd_err 0x0
S:disc_ftb_vm_mode 0x0 disc_ftb_agnt2_miss 0x0
S:disc_ecb_de_pad_err 0x0 disc_ecb_de_tag_err 0x0
S:disc_ecb_de_seq_err 0x0 disc_ecb_err 0x0
S:disc_ftb_type4_match 0x0 disc_fcp_rsp_ftb_type4 0x0
S:disc_fcp_rsp_ftb_type4 0x0 disc_ftb_type5_match
0x0
S:disc_ftb_type3_match 0x0 disc_els_ftb_type3 0x0
S:disc_ftb_type1_match 0x0 disc_els_rsp_ex_port 0x0
S:disc_inv_drp_dps 0x0 disc_did_lookup_miss 0x0
S:disc_ftb_type2_match 0x0 disc_trpd_plogi_pdisc 0x0
S:disc_type2_lookup_miss 0x0 disc_ftb_type6_match
0x0
S:disc_els_rep_ex_port 0x0 disc_els_sid_lkup_bit1 0x0
S:disc_els_sid_lkup_bit0 0x0
disc_bls_frm_trap_bit1 0x0
S:disc_ftb_token_err 0x0 disc_asic_internal_err 0x0
S:disc_hard_zone_miss 0x0 disc_lun_zone_miss 0x0
S:discflt_frame_disc 0x0 discflt_parity_err 0x0
S:disc_frame_marked_du 0x0 disc_frame_marked_to 0x0

E:Connection type: FE

E:Port type: F_port

E:Trunk port: No

E:Configured Speed: AUTO_SPEED_NEGO

E:Max Capable Speed: 32G

E:Current SNSM Speed: UNDEFINED

E:Hardware TX Speed: 32G (0x00000004)

E:Hardware RX Speed: 32G (0x00000040)

E:

E:Interrupts: 0 Link_failure: 0

Loss_of_sync: 0 Loss_of_sig: 0

E:Lli: 0 Invalid_word: 0

E:trapped_frm: 0 fwd_status_ok: 0

E:fwd_timeout: 0 fwd_tx_unavail: 0

```

E: fwd_unroutable:      0          fwd_zone_out:      0
E: fwd_other_err:      0          frm_err_discard:   0
E: Fltr listA:         0          Fltr listB:        0
E: Zone trap fwd:      0          Zone trap disc:    0
E: shim_csum:          0          RTE_perr:          0
E: Invalid_crc:        0          Delim_err:         0
E: Protocol_err:       0
E: Lr_in:              0          Lr_out:            0
E: Ols_in:             0          Ols_out:           0

```

filterportshow 40

FILTER DATA

Shadow settings:

```

Filter Enable: 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass: 0x00000000

```

Real settings:

```

Enable RAM: 0x00000000, 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000

```

Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass RAM: 0x00000000

Shadowed filters:

Filter 0: Not Installed (MIRROR1)(LISTA)
c4_fldenable[0] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[0] = 0x00000000,c4_fltr_config[0] = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
c4_fldenable[1] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[1] = 0x00000000,c4_fltr_config[1] = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
c4_fldenable[2] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[2] = 0x00000000,c4_fltr_config[2] = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
c4_fldenable[3] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[3] = 0x00000000,c4_fltr_config[3] = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
c4_fldenable[4] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[4] = 0x00000000,c4_fltr_config[4] = 0x00000000

Filter 5: Not Installed (ZONING TRAP)(LISTA)
c4_fldenable[5] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[5] = 0x00000000,c4_fltr_config[5] = 0x00000000

Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
c4_fldenable[6] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[6] = 0x00000000,c4_fltr_config[6] = 0x00000000

Filter 7: Not Installed (TIN TRAP)(LISTA)
c4_fldenable[7] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[7] = 0x00000000,c4_fltr_config[7] = 0x00000000

Filter 8: Not Installed (FICON CUP)(LISTA)
c4_fldenable[8] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[8] = 0x00000000,c4_fltr_config[8] = 0x00000000

Filter 9: Not Installed (FICON CUP DST)(LISTA)
c4_fldenable[9] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[9] = 0x00000000,c4_fltr_config[9] = 0x00000000

Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
c4_fldenable[10] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[10] = 0x00000000,c4_fltr_config[10] =
0x00000000

Filter 11: Not Installed (SIM)(LISTA)
c4_fldenable[11] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[11] = 0x00000000,c4_fltr_config[11] =
0x00000000

Filter 12: Not Installed (UNUSED)(LISTA)
c4_fldenable[12] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[12] = 0x00000000,c4_fltr_config[12] =
0x00000000

Filter 13: Not Installed (UNUSED)(LISTA)
c4_fldenable[13] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[13] = 0x00000000,c4_fltr_config[13] =
0x00000000

Filter 14: Not Installed (UNUSED)(LISTA)
c4_fldenable[14] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[14] = 0x00000000,c4_fltr_config[14] =
0x00000000

Filter 15: Not Installed (UNUSED)(LISTA)
c4_fldenable[15] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[15] = 0x00000000,c4_fltr_config[15] =
0x00000000

Filter 16: Not Installed (PERF1)(LISTA)
c4_fldenable[16] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[16] = 0x00000000,c4_fltr_config[16] =

```
0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
    c4_fldenable[17] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[17] = 0x00000000,c4_fltr_config[17] =
0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
    c4_fldenable[18] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[18] = 0x00000000,c4_fltr_config[18] =
0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
    c4_fldenable[19] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[19] = 0x00000000,c4_fltr_config[19] =
0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
    c4_fldenable[20] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[20] = 0x00000000,c4_fltr_config[20] =
0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
    c4_fldenable[21] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[21] = 0x00000000,c4_fltr_config[21] =
0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
    c4_fldenable[22] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[22] = 0x00000000,c4_fltr_config[22] =
0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
    c4_fldenable[23] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[23] = 0x00000000,c4_fltr_config[23] =
0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
    c4_fldenable[24] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[24] = 0x00000000,c4_fltr_config[24] =
0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
    c4_fldenable[25] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[25] = 0x00000000,c4_fltr_config[25] =
0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
    c4_fldenable[26] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[26] = 0x00000000,c4_fltr_config[26] =
0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
    c4_fldenable[27] = 0x00000000 0x00000000 0x00000000
0x00000000
```

```
    c4_fldnegate[27] = 0x00000000,c4_fltr_config[27] =
0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
    c4_fldenable[28] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[28] = 0x00000000,c4_fltr_config[28] =
0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
    c4_fldenable[29] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[29] = 0x00000000,c4_fltr_config[29] =
0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    c4_fldenable[30] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[30] = 0x00000000,c4_fltr_config[30] =
0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    c4_fldenable[31] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[31] = 0x00000000,c4_fltr_config[31] =
0x00000000
```

Real filters:

```
Filter 0: Not Installed (MIRROR1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
```

Filter 7: Not Installed (TIN TRAP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 8: Not Installed (FICON CUP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 9: Not Installed (FICON CUP DST)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 11: Not Installed (SIM)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 12: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 13: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 14: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 15: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 16: Not Installed (PERF1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 17: Not Installed (PERF2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 18: Not Installed (PERF3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 19: Not Installed (PERF4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 20: Not Installed (PERF5)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,

0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter dirty indicator: 0x00000000
Performance filters: 0
Port Mirror filters: 0 (0x0)

FIELD DATA

Shadowed fields:

```
fldoffset[0] = 0x00, fldmask[0] = 0x00, fldvalue_dyna[0]:0x00 0x00
0x00 0x00
fldcontrol[0].inuse = 0x0  fldcontrol[0].refcnt = 0x00 0x00 0x00
0x00
fldoffset[1] = 0x00, fldmask[1] = 0x00, fldvalue_dyna[1]:0x00 0x00
0x00 0x00
fldcontrol[1].inuse = 0x0  fldcontrol[1].refcnt = 0x00 0x00 0x00
0x00
fldoffset[2] = 0x00, fldmask[2] = 0x00, fldvalue_dyna[2]:0x00 0x00
0x00 0x00
fldcontrol[2].inuse = 0x0  fldcontrol[2].refcnt = 0x00 0x00 0x00
0x00
fldoffset[3] = 0x00, fldmask[3] = 0x00, fldvalue_dyna[3]:0x00 0x00
0x00 0x00
fldcontrol[3].inuse = 0x0  fldcontrol[3].refcnt = 0x00 0x00 0x00
0x00
fldoffset[4] = 0x00, fldmask[4] = 0x00, fldvalue_dyna[4]:0x00 0x00
0x00 0x00
fldcontrol[4].inuse = 0x0  fldcontrol[4].refcnt = 0x00 0x00 0x00
0x00
fldoffset[5] = 0x00, fldmask[5] = 0x00, fldvalue_dyna[5]:0x00 0x00
0x00 0x00
fldcontrol[5].inuse = 0x0  fldcontrol[5].refcnt = 0x00 0x00 0x00
0x00
fldoffset[6] = 0x00, fldmask[6] = 0x00, fldvalue_dyna[6]:0x00 0x00
0x00 0x00
fldcontrol[6].inuse = 0x0  fldcontrol[6].refcnt = 0x00 0x00 0x00
0x00
fldoffset[7] = 0x00, fldmask[7] = 0x00, fldvalue_dyna[7]:0x00 0x00
0x00 0x00
fldcontrol[7].inuse = 0x0  fldcontrol[7].refcnt = 0x00 0x00 0x00
0x00
fldoffset[8] = 0x00, fldmask[8] = 0x00, fldvalue_dyna[8]:0x00 0x00
0x00 0x00
fldcontrol[8].inuse = 0x0  fldcontrol[8].refcnt = 0x00 0x00 0x00
0x00
fldoffset[9] = 0x00, fldmask[9] = 0x00, fldvalue_dyna[9]:0x00 0x00
0x00 0x00
fldcontrol[9].inuse = 0x0  fldcontrol[9].refcnt = 0x00 0x00 0x00
0x00
fldoffset[10] = 0x00, fldmask[10] = 0x00, fldvalue_dyna[10]:0x00 0x00
0x00 0x00
fldcontrol[10].inuse = 0x0  fldcontrol[10].refcnt = 0x00 0x00 0x00
0x00
fldoffset[11] = 0x00, fldmask[11] = 0x00, fldvalue_dyna[11]:0x00 0x00
0x00 0x00
fldcontrol[11].inuse = 0x0  fldcontrol[11].refcnt = 0x00 0x00 0x00
0x00
fldoffset[12] = 0x00, fldmask[12] = 0x00, fldvalue_dyna[12]:0x00 0x00
0x00 0x00
fldcontrol[12].inuse = 0x0  fldcontrol[12].refcnt = 0x00 0x00 0x00
```


0x00000000
0x00000000
0x00000000

Field dirty indicator: 0x00000000

FDB reference count fdb: 0 [0 0 0 0]
FDB reference count fdb: 1 [0 0 0 0]
FDB reference count fdb: 2 [0 0 0 0]
FDB reference count fdb: 3 [0 0 0 0]
FDB reference count fdb: 4 [0 0 0 0]
FDB reference count fdb: 5 [0 0 0 0]
FDB reference count fdb: 6 [0 0 0 0]
FDB reference count fdb: 7 [0 0 0 0]
FDB reference count fdb: 8 [0 0 0 0]
FDB reference count fdb: 9 [0 0 0 0]
FDB reference count fdb: 10 [0 0 0 0]
FDB reference count fdb: 11 [0 0 0 0]
FDB reference count fdb: 12 [0 0 0 0]
FDB reference count fdb: 13 [0 0 0 0]
FDB reference count fdb: 14 [0 0 0 0]
FDB reference count fdb: 15 [0 0 0 0]
FDB reference count fdb: 16 [0 0 0 0]
FDB reference count fdb: 17 [0 0 0 0]
FDB reference count fdb: 18 [0 0 0 0]
FDB reference count fdb: 19 [0 0 0 0]

Filter counters:

Filter counter 0: 0 (MIRROR1)
Filter counter 1: 0 (MIRROR2)
Filter counter 2: 0 (MIRROR3)
Filter counter 3: 0 (MIRROR4)
Filter counter 4: 0 (AEPORT_NON_MIRR_DROP)
Filter counter 5: 0 (ZONING TRAP)
Filter counter 6: 0 (FCR_EXPORT_DC)
Filter counter 7: 0 (TIN TRAP)
Filter counter 8: 0 (FICON CUP)
Filter counter 9: 0 (FICON CUP DST)
Filter counter 10: 0 (WELL KNOWN ADDR)
Filter counter 11: 0 (SIM)
Filter counter 12: 0 (UNUSED)
Filter counter 13: 0 (UNUSED)
Filter counter 14: 0 (UNUSED)
Filter counter 15: 0 (UNUSED)
Filter counter 16: 0 (PERF1)
Filter counter 17: 0 (PERF2)
Filter counter 18: 0 (PERF3)
Filter counter 19: 0 (PERF4)
Filter counter 20: 0 (PERF5)
Filter counter 21: 0 (PERF6)
Filter counter 22: 0 (PERF7)
Filter counter 23: 0 (PERF8)
Filter counter 24: 0 (PERF9)
Filter counter 25: 0 (PERF10)
Filter counter 26: 0 (PERF11)

Filter counter 27: 0 (PERF12)
Filter counter 28: 0 (OPM1)
Filter counter 29: 0 (OPM2)
Filter counter 30: 0 (IPM1)
Filter counter 31: 0 (IPM2)

ACL DATA

Logical port 22: Hard Zoning disabled, Soft Zoning disabled
Zone type: WWN Zoning
Frames with hard zone miss: 0

*** Please use filterportshow on user port 56 to display ACL hash tables and Mirroring resources of thischip.
***We show this data only for the first physical port which is an external port.

portFcPortCmdShow --slot 0 41 3
doing portFcPortCmdShow: arg1 = 3, arg2 = -2

portshow 41
portDisableReason: None
portCFlags: 0x1
portFlags: 0x1 PRESENT U_PORT
LocalSwcFlags: 0x0
portType: 26.0
POD Port: Port is licensed
portState: 2 Offline
Protocol: FC
portPhys: 4 No_Light portScn: 2 Offline
port generation number: 0
state transition count: 1

portId: 012900
portIfId: 43020015
portWwn: 20:29:d8:1f:cc:2c:99:90
portWwn of device(s) connected:
16b Area list:
Distance: normal
portSpeed: N32Gbps

FEC: Inactive
Credit Recovery: Inactive
LE domain: 0
Peer beacon: Off
FC Fastwrite: OFF

| | | | | |
|-------------|---|---------------|---|-------|
| Interrupts: | 0 | Link_failure: | 0 | Frjt: |
| 0 | | | | |
| Unknown: | 0 | Loss_of_sync: | 0 | Fbsy: |
| 0 | | | | |
| Lli: | 0 | Loss_of_sig: | 0 | |
| Proc_rqrd: | 0 | Protocol_err: | 0 | |
| Timed_out: | 0 | Invalid_word: | 0 | |
| Tx_unavail: | 0 | Invalid_crc: | 0 | |

```

Delim_err:      0          Address_err: 0
Lr_in:          0          0ls_in:      0
Lr_out:         0          0ls_out:     0

```

portloginshow 41

```

Type  PID      World Wide Name      credit df_sz cos
=====

```

portloginshow 41 -history

```

Type  PID      World Wide Name      logout time
=====

```

portregshow 41

LED registers

=====

```

0x81caa000: c4_led_status      00000000      0x81caa004:
c4_led_ctl      00000000

```

FPL registers

=====

```

0x81ca8200: fpl_port_config      23298002
0x81ca820c: fpl_port_id_ctl      00000000      0x81ca8210:
fpl_port_id_addr      00012900
0x81ca8214: fpl_port_speed      00000004      0x81ca821c:
fpl_lli_ctl      00000100
0x81ca8228: fpl_lli_os_ctl      bc94ffff      0x81ca822c:
fpl_lli_send_word      bc95b5b5
0x81ca8230: fpl_lli_mark_rx      00000000      0x81ca8234:
fpl_lli_rnd_trip_time      00000000
0x81ca8238: fpl_lli_ns_status      00130007      0x81ca823c:
fpl_lli_intr_status      00030007
0x81ca8244: fpl_lli_def      00100000      0x81ca8254:
fpl_lli_intr_enable_clr      001c0000
0x81ca8258: fpl_err_intr_status      00000000      0x81ca8260:
fpl_err_intr_enable_clr      00000000
0x81ca8268: fpl_err_first_error      00000000      0x81ca826c:
fpl_speed_neg_ctl      00000000
0x81ca8270: fpl_speed_neg_stat      00000000      0x81ca8274:
fpl_softasn_ctl      0000000f
0x81ca8278: fpl_link_init_ctl      00000000      0x81ca827c:
fpl_link_init_stat      00000000
0x81ca8280: fpl_aec_ctl      001c1060      0x81ca8284:
fpl_aec_ctl2      04009f60
0x81ca8288: fpl_pcs_ctl      00000170      0x81ca828c:
fpl_fec_ctl      00000424
0x81ca8290: fpl_fec_cor      00000000      0x81ca8294:
fpl_fec_uncor      00000000
0x81ca8298: fpl_hss_link_ctl      0031f040      0x81ca829c:
fpl_afifo_link_ctl      00000a86
0x81ca82a0: fpl_echo_lb_ctl      0000028c      0x81ca82a4:

```

```

fpl_scratch          00000121
0x81ca82a8: fpl_debug          00060005    0x81ca82ac:
fpl_misc_debug      00000800
0x00000000: SW_shadow_reg        00000000    0x00000000:
SW_c4_phyp->cfgptr   00030003

```

per-fpg (per octet) registers

```

=====
0x8181382c: fpg_serdes_ctla0      81a37be7    0x81813830:
fpg_serdes_ctla1      81a37be7
0x81813834: fpg_serdes_ctlb0      81a1c3c3    0x81813838:
fpg_serdes_ctlb1      81a1c3c3
0x8181383c: fpg_serdes_xgmii_1ms 00067c28    0x81813840:
fpg_serdes_regtimctl  40e47946
0x81813844: fpg_serdes_asnrsttimctl 00000102

```

HSS PLL registers

```

=====
0x81813400: 00_hssplla_vco_coarse_cal0 00000000    0x81813404:
01_hssplla_vco_coarse_cal1 00000014
0x81813408: 02_hssplla_vco_coarse_cal2 00000000    0x8181340c:
03_hssplla_vco_coarse_cal3 00000000
0x81813410: 04_hssplla_vco_coarse_cal4 00000000    0x81813424:
09_hssplla_power_ctl 00000000
0x81813428: 0A_hssplla_charge_pump_ctl 00000004    0x81813438:
0E_hssplla_pll_misc_ctl 00000000
0x8181343c: 0F_hssplla_pclk_ctl 000000f8    0x81813440:
10_hssplla_eyem_intv_ctl 00000000
0x81813444: 11_hssplla_eyem_intv_lim1 00000000    0x81813448:
12_hssplla_eyem_intv_lim2 00000000
0x8181344c: 13_hssplla_eyem_intv_lim3 00000000    0x81813450:
14_hssplla_eyem_intv_lim4 00000000
0x818134f0: 3C_hssplla_macro_tst_ctl4 00000000    0x818134f4:
3D_hssplla_macro_tst_ctl3 00000000
0x818134f8: 3E_hssplla_macro_tst_ctl2 00000000    0x818134fc:
3F_hssplla_macro_tst_ctl1 00000000
0x81813500: 00_hssppll_vco_coarse_cal0 0000000a    0x81813504:
01_hssppll_vco_coarse_cal1 00000014
0x81813508: 02_hssppll_vco_coarse_cal2 00000000    0x8181350c:
03_hssppll_vco_coarse_cal3 00000000
0x81813510: 04_hssppll_vco_coarse_cal4 00000000    0x81813524:
09_hssppll_power_ctl 00000000
0x81813528: 0A_hssppll_charge_pump_ctl 00000004    0x81813538:
0E_hssppll_pll_misc_ctl 00000000
0x8181353c: 0F_hssppll_pclk_ctl 000000f8    0x81813540:
10_hssppll_eyem_intv_ctl 00000000
0x81813544: 11_hssppll_eyem_intv_lim1 00000000    0x81813548:
12_hssppll_eyem_intv_lim2 00000000
0x8181354c: 13_hssppll_eyem_intv_lim3 00000000    0x81813550:
14_hssppll_eyem_intv_lim4 00000000
0x818135f0: 3C_hssppll_macro_tst_ctl4 00000000    0x818135f4:
3D_hssppll_macro_tst_ctl3 00000000
0x818135f8: 3E_hssppll_macro_tst_ctl2 00000000    0x818135fc:
3F_hssppll_macro_tst_ctl1 00000000

```

HSS TX registers

=====

| | | |
|---|----------|-------------|
| 0x81812100: 00_hsstx_cfg_mode_PHY | 00009f48 | 0x81812104: |
| 01_hsstx_test_ctl | 00000000 | |
| 0x81812108: 02_hsstx_coeff_ctl_INV | 00000000 | 0x8181210c: |
| 03_hsstx_drv_mode_ctl | 00000000 | |
| 0x81812110: 04_hsstx_drv_ovrd_ctl | 00000010 | 0x81812114: |
| 05_hsstx_dclk_align_ovrd | 00000080 | |
| 0x81812118: 06_hsstx_imp_cal_ovrd | 00000c0c | 0x8181211c: |
| 07_hsstx_dclk_drift_tol | 00000004 | |
| 0x81812120: 08_hsstx_tap0_coeff_TUNE | 00000000 | 0x81812124: |
| 09_hsstx_tap1_coeff_TUNE | 00000003 | |
| 0x81812128: 0A_hsstx_tap2_coeff_TUNE | 00000019 | 0x8181212c: |
| 0B_hsstx_tap3_coeff_TUNE | 00000003 | |
| 0x81812134: 0D_hsstx_pol_INV | 00000004 | 0x81812138: |
| 0E_hsstx_ae_cmd | 00000000 | |
| 0x8181213c: 0F_hsstx_ae_stat | 00000000 | 0x81812140: |
| 10_hsstx_ae_tap0_TUNE | 00000000 | |
| 0x81812144: 11_hsstx_ae_tap1_TUNE | 00000000 | 0x81812148: |
| 12_hsstx_ae_tap2_TUNE | 00000028 | |
| 0x8181214c: 13_hsstx_ae_tap3_TUNE | 00000000 | 0x81812154: |
| 15_hsstx_app_tune | 0000120e | |
| 0x81812158: 16_hsstx_analog_diag | 00000000 | 0x81812160: |
| 18_hsstx_4x_seg_app | 0000aa00 | |
| 0x81812164: 19_hsstx_2x_seg_app | 000000aa | 0x81812168: |
| 1A_hsstx_1x_seg_app | 0000f5e4 | |
| 0x8181216c: 1B_hsstx_seg_4x_term_app | 0000000f | 0x81812170: |
| 1C_hsstx_seg_2x1x_term_app | 00000001 | |
| 0x81812174: 1D_hsstx_tap_sign_app | 00000004 | 0x81812178: |
| 1E_hsstx_ext_addr_data | 00000001 | |
| 0x8181217c: 1F_hsstx_ext_addr_addr | 00000000 | 0x81812180: |
| 20_hsstx_pat_buf_bytes_1_0 | 00000000 | |
| 0x81812184: 21_hsstx_pat_buf_bytes_3_2 | 00000000 | 0x81812188: |
| 22_hsstx_pat_buf_bytes_5_4 | 00000000 | |
| 0x8181218c: 23_hsstx_pat_buf_bytes_7_6 | 00000000 | 0x8181219c: |
| 27_hsstx_8023az_ctl | 00000000 | |
| 0x818121a0: 28_hsstx_dcc_ctl | 000060c0 | 0x818121a4: |
| 29_hsstx_dcc_ovrd | 00000000 | |
| 0x818121a8: 2A_hsstx_dcc_app | 00000000 | 0x818121ac: |
| 2B_hsstx_dcc_timeout | 0000ffff | |
| 0x818121c0: 30_hsstx_tap_sign_ovrd | 00000000 | 0x818121c8: |
| 32_hsstx_seg_4x_ovrd | 00000000 | |
| 0x818121cc: 33_hsstx_seg_2x_ovrd | 00000000 | 0x818121d0: |
| 34_hsstx_seg_1x_ovrd | 00000000 | |
| 0x818121d8: 36_hsstx_tap_seg_4x_term_ovrd | 00000000 | 0x818121dc: |
| 37_hsstx_tap_seg_2x_term_ovrd | 00000000 | |
| 0x818121e0: 38_hsstx_tap_seg_1x_term_ovrd | 00000000 | 0x818121ec: |
| 3B_hsstx_mac_test_ctl5 | 00000000 | |
| 0x818121f0: 3C_hsstx_mac_test_ctl4 | 00000000 | 0x818121f4: |
| 3D_hsstx_mac_test_ctl3 | 00000000 | |
| 0x818121f8: 3E_hsstx_mac_test_ctl2 | 00000000 | 0x818121fc: |
| 3F_hsstx_mac_test_ctl1 | 000000c6 | |

HSS RX registers

=====

| | | |
|---|----------|-------------|
| 0x81812300: 00_hssrx_cfg_mode_PHY | 00009e78 | 0x81812304: |
| 01_hssrx_test_ctl | 00000000 | |
| 0x81812308: 02_hssrx_phs_rot_ctl | 0000cb80 | 0x8181230c: |
| 03_hssrx_phs_rot_ofs_ctl | 00001610 | |
| 0x81812310: 04_hssrx_phs_rot_posn1 | 00001616 | 0x81812314: |
| 05_hssrx_phs_rot_posn2 | 00000005 | |
| 0x81812318: 06_hssrx_phs_rot_sta_ofs1 | 00000000 | 0x8181231c: |
| 07_hssrx_phs_rot_sta_ofs2 | 00000000 | |
| 0x81812320: 08_hssrx_dfe_ctl_PHY | 00002002 | 0x81812324: |
| 09_hssrx_dfe_smpl_snap1 | 00000000 | |
| 0x81812328: 0A_hssrx_dfe_smpl_snap2 | 00008000 | 0x8181232c: |
| 0B_hssrx_vga_ctl1 | 00004001 | |
| 0x81812330: 0C_hssrx_vga_ctl2 | 00007aa0 | 0x81812334: |
| 0D_hssrx_vga_ctl3 | 000009e4 | |
| 0x81812338: 0E_hssrx_pwr_mgmt_ctl | 0000001f | 0x8181233c: |
| 0F_hssrx_iqamp_ctl1 | 0000001a | |
| 0x81812340: 10_hssrx_iqamp_ctl2 | 00000004 | 0x81812344: |
| 11_hssrx_dacap_dacan_sel | 00000003 | |
| 0x81812348: 12_hssrx_dacap_dacan | 0000ffff | 0x8181234c: |
| 13_hssrx_daca_min | 00000000 | |
| 0x81812350: 14_hssrx_adac_ctl | 00000000 | 0x81812354: |
| 15_hssrx_ac_cp_ctl | 000031c3 | |
| 0x81812358: 16_hssrx_ac_cp_val | 00008054 | 0x8181235c: |
| 17_hssrx_dfe_h1h2h3_lcl_off_ch | 00000014 | |
| 0x81812360: 18_hssrx_dfe_h1h2h3_lcl_off_val | 00000000 | 0x81812364: |
| 19_hssrx_peaked_intg | 000000ff | |
| 0x81812368: 1A_hssrx_cdr_analog_sw | 0000ce00 | 0x8181236c: |
| 1B_hssrx_peaking_amp_init_c_PHY | 00000000 | |
| 0x81812370: 1C_hssrx_dac_dpc | 00000040 | 0x81812374: |
| 1D_hssrx_ddc | 00000000 | |
| 0x81812378: 1E_hssrx_int_stat_PHY | 00001c0f | 0x8181237c: |
| 1F_hssrx_dfe_func_ctl1_PHY | 0000ffff | |
| 0x81812380: 20_hssrx_dfe_func_ctl2_INV | 00007ebf | 0x81812384: |
| 21_hssrx_ofs_ch_dcc_qcc_idx | 00002000 | |
| 0x81812388: 22_hssrx_dfe_ofs_val | 0000797f | 0x8181238c: |
| 23_hssrx_h_coeff_bist | 0000040d | |
| 0x81812390: 24_hssrx_ac_cap_bist | 00000067 | 0x81812394: |
| 25_hssrx_max_gain_path_idx_res | 00007800 | |
| 0x81812398: 26_hssrx_loff_ctl | 00000040 | 0x8181239c: |
| 27_hssrx_sigdet_ctl | 00002380 | |
| 0x818123a0: 28_hssrx_ana_ctl_sw | 00000000 | 0x818123a4: |
| 29_hssrx_intg_dac_ofs | 0000dce3 | |
| 0x818123a8: 2A_hssrx_eye_ctl | 00000000 | 0x818123ac: |
| 2B_hssrx_eye_met | 00000004 | |
| 0x818123b0: 2C_hssrx_eye_met_err_cnt | 00000000 | 0x818123b4: |
| 2D_hssrx_eye_met_pdf_eyec | 00000000 | |
| 0x818123b8: 2E_hssrx_eye_met_pat_len | 0000007f | 0x818123bc: |
| 2F_hssrx_dfe_func_ctl3 | 0000dfff | |
| 0x818123c0: 30_hssrx_dfe_tap_ctl_idx_ptr | 00000008 | 0x818123c4: |
| 31_hssrx_dfe_tap | 00003030 | |
| 0x818123c8: 32_hssrx_lte_ctl_TUNE | 00001601 | 0x818123e4: |
| 39_hssrx_int_stat2 | 0000c1ff | |

```

0x818123e8: 3A_hssrx_ac_cpl_cur_src_adj      00000041    0x818123ec:
3B_hssrx_dcd_ctl                      00007c41
0x818123f0: 3C_hssrx_dcc_ctl                    00000d81    0x818123f4:
3D_hssrx_qcc_ctl                      00006983
0x818123f8: 3E_hssrx_mac_test_ctl2             00000000    0x818123fc:
3F_hssrx_mac_test_ctl1                00000000
0x81812348: 12_hssrx_dacap_dacan[02]          00f9 fffd
0x81812360: 18_hssrx_dfe_h1h2h3_lcl_off_va[00] 0000 0000    0000
0000 0000 0000 0000 0000
0x81812360: 18_hssrx_dfe_h1h2h3_lcl_off_va[08] 0000 0000    0000
0000 0000 0000 0000 0000
0x81812360: 18_hssrx_dfe_h1h2h3_lcl_off_va[16] 0000 0000    0000
0000 0000
0x81812388: 22_hssrx_dfe_ofs_val[00][00]      797f 0000    030b
7f7f 7b7f 0000
0x81812388: 22_hssrx_dfe_ofs_val[03][00]      7f7f 0000    7d7d
0000 0301 7f7f
0x81812388: 22_hssrx_dfe_ofs_val[06][00]      7c7d 0000    030d
7f7f 017f 0000
0x81812388: 22_hssrx_dfe_ofs_val[09][00]      7f01 0000    797f
0000 077d 7f00
0x81812388: 22_hssrx_dfe_ofs_val[12][00]      037f 7f00    017d
7f00 7f05 0000
0x81812388: 22_hssrx_dfe_ofs_val[15][00]      057e 7f00    7d03
0000 0509 7f7f
0x81812388: 22_hssrx_dfe_ofs_val[18][00]      7b79 0000    7908
007f 0001 0000
0x81812388: 22_hssrx_dfe_ofs_val[21][00]      0001 0000    0001
0000 0001 0000
0x81812388: 22_hssrx_dfe_ofs_val[24][00]      0204 007f    7c06
007f 7e7a 0000
0x81812394: 25_hssrx_max_gain_path_idx_res[00] 0058 0848    1012
189c 20ef 28af 3097 3800
0x81812394: 25_hssrx_max_gain_path_idx_res[08] 40cf 4895    5082
5800 6044 6800 70f3 7800
0x818123c4: 31_hssrx_dfe_tap[00]              fffe 8080    0000
0000 0030 0030 3030 3030
0x818123c4: 31_hssrx_dfe_tap[08]              3030 3030    3030
0000
0x818123e8: 3A_hssrx_ac_cpl_cur_src_adj[00]    0041 0041    0041
0041
0x818123ec: 3B_hssrx_dcd_ctl[00]              7c41 5c00    7c86
5c00 7c82
0x818123f0: 3C_hssrx_dcc_ctl[00]              0d81 0d82    0d82
0d81
0x818123f4: 3D_hssrx_qcc_ctl[00]              6948 6983

```

xfipcs, fec, aec, & aet registers

=====

```

0x81ca8400: xfipcs_reg [00] 00002040 00000080 00000000
00000000 00000001 00000008 00000000 00000000
0x81ca8420: xfipcs_reg [08] 00008401 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81ca8440: xfipcs_reg [16] 00000000 00000000 00000000

```

```

00000000 00000040 00000000 00000000 00000000
0x81ca8460: xfipcs_reg [24] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81ca8480: xfipcs_reg [32] 00000004 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81ca8620: fec_32g_128g_reg [08] 00000000 00008003 00000000
00000000 00000000 00000000 00000000
0x81ca8648: fec_32g_128g_reg [18] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81ca8a00: aec_reg [00] 00000000 00000000 00000000
00000000 00000040 00000000 00000000 00002490
0x81ca8c00: aet_reg [00] 000000b0 00007000 000008c4
00000000 00000000

```

bbc registers

=====

```

0x81ca9800: bbc_trc 0 0 0 0 0 0 0
0
0x81ca9840: bbc_trc 0 0 0 0 0 0 0
0
0x81ca9880: bbc_trc 0 0 0 0 0 0 0
0
0x81ca98c0: bbc_trc 0 0 0 0 0 0 0
0
0x81ca9900: bbc_trc 0 0 0 0 0 0 0
0
0x81ca9804: bbc_mbc 0 0 0 0 0 0 0
0
0x81ca9844: bbc_mbc 0 0 0 0 0 0 0
0
0x81ca9884: bbc_mbc 0 0 0 0 0 0 0
0
0x81ca98c4: bbc_mbc 0 0 0 0 0 0 0
0
0x81ca9904: bbc_mbc 0 0 0 0 0 0 0
0
0x81ca9a00: bbc_rcc 0 0 0 0 0 0 0
0
0x81ca9a20: bbc_rcc 0 0 0 0 0 0 0
0
0x81ca9a40: bbc_rcc 0 0 0 0 0 0 0
0
0x81ca9a60: bbc_rcc 0 0 0 0 0 0 0
0
0x81ca9a80: bbc_rcc 0 0 0 0 0 0 0
0
0x81ca9c00: bbc_rqc 0 0 0 0 0 0 0
0
0x81ca9c20: bbc_rqc 0 0 0 0 0 0 0
0
0x81ca9c40: bbc_rqc 0 0 0 0 0 0 0
0
0x81ca9c60: bbc_rqc 0 0 0 0 0 0 0
0

```

| | | | | | | | |
|-------------------------------------|----------|---|---|---|---|----------------------|---|
| 0x81ca9c80: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81ca9d00: bbc_fbpc | 00000000 | | | | | 0x81ca9d04: bbc_csc | |
| 00000000 | | | | | | | |
| 0x81ca9d08: bbc_rcc_inc | 00000000 | | | | | 0x81ca9d0c: | |
| bbc_rqc_inc | 00000000 | | | | | | |
| 0x81ca9d10: bbc_fbpc_inc | 00000000 | | | | | 0x81ca9d14: | |
| bbc_tmc_inc | 00000000 | | | | | | |
| 0x81ca9d18: bbc_threshold | 00080100 | | | | | 0x81ca9d1c: | |
| bbc_counter_clr | 00000000 | | | | | | |
| 0x81ca9d20: bbc_debug_en | 00000000 | | | | | 0x81ca9d24: bbc_ctrl | |
| 00200120 | | | | | | | |
| 0x81ca9d28: bbc_rqc_rcc_thresh | 00000055 | | | | | 0x81ca9d34: | |
| bbc_bb_sc_n | 00000000 | | | | | | |
| 0x81ca9d38: bbc_crd_reco_debug | 00000000 | | | | | 0x81ca9d3c: | |
| bbc_crd_reco_debug_data | 00000000 | | | | | | |
| 0x81ca9d40: bbc_multi_frm_loss_cnt | 00000000 | | | | | 0x81ca9d44: | |
| bbc_multi_rdy_loss_cnt | 00000000 | | | | | | |
| 0x81ca9d48: bbc_1frm_loss_recov_cnt | 00000000 | | | | | 0x81ca9d4c: | |
| bbc_1rdy_loss_recov_cnt | 00000000 | | | | | | |
| 0x81ca9d58: bbc_int_status | 00000000 | | | | | 0x81ca9d5c: | |
| bbc_int_set | 00000000 | | | | | | |
| 0x81ca9d60: bbc_int_first | 00000000 | | | | | 0x81ca9d64: | |
| bbc_frm_rdy_rx_err_addr | 00000000 | | | | | | |
| 0x81ca9d68: bbc_frm_rdy_tx_err_addr | 00000000 | | | | | 0x81ca9d6c: | |
| bbc_trc_mbc_err_addr | 00000000 | | | | | | |
| 0x81ca9d70: bbc_frm_rdy_rx_dbl_ecc | 00000000 | | | | | 0x81ca9d74: | |
| bbc_frm_rdy_tx_dbl_ecc | 00000000 | | | | | | |
| 0x81ca9d78: bbc_trc_mbc_dbl_ecc | 00000000 | | | | | | |
| 0x81ca9d7c: bbc_fsm_status | 00001011 | | | | | 0x81ca9d80: | |
| bbc_force_err | 00000000 | | | | | | |
| 0x81ca9d84: bbc_crdt_avail0 | 00000000 | | | | | 0x81ca9d88: | |
| bbc_crdt_avail1 | 00000000 | | | | | | |
| 0x81ca9d8c: bbc_scratch | 00000000 | | | | | | |

FPS registers

=====

| | | | | | | | |
|--------------------------------|----------|--|--|--|--|-------------|--|
| 0x81ca8004: fps_er_enc_in | 00000000 | | | | | 0x81ca8008: | |
| fps_er_crc | 00000000 | | | | | | |
| 0x81ca800c: fps_er_trunc | 00000000 | | | | | 0x81ca8010: | |
| fps_er_toolong | 00000000 | | | | | | |
| 0x81ca8014: fps_er_bad_eof | 00000000 | | | | | 0x81ca8018: | |
| fps_er_enc_out | 00000000 | | | | | | |
| 0x81ca801c: fps_er_bad_os | 00000000 | | | | | 0x81ca8020: | |
| fps_er_flush | 00000000 | | | | | | |
| 0x81ca8024: fps_er_ifg | 00000000 | | | | | 0x81ca8038: | |
| fps_er_crc_good_eof | 00000000 | | | | | | |
| 0x81ca803c: fps_inv_arb | 00000000 | | | | | 0x81ca8040: | |
| fps_slow_sts_status | 00000000 | | | | | | |
| 0x81ca8044: fps_tx_frm_cnt | 00000000 | | | | | 0x81ca8048: | |
| fps_rx_frm_cnt | 00000000 | | | | | | |
| 0x81ca8050: fps_tx_word_cnt_hi | 00000000 | | | | | 0x81ca804c: | |
| fps_tx_word_cnt_lo | 00000000 | | | | | | |
| 0x81ca8058: fps_rx_word_cnt_hi | 00000000 | | | | | 0x81ca8054: | |

fps_rx_word_cnt_lo 00000000

BAL registers

=====

0x81caf000: bal_desired_buf 00000000 0x81caf004:
bal_alloc_buf 00000000
0x81caf008: bal_busy_buf 00000000 0x81caf00c:
bal_usable_buf 00000000
0x81caf010: bal_max_bor_buf 00000000
0x81caf014: bal_busy_buf_thresh 00000002

TXQ registers

=====

0x81cab004: txq_phys_port_ctl 00450000
0x81cab050: txq_link_skew 00000000
0x81cab068: txq_cr_lk_dttm_intr_sts [00] 00000000 00000000
0x81cab070: txq_cr_lk_dttm_intr_en [00] 00000000 00000000
0x81cab024: txq_disc_frm_trap_cnt 00000014

FDS registers

=====

0x81cac000: fds_rxf_ctl 00000002 0x81cac004:
fds_rxf_wait_thresh 00000909
0x81cac018: fds_rxf_first_error 00000000 0x81cac01c:
fds_rxf_first_error_info 00000000
0x81cac020: fds_rxf_inout_pkt_cnt 00000000
0x81cac008: fds_rxf_err_int_status 00000000 0x81cac024:
fds_rxf_fifo_status 00888888
0x81cad000: fds_txf_ctl 0000003a 0x81cad004:
fds_txf_wait_ifg_thresh 00a00106
0x81cad008: fds_txf_err_int_status 00000000 0x81cad024:
fds_txf_fifo_status 00088888
0x81cad02c: fds_txf_bbc_scs 00000000

Logical TXQ registers

=====

0x81cab000: txq_log_port_ctl 00000002 0x81cab008:
txq_port_status 00000000
0x81cab00c: txq_todo_flags [00] 00000000 00000000
0x81cab014: txq_spd_match_desc [00] 00000000 00000000 00000000
00000000
0x81cab024: txq_spd_match_desc [04] 00000014
0x81cab028: txq_vc_weight [00] 01010101 01010101 01010101
01010101
0x81cab038: txq_vc_weight [04] 01010101 01010101 01010101
01010101
0x81cab048: txq_vc_weight [08] 01010101 00010101
0x81cab054: txq_cong_dttm_ctrl 00000106
0x81cab058: txq_cong_dttm_intr_sts [00] 00000000 00000000
0x81cab060: txq_cong_dttm_intr_en [00] 00000000 00000000
0x81cab078: txq_bw_limit_en_reg [00] 00000000 00000000
0x81cab080: txq_bw_gua_en_reg [00] 00000000 00000000
0x81cab088: txq_vc_group [00] 03030300 03030303 03030303
03030303

| | | | | |
|---------------------------------|------|----------|----------|----------|
| 0x81cab098: txq_vc_group | [04] | 03030303 | 03030303 | 03030303 |
| 03030303 | | | | |
| 0x81cab0a8: txq_vc_group | [08] | 03030303 | 03030303 | 00000000 |
| 00000000 | | | | |
| 0x81cab0b0: txq_bw_thresh_group | [00] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81cab0c0: txq_bw_thresh_group | [04] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81cab0d0: txq_bw_thresh_group | [08] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81cab0e0: txq_bw_thresh_group | [12] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81cab0f0: txq_bw_thresh_group | [16] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81cab100: txq_bw_thresh_group | [20] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81cab110: txq_bw_thresh_group | [24] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81cab120: txq_bw_thresh_group | [28] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81cab130: txq_bw_thresh_group | [32] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81cab140: txq_bw_thresh_group | [36] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |

txq Congestion detection Statistics RAM

```

=====
0x81090d20: vc[0]      00000000      0x81090d24: vc[1]
00000000
0x81090d28: vc[2]      00000000      0x81090d2c: vc[3]
00000000
0x81090d30: vc[4]      00000000      0x81090d34: vc[5]
00000000
0x81090d38: vc[6]      00000000      0x81090d3c: vc[7]
00000000
0x81090d40: vc[8]      00000000      0x81090d44: vc[9]
00000000
0x81090d48: vc[10]     00000000      0x81090d4c: vc[11]
00000000
0x81090d50: vc[12]     00000000      0x81090d54: vc[13]
00000000
0x81090d58: vc[14]     00000000      0x81090d5c: vc[15]
00000000
0x81090d60: vc[16]     00000000      0x81090d64: vc[17]
00000000
0x81090d68: vc[18]     00000000      0x81090d6c: vc[19]
00000000
0x81090d70: vc[20]     00000000      0x81090d74: vc[21]
00000000
0x81090d78: vc[22]     00000000      0x81090d7c: vc[23]
00000000
0x81090d80: vc[24]     00000000      0x81090d84: vc[25]
00000000
0x81090d88: vc[26]     00000000      0x81090d8c: vc[27]

```

```

00000000
0x81090d90: vc[28]      00000000      0x81090d94: vc[29]
00000000
0x81090d98: vc[30]      00000000      0x81090d9c: vc[31]
00000000
0x81090da0: vc[32]      00000000      0x81090da4: vc[33]
00000000
0x81090da8: vc[34]      00000000      0x81090dac: vc[35]
00000000
0x81090db0: vc[36]      00000000      0x81090db4: vc[37]
00000000
0x81090db8: vc[38]      00000000      0x81090dbc: vc[39]
00000000

```

Logical STS registers

=====

```

0x81585044: sts_ftb_type1_miss      00000000
0x81585048: sts_ftb_type2_miss      00000000
0x8158504c: sts_ftb_type6_miss      00000000
0x81585050: sts_hard_zoning_miss    00000000
0x81585054: sts_lun_zoning_miss     00000000
0x8158505c: sts_unroutable          00000000
0x81582074: sts_rte_cl2             00000000      0x81582078:
sts_rte_cl3             00000000      0x8158207c: sts_rte_link_ctl
00000000      0x81585068: sts_tx_timeout          00000000

```

Logical STS filter registers

=====

```

0x81584fc0: stsflt_trig [00] 00000000 00000000 00000000
00000000
0x81584fd0: stsflt_trig [04] 00000000 00000000 00000000
00000000
0x81584fe0: stsflt_trig [08] 00000000 00000000 00000000
00000000
0x81584ff0: stsflt_trig [12] 00000000 00000000 00000000
00000000
0x81585000: stsflt_trig [16] 00000000 00000000 00000000
00000000
0x81585010: stsflt_trig [20] 00000000 00000000 00000000
00000000
0x81585020: stsflt_trig [24] 00000000 00000000 00000000
00000000
0x81585030: stsflt_trig [28] 00000000 00000000 00000000
00000000
0x81585040: stsflt_trig [32]

```

Logical STS discard registers

=====

```

0x81582e84: disc_mcast_wka          00000000      0x81582e88:
disc_inv_did            00000000
0x81582e8c: disc_cl1_cl4           00000000      0x81582e90:
disc_sid_chk_fail       00000000
0x81582e94: disc_inv_dom_egid_txpt 00000000      0x81582e98:

```

```

disc_vft_hop_cnt_1      00000000
0x81582e9c: disc_classf      00000000      0x81582ea0:
disc_fcp_cdb_inv      00000000
0x81582ea4: disc_vfid_trap_enabled 00000000      0x81582ea8:
disc_vfid_hdr_chk_fail 00000000
0x81582eac: disc_shim_cksum_fail 00000000      0x81582eb0:
disc_fed_edit_cmd_err 00000000
0x81582eb4: disc_ftb_vm_mode      00000000      0x81582eb8:
disc_ftb_agnt2_miss 00000000
0x81582ebc: disc_ecb_reserved      00000000      0x81582ec0:
disc_ecb_de_pad_err 00000000
0x81582ec4: disc_ecb_de_tag_err      00000000      0x81582ec8:
disc_ecb_de_seq_err 00000000
0x81582ecc: disc_ecb_err      00000000      0x81582ed0:
disc_ftb_type4_match 00000000
0x81582ed4: disc_fcp_rsp_ftb_type4 00000000      0x81582ed8:
disc_ftb_type5_match 00000000
0x81582edc: disc_ftb_type3_match 00000000      0x81582ee0:
disc_els_ftb_type3 00000000
0x81582ee4: disc_ftb_type1_match 00000000      0x81582ee8:
disc_els_rsp_ex_port 00000000
0x81582eec: disc_inv_drp_dps      00000000      0x81582ef0:
disc_did_lookup_miss 00000000
0x81582ef4: disc_ftb_type2_match      00000000      0x81582ef8:
disc_trpd_plogi_pdisc 00000000
0x81582efc: disc_type2_lookup_miss 00000000      0x81582f00:
disc_ftb_type6_match 00000000
0x81582f04: disc_els_rep_ex_port      00000000      0x81582f08:
disc_els_sid_lkup_bit1 00000000
0x81582f0c: disc_els_sid_lkup_bit0 00000000      0x81582f10:
disc_bls_frm_trap_bit1 00000000
0x81582f14: disc_ftb_token_err      00000000      0x81582f18:
disc_asic_internal_err 00000000
0x81582f1c: disc_hard_zone_miss      00000000      0x81582f20:
disc_lun_zone_miss 00000000
0x81582f24: discflt_frame_disc      00000000      0x81582f28:
discflt_parity_err 00000000
0x81582f2c: disc_frame_marked_du      00000000      0x81582f30:
disc_frame_marked_to 00000000
0x81582f34: disc_lkup_rte_prty_err 00000000

```

portstatsshow 41

```

stat_wtx      0      4-byte words transmitted
stat_wrx      0      4-byte words received
stat_ftx      0      Frames transmitted
stat_frx      0      Frames received
stat_c2_frx   0      Class 2 frames received
stat_c3_frx   0      Class 3 frames received
stat_lc_rx    0      Link control frames
received
stat_mc_rx    0      Multicast frames
received
stat_mc_to    0      Multicast timeouts

```

| | | | | |
|------------------------------|------------|-----|-----|-------------------------|
| stat_mc_tx | 0 | | | Multicast frames |
| transmitted | | | | |
| tim_txcrd_z | 0 | | | Time TX Credit Zero |
| (2.5Us ticks) | | | | |
| tim_txcrd_z_vc 0- 3: | 0 | 0 | 0 | 0 |
| tim_txcrd_z_vc 4- 7: | 0 | 0 | 0 | 0 |
| tim_txcrd_z_vc 8-11: | 0 | 0 | 0 | 0 |
| tim_txcrd_z_vc 12-15: | 0 | 0 | 0 | 0 |
| lat_tot_pkt_vc 0- 3: | 1 | 1 | 1 | 1 |
| lat_tot_pkt_vc 4- 7: | 1 | 1 | 1 | 1 |
| lat_tot_pkt_vc 8-11: | 1 | 1 | 1 | 1 |
| lat_tot_pkt_vc 12-15: | 1 | 1 | 1 | 1 |
| lat_hi_time_vc 0- 3: | 0 | 0 | 0 | 0 |
| lat_hi_time_vc 4- 7: | 0 | 0 | 0 | 0 |
| lat_hi_time_vc 8-11: | 0 | 0 | 0 | 0 |
| lat_hi_time_vc 12-15: | 0 | 0 | 0 | 0 |
| lat_lo_time_vc 0- 3: | 1 | 1 | 1 | 1 |
| lat_lo_time_vc 4- 7: | 1 | 1 | 1 | 1 |
| lat_lo_time_vc 8-11: | 1 | 1 | 1 | 1 |
| lat_lo_time_vc 12-15: | 1 | 1 | 1 | 1 |
| max_latency_vc 0- 3: | 1 | 1 | 1 | 1 |
| max_latency_vc 4- 7: | 1 | 1 | 1 | 1 |
| max_latency_vc 8-11: | 1 | 1 | 1 | 1 |
| max_latency_vc 12-15: | 1 | 1 | 1 | 1 |
| latency_dma_ts | 09-09-2024 | UTC | Mon | 08:47:24 TXQ |
| Latency DMA TimeStamp | | | | |
| fec_cor_detected | 0 | | | Count of blocks that |
| were corrected by FEC | | | | |
| fec_uncor_detected | 0 | | | Count of blocks that |
| were left uncorrected by FEC | | | | |
| er_enc_in | 0 | | | Encoding errors inside |
| of frames | | | | |
| er_crc | 0 | | | Frames with CRC errors |
| er_trunc | 0 | | | Frames shorter than |
| minimum | | | | |
| er_toolong | 0 | | | Frames longer than |
| maximum | | | | |
| er_bad_eof | 0 | | | Frames with bad end-of- |
| frame | | | | |
| er_enc_out | 0 | | | Encoding error outside |
| of frames | | | | |
| er_bad_os | 0 | | | Invalid ordered set |
| er_pcs_blk | 0 | | | PCS block errors |
| er_rx_c3_timeout | 0 | | | Class 3 receive frames |
| discarded due to timeout | | | | |
| er_tx_c3_timeout | 0 | | | Class 3 transmit frames |
| discarded due to timeout | | | | |
| er_unroutable | 0 | | | Frames that are |
| unroutable | | | | |
| er_unreachable | 0 | | | Frame with unreachable |
| destination | | | | |
| er_other_discard | 0 | | | Other discards |
| er_type1_miss | 0 | | | frames with FTB type 1 |
| miss | | | | |

| | | |
|-----------------------|-----------------------------|--------------------------|
| er_type2_miss | 0 | frames with FTB type 2 |
| miss | | |
| er_type6_miss | 0 | frames with FTB type 6 |
| miss | | |
| er_zone_miss | 0 | frames with hard zoning |
| miss | | |
| er_lun_zone_miss | 0 | frames with LUN zoning |
| miss | | |
| er_crc_good_eof | 0 | Crc error with good eof |
| er_inv_arb | 0 | Invalid ARB |
| er_single_credit_loss | 0 | Single vcrdy/frame loss |
| on link | | |
| er_multi_credit_loss | 0 | Multiple vcrdy/frame |
| loss on link | | |
| other_credit_loss | 0 | Link timeout/complete |
| credit loss | | |
| phy_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | Timestamp of |
| phy_port stats clear | | |
| lgc_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | Timestamp of |
| lgc_port stats clear | | |
| fec_corrected_rate | 0 | FEC Corrected blocks per |
| second | | |

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| | | |
|---------------|---|--|
| stat64_wtx | 0 | top_int : 4-byte words transmitted |
| | 0 | bottom_int : 4-byte words transmitted |
| stat64_wrx | 0 | top_int : 4-byte words received |
| | 0 | bottom_int : 4-byte words received |
| stat64_ftx | 0 | top_int : Frames transmitted |
| | 0 | bottom_int : Frames transmitted |
| stat64_frx | 0 | top_int : Frames received |
| | 0 | bottom_int : Frames received |
| stat64_c2_frx | 0 | top_int : Class 2 frames received |
| | 0 | bottom_int : Class 2 frames received |
| stat64_c3_frx | 0 | top_int : Class 3 frames received |
| | 0 | bottom_int : Class 3 frames received |
| stat64_lc_rx | 0 | top_int : Link control frames received |
| | 0 | bottom_int : Link control frames |
| received | | |
| stat64_mc_rx | 0 | top_int : Multicast frames received |
| | 0 | bottom_int : Multicast frames received |
| stat64_mc_to | 0 | top_int : Multicast timeouts |
| | 0 | bottom_int : Multicast timeouts |
| stat64_mc_tx | 0 | top_int : Multicast frames transmitted |
| | 0 | bottom_int : Multicast frames |
| transmitted | | |
| tim64_rdy_pri | 0 | top_int : Time R_RDY high priority |
| | 0 | bottom_int : Time R_RDY high priority |
| tim64_txcrd_z | 0 | top_int : Time BB_credit zero |
| | 0 | bottom_int : Time BB_credit zero |
| er64_enc_in | 0 | top_int : Encoding errors inside of |
| frames | | |
| | 0 | bottom_int : Encoding errors inside of |
| frames | | |

| | | |
|---|---|--|
| er64_crc | 0 | top_int : Frames with CRC errors |
| | 0 | bottom_int : Frames with CRC errors |
| er64_trunc | 0 | top_int : Frames shorter than minimum |
| | 0 | bottom_int : Frames shorter than minimum |
| er64_toolong | 0 | top_int : Frames longer than maximum |
| | 0 | bottom_int : Frames longer than maximum |
| er64_bad_eof | 0 | top_int : Frames with bad end-of-frame |
| | 0 | bottom_int : Frames with bad end-of- |
| frame | | |
| er64_enc_out | 0 | top_int : Encoding error outside of |
| frames | 0 | bottom_int : Encoding error outside of |
| frames | | |
| er64_disc_c3 | 0 | top_int : Class 3 frames discarded |
| | 0 | bottom_int : Class 3 frames discarded |
| er64_pcs_blk | 0 | top_int : PCS block errors |
| | 0 | bottom_int : PCS block errors |
| stat64_rateTxFrame | 0 | Tx frame rate (fr/sec) |
| stat64_rateRxFrame | 0 | Rx frame rate (fr/sec) |
| stat64_rateTxPeakFrame | 0 | Tx peak frame rate (fr/sec) |
| stat64_rateRxPeakFrame | 0 | Rx peak frame rate (fr/sec) |
| stat64_rateTxWord | 0 | Tx Word rate (words/sec) |
| stat64_rateRxWord | 0 | Rx Word rate (words/sec) |
| stat64_rateTxPeakWord | 0 | Tx peak Word rate (words/sec) |
| stat64_rateRxPeakWord | 0 | Rx peak Word rate (words/sec) |
| stat64_PRJTFrames | 0 | top_int : Number of PRJT frames |
| returned to this port | 0 | bottom_int : Number of PRJT |
| frames returned to this port | | |
| stat64_PBSYFrames | 0 | top_int : Number of PBSY frames |
| returned to this port | 0 | bottom_int : Number of PBSY |
| frames returned to this port | | |
| stat64_inputBuffersFull | 0 | top_int : Number of occurrences |
| when all input buffers full | 0 | bottom_int : Number of |
| occurrences when all input buffers full | | |
| stat64_rxClass1Frames | 0 | top_int : Number of class 1 |
| frames received | 0 | bottom_int : Number of class 1 |
| frames received | | |
| stat64_aveTxFrameSize | 0 | Average Tx Frame size |
| stat64_aveRxFrameSize | 0 | Average Rx Frame size |
| Lr_in | 0 | top_int |
| | 0 | bottom_int |
| Ols_in | 0 | top_int |
| | 0 | bottom_int |
| Lr_out | 0 | top_int |
| | 0 | bottom_int |
| Ols_out | 0 | top_int |
| | 0 | bottom_int |
| Link_failure | 0 | top_int |
| | 0 | bottom_int |
| Invalid_CRC | 0 | top_int |

```

Invalid_word      0          bottom_int
                  0          top_int
                  0          bottom_int
Protocol_err      0          top_int
                  0          bottom_int
Loss_of_sig       0          top_int
                  0          bottom_int
Loss_of_sync      0          top_int
                  0          bottom_int
er_bad_os         0          top_int : Invalid ordered set
                  0          bottom_int: Invalid ordered set

```

```

portrouteshow 41
port address ID: 0x012900
external unicast routing table:
  0: Embedded
 255: Embedded
internal unicast routing table:
  0: Embedded

```

```

portcamshow 41
-----
Port  SID used  DID used  SID entries  DID entries
41    0        0        000000     000000
-----

```

```

ptbufshow, ptcreditshow, ptdatashow, ptstatsshow 41
S:
S:VF Enable:          1
S:
S:C4 Global Variable:
S:-----
-----
S:trace_stop:        0
S:
S:C4 Phy Data Pointers: c4_phyp = 0xb6ae0000
S:-----
-----
S:tnodep              0xbb843540      pt
   0x43028015
S:proto_phyp          0xb880a120      phy_cfg
0xb6ae1040
S:c4_chp              0x97e28000      c4_lgcp
0x97f9c000
S:c4_phy_regp         0x81ca8000      proc_dir
0xb851b140
S:-----
-----
S:magic_id            0xc4345678      num_port_timer    12
S:prev_if_id         0x43020015      S:ftx              0
   tov              0
S:initialized         1                port_idx           21
S:ui_idx              41                slot_no

```


| | | | | |
|----------------------------|------------|------------|-----------------------|-----|
| 0 | | | | |
| S:blade_idx | 21 | | sw_usr_ports | 400 |
| S:unused | | 0 | intr_debounced | |
| 0 | | | | |
| S:aec_status | 0x0 | | reason_code | |
| 0 | | | | |
| S:debug | 0x00000004 | | debug_trc_line | 0 |
| S:rxbuf_list_head | 0xffffffff | | rxbuf_list_tail | |
| 0xffffffff | | | | |
| S:isAePort | | 0 | port_misc_data | |
| 0 | | | | |
| S:num_fault1_rx_disc | 0 | | num_fault2_rx_disc | 0 |
| S:p_lli_cause0 | 0 | | p_sig_regained | 0 |
| S:p_sync_regained | | 0 | enc_out | |
| 0x0 | | | | |
| S:cached_fps_status | 0 | | cached_sts_status | 0 |
| S:cached_er_crc_good_eof | | 0 | | |
| S:cached_er_bad_os | 0 | | cached_er_too_long | 0 |
| S:cached_er_trunc | 0 | | | |
| cached_tot_er_crc_good_eof | | 0 | | |
| S:num_pt_excess_intr | 0 | | num_no_fid | 0 |
| S:num_fault1_cnt | | 0 | num_fault2_cnt | |
| 0 | | | | |
| S:num_fault_lip | 0 | | num_fault_lli | 0 |
| S:num_fault_rx_fifo | 0 | | num_fault_hss | 0 |
| S:num_fault_bwait | | 0 | lli_intr_prim | |
| 0 | | | | |
| S:num_sw_link_to | | 0 | | |
| be_link_err_mon_count | | 0 | | |
| S:ecb_enc_enabled | | 0 | ecb_comp_enabled | |
| 0 | | | | |
| S:ecb_rsv_enc | 0 | | ecb_rsv_comp | 0 |
| S:ecb_enc_bm | 0x0 | | ecb_key_index | |
| 0xffffffff | | | | |
| S:fab_idx | 0 | | | |
| S:num_be_lto | 0 | | lto_count_reset_intvl | |
| 0 | | | | |
| S:lr_count_reset_intvl | | 0 | num_be_lr | |
| 0 | | | | |
| S:num_fault_qsfp | | 0 | check_lto | |
| 0 | | | | |
| S:credit_loaded | 0 | | num_credit_overrun | |
| 0 | | | | |
| S:fec_enabled | 0x0 | | fec_los_to_flag | 0x0 |
| S:phy_stats_clear_ts | | 1725611419 | pcs_err_online | |
| 0 | | | | |
| S:pcs_err_light_det | | 0 | pcs_err_ignore | |
| 0 | | | | |
| S:pcs_blk_err | 0 | | pcs_hiber | 0 |
| S:phy_port_status | | 0 | ecb_enc_lr_count | |
| 0 | | | | |
| S:dport_mode | 0 | | avoid_lto_det | 0 |
| S:sn_debounced | 0x0 | | sn_started_kr_reqd | 0 |
| S:major_timer_started | 0x0 | | ready_bm | 0x0 |

```

S:parln_1_bm          0x0          parln_0_bm          0x0
S:be_los_of_sync_event_intvl          0
be_los_of_sync_event          0
S:errataPtenable_cntr          0          errataPoll_cntr
0
S:jda_rx_sig_loss_det          0          jda_rx_sig_loss_cnt
0
S:encrypt_blk_error          0
S:
S:      c4_trunk
S:=====
S:mark_ts          0x0          deskew          0x0
S:master_phyp          0x0
S:
S:adelay[00]: 0x00000000 0x00000000 0x00000000 0x00000000
S:adelay[04]: 0x00000000 0x00000000 0x00000000 0x00000000
S:
S:      c4_buf
S:=====
S:tx_csc          0          rx_csc
0
S:ld_vc_credits          0          tx_flag          0x0
S:alloc_buffers          0          req_buffers          0
S:est_buffers          20          ld_use_est          0
S:bb_sc_n          0          rx_bb_sc_n
0
S:data_cr          5          nondata_cr
6
S:cr_enable          0
S:ld_nondata_cr          6          tnodep
0xbb843620
S:tx_credits[0] 0 0 0 0 0 0 0 0
S:tx_credits[8] 0 0 0 0 0 0 0 0
S:tx_credits[16] 0 0 0 0 0 0 0 0 0 0
S:tx_credits[24] 0 0 0 0 0 0 0 0 0 0
S:tx_credits[32] 0 0 0 0 0 0 0 0 0 0
S:rx_credits[0] 0 0 0 0 0 0 0 0
S:rx_credits[8] 0 0 0 0 0 0 0 0
S:rx_credits[16] 0 0 0 0 0 0 0 0 0 0
S:rx_credits[24] 0 0 0 0 0 0 0 0 0 0
S:rx_credits[32] 0 0 0 0 0 0 0 0 0 0
S:tx_mbc[0] 0 0 0 0 0 0 0 0
S:tx_mbc[8] 0 0 0 0 0 0 0 0
S:tx_mbc[16] 0 0 0 0 0 0 0 0
S:tx_mbc[24] 0 0 0 0 0 0 0 0
S:tx_mbc[32] 0 0 0 0 0 0 0 0
S:rx_mbc[0] 0 0 0 0 0 0 0 0
S:rx_mbc[8] 0 0 0 0 0 0 0 0
S:rx_mbc[16] 0 0 0 0 0 0 0 0
S:rx_mbc[24] 0 0 0 0 0 0 0 0
S:rx_mbc[32] 0 0 0 0 0 0 0 0
S:
S:C4 Chip Variables: c4_phyp->c4_chp = 0x97e28000
S:-----

```

```

-----
S:version = 2.1
S:magic_id          0xc4234567      init_state          0x8
S:reset_reg_mem    0x1
S:ch_int0_en_bm    0x0          intr0_cause         0x0
S:ch_int1_en_bm    0x0          intr1_cause         0x0
S:ch_int2_en_bm    0x0          intr2_cause         0x0
S:ch                0x43010080      ch_cfg
0xb7013ba0
S:raslog_hndl.hndl 0x0          obj_halted          0x0
S:c4_chip_regp     0x80000000      c4_fpg_regp
0x81800000
S:num_chip_timer   0x5
S:hi_task_bm       0x0          lo_task_bm          0x0
S:c4_deferq.q_head 0x0          c4_deferq.q_tail   0x0
S:c4_tmrq.q_head   0x0          c4_tmrq.q_tail     0x0
slot_no            0
S:chip_inst        0          chip_idx             0
S:pll_initialized          1
pll_serdes_initialized 1
S:init_tries        0          init_ptEnableBM
0xba01b488
S:tick_polling     0xb980c9c0      sec_polling
0xb980c960
S:bb_fid            129
S:ecb_key_bm[0]    0x0          ecb_key_bm[1]       0x0
S:ecb_key_bm[2]    0x0          ecb_key_bm[3]       0x0
S:is_chip_enc_enabled
is_chip_comp_enabled 0x0
S:ftb_rsrcp->ftb_flags 0x0          act_rsrcp->act_flag 0x1
S:lue_rsrcp->lue_flags[0] 0x0          lue_rsrcp->
>lue_flags[1] 0x0
S:c4_phyp[00]: 0xb6ab0000 0xb6ab2080 0xb6ab4100 0xb6ab6180
S:c4_phyp[04]: 0xb6ab9040 0xb6abb0c0 0xb6abd140 0xb6ac0000
S:c4_phyp[08]: 0xb6ac2080 0xb6ac4100 0xb6ac6180 0xb6ac9040
S:c4_phyp[12]: 0xb6acb0c0 0xb6acd140 0xb6ad0000 0xb6ad2080
S:c4_phyp[16]: 0xb6ad4100 0xb6ad6180 0xb6ad9040 0xb6adb0c0
S:c4_phyp[20]: 0xb6add140 0xb6ae0000 0xb6ae2080 0xb6ae4100
S:c4_phyp[24]: 0xb6ae6180 0xb6ae9040 0xb6aeb0c0 0xb6aed140
S:c4_phyp[28]: 0xb6af0000 0xb6af2080 0xb6af4100 0xb6af6180
S:c4_phyp[32]: 0xb6af9040 0xb6afb0c0 0xb6afd140 0xb6b00000
S:c4_phyp[36]: 0xb6b02080 0xb6b04100 0xb6b06180 0xb6b09040
S:c4_phyp[40]: 0xb6b0b0c0 0xb6b0d140 0xb6b10000 0xb6b12080
S:c4_phyp[44]: 0xb6b14100 0xb6b16180 0xb6b19040 0xb6b1b0c0
S:c4_phyp[48]: 0xb6b1d140 0xb6b20000 0xb6b22080 0xb6b24100
S:c4_phyp[52]: 0xb6b26180 0xb6b29040 0xb6b2b0c0 0xb6b2d140
S:c4_phyp[56]: 0xb6b30000 0xb6b32080 0xb6b34100 0xb6b36180
S:c4_phyp[60]: 0xb6b39040 0xb6b3b0c0 0xb6b3d140 0xb6b40000
S:c4_lgcp[00]: 0x97f48000 0x97f4c000 0x97f50000 0x97f54000
S:c4_lgcp[04]: 0x97f58000 0x97f5c000 0x97f60000 0x97f64000
S:c4_lgcp[08]: 0x97f68000 0x97f6c000 0x97f70000 0x97f74000
S:c4_lgcp[12]: 0x97f78000 0x97f7c000 0x97f80000 0x97f84000
S:c4_lgcp[16]: 0x97f88000 0x97f8c000 0x97f90000 0x97f94000
S:c4_lgcp[20]: 0x97f98000 0x97f9c000 0x97fa0000 0x97fa4000

```

```

S:c4_lgcp[24]: 0x97fa8000 0x97fac000 0x97fb0000 0x97fb4000
S:c4_lgcp[28]: 0x97fb8000 0x97fbc000 0x97fc0000 0x97fc4000
S:c4_lgcp[32]: 0x97fc8000 0x97fcc000 0x97fd0000 0x97fd4000
S:c4_lgcp[36]: 0x97fd8000 0x97fdc000 0x97fe0000 0x97fe4000
S:c4_lgcp[40]: 0x97fe8000 0x97fec000 0x97ff0000 0x97ff4000
S:c4_lgcp[44]: 0x97ff8000 0x97ffc000 0x8e000000 0x8e004000
S:c4_lgcp[48]: 0x8e008000 0x8e00c000 0x8e010000 0x8e014000
S:c4_lgcp[52]: 0x8e018000 0x8e01c000 0x8e020000 0x8e024000
S:c4_lgcp[56]: 0x8e028000 0x8e02c000 0x8e030000 0x8e034000
S:c4_lgcp[60]: 0x8e038000 0x8e03c000 0x8e040000 0x8e044000
S:chip_timers[00]: 0xb980c720 0xb980c780 0xb980c7e0 0xb980c840
S:chip_timers[04]: 0xb980c8a0 0xb980c900
S:disc_trap_enable_required      0x0          rxlp_disc_log_stop
      0x0
S:curr_rxlp_frm_cnt      0x0          curr_rxlp_disc_frm_cnt  0x0
S:sw_disc_frm_cnt      0x0          last_disc_frm_cnt      0x0
S:txq_nopop_pr_cnt      0x0          pollErrataDfe_ptBM
0xba01b4b0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][0]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][1] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][2]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][0] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][1]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][2] 0x0
S:
S:C4 Logical Port Variables
S:-----
-----
S:c4_lgc_regp      0x81ca8000
S:c4_phyp:
S:      0xb6ae0000      0x0          0x0          0x0

S:      0x0          0x0          0x0          0x0

S:master_phyp      0xb6ae0000      if_id
0x43020015
S:min_phyp      0x0          max_phyp      0x0
S:num_phy_ports      1          lgc_num      21
S:num_iu_to      0          sw_txq_bm
0
S:port_fid      128          unused      0
S:port_group      2          lgc_stats_clear_ts
1725611419
S:domain_tbl_sel      0          area_tbl_sel
0
S:egid_tbl_sel      0
S:serv_lo_bm      0x0
S:
S:Proto Phy Variables:
S:-----
-----
S:magic_id      0xc4123456      asic_phyp
0xb6ae0000
S:port_id      0x43028015      phy_cfg

```

```

        0xb6ae1040
S:upsm_hdl          0xb80166e0      physm_hdl
0xb8016460
S:ov_snsn_hdl      0xb8016320      sw_snsn_hdl
0xb80163c0
S:ov_lksm_hdl      0xb8016500      sw_lksm_hdl
0xb80165a0
S:trksm_hdl        0xb8016640      lr_flag          0x0
S:lr_active        0x0          qsfp_tsr_x_rate_sel
        0x0
S:
S:UPSM          UP00: UPST_PORT_DISABLED      --> UP01:
UPST_START_PORT_INIT
S:SNSM(OV)      SN00: OV_SNST_STOPPED      --> SN00: OV_SNST_STOPPED
S:SNSM(SW)      SW00: SW_SNST_STAGE_WS      --> SW00: SW_SNST_STAGE_WS
S:PHYSM          UNKNOWN      --> PP03: PHYST_NO_SIGNAL
S:LKSM(OV)      LK00: OV_LKST_INACTIVE      --> LK00: OV_LKST_INACTIVE
S:LKSM(SW)      SW13: INACTIVE      --> SW13: INACTIVE
S:TRKSM          TRK0: TRKST_INIT      --> TRK0: TRKST_INIT
S:
S:physm variables:
S:-----
-----
S:proto_phyp      0xb880a120      physm_hdl
0xb8016460
S:force_offline   0          copper          0
S:fault_reason    0: UNKNOWN
S:phy_media_present      1
S:
S:snsn variables:
S:-----
-----
S:speed          0xff          proto_phyp
0xb880a120
S:hw_sn_tries_left      0x0          sw_sn_tries_left      0x0
S:curr_txsp_count      0x0
S:tx_max          0x0          curr_tx_indx
        0x0
S:curr_tx          0x0          curr_rxsp_count
        0x0
S:rx_max          0x0          curr_rx_indx
        0x0
S:curr_rx          0x0          rx_mem
        0x0
S:rxsp_rec_count      0x0
S:nc_start        0x0          tx_start          0x0
S:sync_start      0x0          sync_present      0x0
S:diag_auto       0x0          diag_speed        0xff
S:striped_wd_tov   3000          hw_wd_tov
        3000
S:step            0x0          qsfp28_speed_mode
        0x0
S:qsfp_mode0_hw_sn_tries_left      0x0
S:qsfp_mode1_hw_sn_tries_left      0x0

```

```

S:
S:lksm variables:
S:-----
-----
S:proto_phyph          0xb880a120      ov_lksm_hdl
0xb8016500
sw_lksm_hdl           0xb80165a0
num_lf1               0
S:hw_link_tries_left  0              sw_link_tries_left  0
S:buf_ptype           0x0            stored_entry_state   0x6
S:handshake_owner     0x0            mark_unsent
0x0
S:busybuf_stuck       0x0            lr_wait              0x0
S:
S:trksm variables:
S:-----
-----
S:Not a trunk port
S:
S:upsm variables:
S:-----
-----
S:proto_phyph          0xb880a120      upsm_hdl
0xb80166e0
S:bb_credits          0              port_beacon          0
S:port_diag_flag      0              force_offline
0
S:port_fault_rsn      0: PORT_NO_FAULT
S:retry_init_rsn      0: UNKNOWN
S:limit_reason        0              linit_result         0
S:ie_fctl_mode        0              fec_in_sync_tries_left 0
S:retry_sn_fail_init  0
retry_link_fail_init  0
S:excess_lr_count     0
S:
S:c4_ch_cfg
S:-----
-----
S:c4_desc_ring_size   256           292           256           256           292
292           2           292           292
S:thresh_def          0              16             1              0
S:intr_tries          500           cmem_pattern
0xdeadbeef
S:cmem_pattern_upwd   2              cmem_init_time      16
S:cmem_init_tries     5
S:ctrl_par_thresh    2              data_par_thresh
4
S:cam_par_thresh      4              buf_loss_thresh
12
S:crit_par_thresh     2              non_crit_par_thresh
6
S:pci_abort_thresh    10            pci_err_thresh       5
S:excess_chintr_thresh 8              sw_err_thresh        20
S:err_sample_period   300           intr_sleep

```

```

20000
S:frame_timeout 2500 proxy_dev 16384
S:vf_route 81920 qos 2048
S:stats 2048 f_redirect 2048
S:rsp_trap 2048 lun_zoning 20480
S:area_mode 0 ftb_max_loop[0] 0
S:ftb_max_loop[1] 6 ftb_max_loop[2] 9
S:ftb_max_loop[3] 10 ftb_max_loop[4] 10
S:ftb_max_loop[5] 5 ftb_max_loop[6] 6
S:ftb_seg_size[0] 0 ftb_seg_size[1]
16384
S:ftb_seg_size[2] 65536 ftb_seg_size[3]
16384
S:ftb_seg_size[4] 16384 ftb_seg_size[5]
65536
S:ftb_seg_size[6] 16384 ftb_seg_base[0] 0
S:ftb_seg_base[1] 0 ftb_seg_base[2]
65536
S:ftb_seg_base[3] 16384 ftb_seg_base[4]
32768
S:ftb_seg_base[5] 131072 ftb_seg_base[6]
49152
asic_err_monitor_period1 300
asic_err_monitor_period2 86400
zone_chk_to_poll_period 25
zone_chk_class2_reject_tov
S:
S:c4_phy_cfg
S:-----
-----
S:version = 2.1
S:pt 0x43028015 fab_ptr
0x9a800000
S:fabattr 0x9a8000d4 fab_iop
0x9a800050
S:cfgbm 0xbb843384 port_ctrl
0xb6ae1058
S:pcap.pcap_bm 0x8d215547 pcap.pcap2_bm
0x588289
S:pcap.pcap3_bm 0x1bebe0c
ui_idx 41 S:slot_no
0
is_icl 0 S:sw_usr_ports 400
S:neg_speed 0 0 0 0 0 0
S:my_domain 0x1 port_mode 0x0
S:hw_sn_maxtries 100 sw_sn_maxtries
0
S:hw_link_maxtries 10 sw_link_maxtries 5
S:rx_cyc_tov 28 rttov 300
S:bufrdy_tov 300 busybuf_tov 286
S:mark_tov 300 lksm_tov 3000
S:buf_dealloc_wait 4 hw_wd_tov 3000
S:hw_lk_train_tov 540 hw_lk_test_tov
150

```

```

S:syswait_tx_12_lips      1          lip_rx_tov          55
S:al_time_tov            15          lp_tov              2000
S:intr_tries_port        500          intr_mod_debounce
    250
S:intr_lsrflt_debounce   500          intr_efifo_debounce 100
S:port_no_fid            3          excess_ptintr_thresh 8
S:port_fault1_thresh     100         port_fault1_spur_thresh 250
S:port_fault1_disc_thresh 500
port_fault1_disc_spur_thresh 1000
S:port_fault2_thresh     5          losync_tov          100
S:port_sw_link_to        15          en_8g_scramble
    1
frc_hw_sn_mode           0x1
S:enc_poll_thresh        0          fec_enable
    0
S:fec_in_sync_to         50          fec_in_sync_try_max
    4
S:port_be_lto_threshold  100         port_be_lr_threshold
    2
S:be_cr_in_sync_to       5
port_credit_overrun_thresh 10
S:jda_sfp_losig_tov      400
jda_sfp_losig_try_max    30
S:striped_wd_tov         3000
no_sync_debounce         1200
S:
S:      fab_iop
S:=====
S:fab_iop->interop_mode  0x0          fab_iop->lab_mode    0x0
S:fab_iop->fl_bbc         0x0          fab_iop->fl_fan
    0x0
S:fab_iop->fl_cls         0x4          fab_iop->fl_rscn
    0x0
S:fab_iop->domain_id_offset 0x60         fab_iop-
>mcdt_fabric_mode        0x0
S:fab_iop->mcdt_default_zone 0x0          fab_iop-
>mcdt_safe_zone          0x0
S:
S:      port_ctrl
S:=====
S:port_ctrl.port_type     1          port_ctrl.port_grp   2
S:port_ctrl.port_number  41          port_ctrl.vc_mode    1
S:
S:      port_ctrl.lcap
S:=====
S:has_serdes              0          has_media            1
S:topology                 1          skip_nego             0
S:skip_pnego               0          skip_init_event      0
S:en_shim                  0          speed_neg
    1
S:loop_back                0          num_speeds           5
S:fec_enable               0
S:
S:      port_ctrl.speed_list array

```



```

S:=====
S:speed_list[0].auto_neg 1 speed_list[0].lnk_speed 0x0000000a
S:speed_list[1].auto_neg 1 speed_list[1].lnk_speed 0x00000008
S:speed_list[2].auto_neg 0 speed_list[2].lnk_speed 0x00000006
S:speed_list[3].auto_neg 1 speed_list[3].lnk_speed 0x00000005
S:speed_list[4].auto_neg 0 speed_list[4].lnk_speed 0x00000003
S:speed_list[5].auto_neg 0 speed_list[5].lnk_speed 0x00000000
S:
S: port_ctrl.cm
S:=====
S:port_ctrl.cm.num_vcs 8
S:port_ctrl.cm.min_bufs 8
S:port_ctrl.cm.cr_shar_bufs 0
S:port_ctrl.vc_alloc
S:port_ctrl.vc_alloc 2 0 1 1 1 1 1 1
S:port_ctrl.vc_alloc 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.norm_vc_alloc
S:port_ctrl.norm_vc_alloc 4 0 5 5 5 5 1 1
S:port_ctrl.norm_vc_alloc 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.cm.skip_bb_credit 0
S:port_ctrl.cm.use_shim_based_sublist 0
S:
S: port_ctrl.serdes_set
S:=====
S:serdes_type 0x8
S:serdes_data_t.ibm_hss_serdes.tx_drive_power 0x1
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b_sign 0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b 0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_a 0x0
S:serdes_data_t.ibm_hss_serdes.rxeq 0x0
S:
S: cfgbm
S:=====
S:old_distance 0x0 gport_lockdown 0x0
S:tport 0x1 speed 0x0
S:disable_eport 0x0 fcacc 0x0
S:lport_lockdown 0x0 priv_lport_lockdown
0x0
S:vcxlt_linit 0x0 delay_flogi 0x0
S:isl_interop 0x0 distance 0x0
S:BufStarvFlag 0x0 credit_sharing 0x0
S:lport_halfduplex 0x0 lport_fairness 0x0
S:soft_neg 0x0 asn_frc_hwretry 0x0
S:cr_recov 0x0 fport_buffers 0x0
S:export 0x0 export_mode
0x0
S:csctl_en 0x0 mirror_port 0x0
S:fault_delay 0x0 non_dfe 0x0
S:fec_configured*(0=ENAB) 0 fec_tts
0
S:port_persistently_disabled (permanently) 0 (0)
S:

```

```

S:      cfg property
S:=====
S:priv_pcfg_bm      0x00000000      lgcl_pcfg_bm
0xbb8433c4
S:fport_buffer      0x00000000
S:
S:
S:C4 Discard Cntrs: rxlp_stats = 0xb6ae03b0
S:-----
-----
S:disc_mcast_wka      0x0          disc_inv_did          0x0
S:disc_cl1_cl4        0x0          disc_sid_chk_fail     0x0
S:disc_inv_dom_egid_txpt      0x0          disc_vft_hop_cnt_1
0x0
S:disc_classf          0x0          disc_fcp_cdb_inv      0x0
S:disc_vfid_trap_enabled      0x0
disc_vfid_hdr_chk_fail 0x0
S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err 0x0
S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err 0x0
S:disc_ftb_vm_mode     0x0          disc_ftb_agnt2_miss   0x0
S:disc_ecb_de_pad_err  0x0          disc_ecb_de_tag_err   0x0
S:disc_ecb_de_seq_err  0x0          disc_ecb_err           0x0
S:disc_ftb_type4_match 0x0          disc_fcp_rsp_ftb_type4 0x0
S:disc_fcp_rsp_ftb_type4      0x0          disc_ftb_type5_match
0x0
S:disc_ftb_type3_match 0x0          disc_els_ftb_type3    0x0
S:disc_ftb_type1_match 0x0          disc_els_rsp_ex_port  0x0
S:disc_inv_drp_dps      0x0          disc_did_lookup_miss  0x0
S:disc_ftb_type2_match 0x0          disc_trpd_plogi_pdisc 0x0
S:disc_type2_lookup_miss      0x0          disc_ftb_type6_match
0x0
S:disc_els_rep_ex_port 0x0          disc_els_sid_lkup_bit1 0x0
S:disc_els_sid_lkup_bit0      0x0
disc_bls_frm_trap_bit1 0x0
S:disc_ftb_token_err    0x0          disc_asic_internal_err 0x0
S:disc_hard_zone_miss   0x0          disc_lun_zone_miss    0x0
S:discflt_frame_disc    0x0          discflt_parity_err    0x0
S:disc_frame_marked_du  0x0          disc_frame_marked_to  0x0
E:Connection type: FE
E:Port type: F_port
E:Trunk port: No
E:Configured Speed: AUTO_SPEED_NEGO
E:Max Capable Speed: 32G
E:Current SNSM Speed: UNDEFINED
E:Hardware TX Speed: 32G (0x00000004)
E:Hardware RX Speed: 32G (0x00000040)
E:
E:Interrupts:      0          Link_failure:          0
Loss_of_sync:      0          Loss_of_sig:           0
E:Lli:              0          Invalid_word:          0
E:trapped_frm:      0          fwd_status_ok:         0
E:fwd_timeout:      0          fwd_tx_unavail:        0
E:fwd_unroutable:   0          fwd_zone_out:          0
E:fwd_other_err:    0          frm_err_discard:       0

```

| | | | |
|------------------|---|-----------------|---|
| E:Fltr listA: | 0 | Fltr listB: | 0 |
| E:Zone trap fwd: | 0 | Zone trap disc: | 0 |
| E:shim_csum: | 0 | RTE_perr: | 0 |
| E:Invalid_crc: | 0 | Delim_err: | 0 |
| E:Protocol_err: | 0 | | |
| E:Lr_in: | 0 | Lr_out: | 0 |
| E:Ols_in: | 0 | Ols_out: | 0 |

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FILTER DATA

Shadow settings:

Filter Enable: 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass: 0x00000000

Real settings:

Enable RAM: 0x00000000, 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000

Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass RAM: 0x00000000

Shadowed filters:

Filter 0: Not Installed (MIRROR1)(LISTA)
c4_fldenable[0] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[0] = 0x00000000,c4_fltr_config[0] = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
c4_fldenable[1] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[1] = 0x00000000,c4_fltr_config[1] = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
c4_fldenable[2] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[2] = 0x00000000,c4_fltr_config[2] = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
c4_fldenable[3] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[3] = 0x00000000,c4_fltr_config[3] = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
c4_fldenable[4] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[4] = 0x00000000,c4_fltr_config[4] = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
c4_fldenable[5] = 0x00000000 0x00000000 0x00000000

```
0x00000000
    c4_fldnegate[5] = 0x00000000,c4_fltr_config[5] = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
    c4_fldenable[6] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[6] = 0x00000000,c4_fltr_config[6] = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
    c4_fldenable[7] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[7] = 0x00000000,c4_fltr_config[7] = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
    c4_fldenable[8] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[8] = 0x00000000,c4_fltr_config[8] = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
    c4_fldenable[9] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[9] = 0x00000000,c4_fltr_config[9] = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
    c4_fldenable[10] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[10] = 0x00000000,c4_fltr_config[10] =
0x00000000
Filter 11: Not Installed (SIM)(LISTA)
    c4_fldenable[11] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[11] = 0x00000000,c4_fltr_config[11] =
0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
    c4_fldenable[12] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[12] = 0x00000000,c4_fltr_config[12] =
0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
    c4_fldenable[13] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[13] = 0x00000000,c4_fltr_config[13] =
0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
    c4_fldenable[14] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[14] = 0x00000000,c4_fltr_config[14] =
0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
    c4_fldenable[15] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[15] = 0x00000000,c4_fltr_config[15] =
0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
    c4_fldenable[16] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[16] = 0x00000000,c4_fltr_config[16] =
0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
```

```
    c4_fldenable[17] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[17] = 0x00000000,c4_fltr_config[17] =
0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
    c4_fldenable[18] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[18] = 0x00000000,c4_fltr_config[18] =
0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
    c4_fldenable[19] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[19] = 0x00000000,c4_fltr_config[19] =
0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
    c4_fldenable[20] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[20] = 0x00000000,c4_fltr_config[20] =
0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
    c4_fldenable[21] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[21] = 0x00000000,c4_fltr_config[21] =
0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
    c4_fldenable[22] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[22] = 0x00000000,c4_fltr_config[22] =
0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
    c4_fldenable[23] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[23] = 0x00000000,c4_fltr_config[23] =
0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
    c4_fldenable[24] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[24] = 0x00000000,c4_fltr_config[24] =
0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
    c4_fldenable[25] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[25] = 0x00000000,c4_fltr_config[25] =
0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
    c4_fldenable[26] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[26] = 0x00000000,c4_fltr_config[26] =
0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
    c4_fldenable[27] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[27] = 0x00000000,c4_fltr_config[27] =
0x00000000
```

Filter 28: Not Installed (OPM1)(LISTA)
c4_fldenable[28] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[28] = 0x00000000,c4_fltr_config[28] =
0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
c4_fldenable[29] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[29] = 0x00000000,c4_fltr_config[29] =
0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
c4_fldenable[30] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[30] = 0x00000000,c4_fltr_config[30] =
0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
c4_fldenable[31] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[31] = 0x00000000,c4_fltr_config[31] =
0x00000000

Real filters:

Filter 0: Not Installed (MIRROR1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,

0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 11: Not Installed (SIM)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 21: Not Installed (PERF6)(LISTA)
 fld enable ram = 0x00000000, 0x00000000, 0x00000000,
 0x00000000,
 fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 22: Not Installed (PERF7)(LISTA)
 fld enable ram = 0x00000000, 0x00000000, 0x00000000,
 0x00000000,
 fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 23: Not Installed (PERF8)(LISTA)
 fld enable ram = 0x00000000, 0x00000000, 0x00000000,
 0x00000000,
 fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 24: Not Installed (PERF9)(LISTA)
 fld enable ram = 0x00000000, 0x00000000, 0x00000000,
 0x00000000,
 fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 25: Not Installed (PERF10)(LISTA)
 fld enable ram = 0x00000000, 0x00000000, 0x00000000,
 0x00000000,
 fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 26: Not Installed (PERF11)(LISTA)
 fld enable ram = 0x00000000, 0x00000000, 0x00000000,
 0x00000000,
 fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 27: Not Installed (PERF12)(LISTA)
 fld enable ram = 0x00000000, 0x00000000, 0x00000000,
 0x00000000,
 fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 28: Not Installed (OPM1)(LISTA)
 fld enable ram = 0x00000000, 0x00000000, 0x00000000,
 0x00000000,
 fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 29: Not Installed (OPM2)(LISTA)
 fld enable ram = 0x00000000, 0x00000000, 0x00000000,
 0x00000000,
 fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 30: Not Installed (IPM1)(LISTA)
 fld enable ram = 0x00000000, 0x00000000, 0x00000000,
 0x00000000,
 fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 31: Not Installed (IPM2)(LISTA)
 fld enable ram = 0x00000000, 0x00000000, 0x00000000,
 0x00000000,
 fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter dirty indicator: 0x00000000
 Performance filters: 0
 Port Mirror filters: 0 (0x0)

FIELD DATA

Shadowed fields:

```
fldoffset[0] = 0x00, fldmask[0] = 0x00, fldvalue_dyna[0]:0x00 0x00
0x00 0x00
fldcontrol[0].inuse = 0x0 fldcontrol[0].refcnt = 0x00 0x00 0x00
0x00
fldoffset[1] = 0x00, fldmask[1] = 0x00, fldvalue_dyna[1]:0x00 0x00
0x00 0x00
fldcontrol[1].inuse = 0x0 fldcontrol[1].refcnt = 0x00 0x00 0x00
0x00
fldoffset[2] = 0x00, fldmask[2] = 0x00, fldvalue_dyna[2]:0x00 0x00
0x00 0x00
fldcontrol[2].inuse = 0x0 fldcontrol[2].refcnt = 0x00 0x00 0x00
0x00
fldoffset[3] = 0x00, fldmask[3] = 0x00, fldvalue_dyna[3]:0x00 0x00
0x00 0x00
fldcontrol[3].inuse = 0x0 fldcontrol[3].refcnt = 0x00 0x00 0x00
0x00
fldoffset[4] = 0x00, fldmask[4] = 0x00, fldvalue_dyna[4]:0x00 0x00
0x00 0x00
fldcontrol[4].inuse = 0x0 fldcontrol[4].refcnt = 0x00 0x00 0x00
0x00
fldoffset[5] = 0x00, fldmask[5] = 0x00, fldvalue_dyna[5]:0x00 0x00
0x00 0x00
fldcontrol[5].inuse = 0x0 fldcontrol[5].refcnt = 0x00 0x00 0x00
0x00
fldoffset[6] = 0x00, fldmask[6] = 0x00, fldvalue_dyna[6]:0x00 0x00
0x00 0x00
fldcontrol[6].inuse = 0x0 fldcontrol[6].refcnt = 0x00 0x00 0x00
0x00
fldoffset[7] = 0x00, fldmask[7] = 0x00, fldvalue_dyna[7]:0x00 0x00
0x00 0x00
fldcontrol[7].inuse = 0x0 fldcontrol[7].refcnt = 0x00 0x00 0x00
0x00
fldoffset[8] = 0x00, fldmask[8] = 0x00, fldvalue_dyna[8]:0x00 0x00
0x00 0x00
fldcontrol[8].inuse = 0x0 fldcontrol[8].refcnt = 0x00 0x00 0x00
0x00
fldoffset[9] = 0x00, fldmask[9] = 0x00, fldvalue_dyna[9]:0x00 0x00
0x00 0x00
fldcontrol[9].inuse = 0x0 fldcontrol[9].refcnt = 0x00 0x00 0x00
0x00
fldoffset[10] = 0x00, fldmask[10] = 0x00, fldvalue_dyna[10]:0x00 0x00
0x00 0x00
fldcontrol[10].inuse = 0x0 fldcontrol[10].refcnt = 0x00 0x00 0x00
0x00
fldoffset[11] = 0x00, fldmask[11] = 0x00, fldvalue_dyna[11]:0x00 0x00
0x00 0x00
fldcontrol[11].inuse = 0x0 fldcontrol[11].refcnt = 0x00 0x00 0x00
0x00
fldoffset[12] = 0x00, fldmask[12] = 0x00, fldvalue_dyna[12]:0x00 0x00
0x00 0x00
fldcontrol[12].inuse = 0x0 fldcontrol[12].refcnt = 0x00 0x00 0x00
0x00
fldoffset[13] = 0x00, fldmask[13] = 0x00, fldvalue_dyna[13]:0x00 0x00
```


0x00000000

Field dirty indicator: 0x00000000

FDB reference count fdb: 0 [0 0 0 0]
FDB reference count fdb: 1 [0 0 0 0]
FDB reference count fdb: 2 [0 0 0 0]
FDB reference count fdb: 3 [0 0 0 0]
FDB reference count fdb: 4 [0 0 0 0]
FDB reference count fdb: 5 [0 0 0 0]
FDB reference count fdb: 6 [0 0 0 0]
FDB reference count fdb: 7 [0 0 0 0]
FDB reference count fdb: 8 [0 0 0 0]
FDB reference count fdb: 9 [0 0 0 0]
FDB reference count fdb: 10 [0 0 0 0]
FDB reference count fdb: 11 [0 0 0 0]
FDB reference count fdb: 12 [0 0 0 0]
FDB reference count fdb: 13 [0 0 0 0]
FDB reference count fdb: 14 [0 0 0 0]
FDB reference count fdb: 15 [0 0 0 0]
FDB reference count fdb: 16 [0 0 0 0]
FDB reference count fdb: 17 [0 0 0 0]
FDB reference count fdb: 18 [0 0 0 0]
FDB reference count fdb: 19 [0 0 0 0]

Filter counters:

Filter counter 0: 0 (MIRROR1)
Filter counter 1: 0 (MIRROR2)
Filter counter 2: 0 (MIRROR3)
Filter counter 3: 0 (MIRROR4)
Filter counter 4: 0 (AEPORT_NON_MIRR_DROP)
Filter counter 5: 0 (ZONING TRAP)
Filter counter 6: 0 (FCR_EXPORT_DC)
Filter counter 7: 0 (TIN TRAP)
Filter counter 8: 0 (FICON CUP)
Filter counter 9: 0 (FICON CUP DST)
Filter counter 10: 0 (WELL KNOWN ADDR)
Filter counter 11: 0 (SIM)
Filter counter 12: 0 (UNUSED)
Filter counter 13: 0 (UNUSED)
Filter counter 14: 0 (UNUSED)
Filter counter 15: 0 (UNUSED)
Filter counter 16: 0 (PERF1)
Filter counter 17: 0 (PERF2)
Filter counter 18: 0 (PERF3)
Filter counter 19: 0 (PERF4)
Filter counter 20: 0 (PERF5)
Filter counter 21: 0 (PERF6)
Filter counter 22: 0 (PERF7)
Filter counter 23: 0 (PERF8)
Filter counter 24: 0 (PERF9)
Filter counter 25: 0 (PERF10)
Filter counter 26: 0 (PERF11)
Filter counter 27: 0 (PERF12)
Filter counter 28: 0 (OPM1)

Filter counter 29: 0 (OPM2)
Filter counter 30: 0 (IPM1)
Filter counter 31: 0 (IPM2)

ACL DATA

Logical port 21: Hard Zoning disabled, Soft Zoning disabled
Zone type: WWN Zoning
Frames with hard zone miss: 0

*** Please use filterportshow on user port 56 to display ACL hash tables and Mirroring resources of thischip.
***We show this data only for the first physical port which is an external port.

portFcPortCmdShow --slot 0 42 3
doing portFcPortCmdShow: arg1 = 3, arg2 = -2

portshow 42
portDisableReason: None
portCFlags: 0x1
portFlags: 0x1 PRESENT U_PORT
LocalSwcFlags: 0x0
portType: 26.0
POD Port: Port is licensed
portState: 2 Offline
Protocol: FC
portPhys: 4 No_Light portScn: 2 Offline
port generation number: 0
state transition count: 1

portId: 012a00
portIfId: 43020012
portWwn: 20:2a:d8:1f:cc:2c:99:90
portWwn of device(s) connected:
16b Area list:
Distance: normal
portSpeed: N32Gbps

FEC: Inactive
Credit Recovery: Inactive
LE domain: 0
Peer beacon: Off
FC Fastwrite: OFF

| | | | | |
|-------------|---|---------------|---|-------|
| Interrupts: | 0 | Link_failure: | 0 | Frjt: |
| 0 | | | | |
| Unknown: | 0 | Loss_of_sync: | 0 | Fbsy: |
| 0 | | | | |
| Lli: | 0 | Loss_of_sig: | 0 | |
| Proc_rqrd: | 0 | Protocol_err: | 0 | |
| Timed_out: | 0 | Invalid_word: | 0 | |
| Tx_unavail: | 0 | Invalid_crc: | 0 | |
| Delim_err: | 0 | Address_err: | 0 | |
| Lr_in: | 0 | Ols_in: | 0 | |

Lr_out: 0 Ols_out: 0

portloginshow 42

| Type | PID | World Wide Name | credit | df_sz | cos |
|------|-----|-----------------|--------|-------|-----|
|------|-----|-----------------|--------|-------|-----|

portloginshow 42 -history

| Type | PID | World Wide Name | logout time |
|------|-----|-----------------|-------------|
|------|-----|-----------------|-------------|

portregshow 42

LED registers

| | | |
|---------------------------|----------|-------------|
| 0x81c92000: c4_led_status | 00000000 | 0x81c92004: |
| c4_led_ctl | 00000000 | |

FPL registers

| | | |
|---------------------------------|----------|-------------|
| 0x81c90200: fpl_port_config | 23298002 | |
| 0x81c9020c: fpl_port_id_ctl | 00000000 | 0x81c90210: |
| fpl_port_id_addr | 00012a00 | |
| 0x81c90214: fpl_port_speed | 00000004 | 0x81c9021c: |
| fpl_lli_ctl | 00000100 | |
| 0x81c90228: fpl_lli_os_ctl | bc94ffff | 0x81c9022c: |
| fpl_lli_send_word | bc95b5b5 | |
| 0x81c90230: fpl_lli_mark_rx | 00000000 | 0x81c90234: |
| fpl_lli_rnd_trip_time | 00000000 | |
| 0x81c90238: fpl_lli_ns_status | 00130007 | 0x81c9023c: |
| fpl_lli_intr_status | 00030007 | |
| 0x81c90244: fpl_lli_def | 00100000 | 0x81c90254: |
| fpl_lli_intr_enable_clr | 001c0000 | |
| 0x81c90258: fpl_err_intr_status | 00000000 | 0x81c90260: |
| fpl_err_intr_enable_clr | 00000000 | |
| 0x81c90268: fpl_err_first_error | 00000000 | 0x81c9026c: |
| fpl_speed_neg_ctl | 00000000 | |
| 0x81c90270: fpl_speed_neg_stat | 00000000 | 0x81c90274: |
| fpl_softasn_ctl | 0000000f | |
| 0x81c90278: fpl_link_init_ctl | 00000000 | 0x81c9027c: |
| fpl_link_init_stat | 00000000 | |
| 0x81c90280: fpl_aec_ctl | 001c1060 | 0x81c90284: |
| fpl_aec_ctl2 | 04009f60 | |
| 0x81c90288: fpl_pcs_ctl | 00000170 | 0x81c9028c: |
| fpl_fec_ctl | 00000424 | |
| 0x81c90290: fpl_fec_cor | 00000000 | 0x81c90294: |
| fpl_fec_uncor | 00000000 | |
| 0x81c90298: fpl_hss_link_ctl | 0031f040 | 0x81c9029c: |
| fpl_afifo_link_ctl | 00000a86 | |
| 0x81c902a0: fpl_echo_lb_ctl | 0000028c | 0x81c902a4: |
| fpl_scratch | 00000121 | |
| 0x81c902a8: fpl_debug | 00060005 | 0x81c902ac: |

```

fpl_misc_debug          00000800
0x00000000: SW_shadow_reg          00000000      0x00000000:
SW_c4_phyp->cfgptr      00030003

```

per-fpg (per octet) registers

```

=====
0x8181382c: fpg_serdes_ctla0          81a37be7      0x81813830:
fpg_serdes_ctla1          81a37be7
0x81813834: fpg_serdes_ctlb0          81a1c3c3      0x81813838:
fpg_serdes_ctlb1          81a1c3c3
0x8181383c: fpg_serdes_xgmii_1ms      00067c28      0x81813840:
fpg_serdes_regtimctl      40e47946
0x81813844: fpg_serdes_asnrsttimctl 00000102

```

HSS PLL registers

```

=====
0x81811400: 00_hsspll_vco_coarse_cal0      00000000      0x81811404:
01_hsspll_vco_coarse_cal1      00000014
0x81811408: 02_hsspll_vco_coarse_cal2      00000000      0x8181140c:
03_hsspll_vco_coarse_cal3      00000000
0x81811410: 04_hsspll_vco_coarse_cal4      00000000      0x81811424:
09_hsspll_power_ctl            00000000
0x81811428: 0A_hsspll_charge_pump_ctl        00000004      0x81811438:
0E_hsspll_pll_misc_ctl         00000000
0x8181143c: 0F_hsspll_pclk_ctl              000000f8      0x81811440:
10_hsspll_eyem_intv_ctl        00000000
0x81811444: 11_hsspll_eyem_intv_lim1          00000000      0x81811448:
12_hsspll_eyem_intv_lim2        00000000
0x8181144c: 13_hsspll_eyem_intv_lim3          00000000      0x81811450:
14_hsspll_eyem_intv_lim4        00000000
0x818114f0: 3C_hsspll_macro_tst_ctl4          00000000      0x818114f4:
3D_hsspll_macro_tst_ctl3        00000000
0x818114f8: 3E_hsspll_macro_tst_ctl2          00000000      0x818114fc:
3F_hsspll_macro_tst_ctl1        00000000
0x81811500: 00_hsspll_vco_coarse_cal0          0000000a      0x81811504:
01_hsspll_vco_coarse_cal1        00000014
0x81811508: 02_hsspll_vco_coarse_cal2          00000000      0x8181150c:
03_hsspll_vco_coarse_cal3        00000000
0x81811510: 04_hsspll_vco_coarse_cal4          00000000      0x81811524:
09_hsspll_power_ctl            00000000
0x81811528: 0A_hsspll_charge_pump_ctl          00000004      0x81811538:
0E_hsspll_pll_misc_ctl         00000000
0x8181153c: 0F_hsspll_pclk_ctl              000000f8      0x81811540:
10_hsspll_eyem_intv_ctl        00000000
0x81811544: 11_hsspll_eyem_intv_lim1          00000000      0x81811548:
12_hsspll_eyem_intv_lim2        00000000
0x8181154c: 13_hsspll_eyem_intv_lim3          00000000      0x81811550:
14_hsspll_eyem_intv_lim4        00000000
0x818115f0: 3C_hsspll_macro_tst_ctl4          00000000      0x818115f4:
3D_hsspll_macro_tst_ctl3        00000000
0x818115f8: 3E_hsspll_macro_tst_ctl2          00000000      0x818115fc:
3F_hsspll_macro_tst_ctl1        00000000

```

HSS TX registers

```

=====
0x81810400: 00_hsstx_cfg_mode_PHY          00009f48    0x81810404:
01_hsstx_test_ctl                      00000000
0x81810408: 02_hsstx_coeff_ctl_INV              00000000    0x8181040c:
03_hsstx_drv_mode_ctl                  00000000
0x81810410: 04_hsstx_drv_ovrd_ctl                00000010    0x81810414:
05_hsstx_dclk_align_ovrd               00000080
0x81810418: 06_hsstx_imp_cal_ovrd                00000c0c    0x8181041c:
07_hsstx_dclk_drift_tol                 00000004
0x81810420: 08_hsstx_tap0_coeff_TUNE             00000000    0x81810424:
09_hsstx_tap1_coeff_TUNE                00000003
0x81810428: 0A_hsstx_tap2_coeff_TUNE             00000019    0x8181042c:
0B_hsstx_tap3_coeff_TUNE                00000003
0x81810434: 0D_hsstx_pol_INV                     0000000a    0x81810438:
0E_hsstx_ae_cmd                         00000000
0x8181043c: 0F_hsstx_ae_stat                     00000000    0x81810440:
10_hsstx_ae_tap0_TUNE                   00000000
0x81810444: 11_hsstx_ae_tap1_TUNE                00000000    0x81810448:
12_hsstx_ae_tap2_TUNE                   00000028
0x8181044c: 13_hsstx_ae_tap3_TUNE                00000000    0x81810454:
15_hsstx_app_tune                       0000120e
0x81810458: 16_hsstx_analog_diag                 00000000    0x81810460:
18_hsstx_4x_seg_app                     0000aa00
0x81810464: 19_hsstx_2x_seg_app                 000000aa    0x81810468:
1A_hsstx_1x_seg_app                     0000f5e4
0x8181046c: 1B_hsstx_seg_4x_term_app             0000000f    0x81810470:
1C_hsstx_seg_2x1x_term_app              00000001
0x81810474: 1D_hsstx_tap_sign_app                0000000a    0x81810478:
1E_hsstx_ext_addr_data                   00000001
0x8181047c: 1F_hsstx_ext_addr_addr              00000000    0x81810480:
20_hsstx_pat_buf_bytes_1_0              00000000
0x81810484: 21_hsstx_pat_buf_bytes_3_2          00000000    0x81810488:
22_hsstx_pat_buf_bytes_5_4              00000000
0x8181048c: 23_hsstx_pat_buf_bytes_7_6          00000000    0x8181049c:
27_hsstx_8023az_ctl                     00000000
0x818104a0: 28_hsstx_dcc_ctl                     000060c0    0x818104a4:
29_hsstx_dcc_ovrd                       00000000
0x818104a8: 2A_hsstx_dcc_app                     00000106    0x818104ac:
2B_hsstx_dcc_timeout                     0000ffff
0x818104c0: 30_hsstx_tap_sign_ovrd               00000000    0x818104c8:
32_hsstx_seg_4x_ovrd                     00000000
0x818104cc: 33_hsstx_seg_2x_ovrd                 00000000    0x818104d0:
34_hsstx_seg_1x_ovrd                     00000000
0x818104d8: 36_hsstx_tap_seg_4x_term_ovrd        00000000    0x818104dc:
37_hsstx_tap_seg_2x_term_ovrd           00000000
0x818104e0: 38_hsstx_tap_seg_1x_term_ovrd        00000000    0x818104ec:
3B_hsstx_mac_test_ctl5                   00000000
0x818104f0: 3C_hsstx_mac_test_ctl4               00000000    0x818104f4:
3D_hsstx_mac_test_ctl3                   00000000
0x818104f8: 3E_hsstx_mac_test_ctl2               00000000    0x818104fc:
3F_hsstx_mac_test_ctl1                   000000c6
=====

```

HSS RX registers

=====

| | | |
|---|----------|-------------|
| 0x81810600: 00_hssrx_cfg_mode_PHY | 00009e78 | 0x81810604: |
| 01_hssrx_test_ctl | 00000000 | |
| 0x81810608: 02_hssrx_phs_rot_ctl | 0000cb80 | 0x8181060c: |
| 03_hssrx_phs_rot_ofs_ctl | 00000610 | |
| 0x81810610: 04_hssrx_phs_rot_posn1 | 0000322f | 0x81810614: |
| 05_hssrx_phs_rot_posn2 | 0000001f | |
| 0x81810618: 06_hssrx_phs_rot_sta_ofs1 | 00000103 | 0x8181061c: |
| 07_hssrx_phs_rot_sta_ofs2 | 00000000 | |
| 0x81810620: 08_hssrx_dfe_ctl_PHY | 00002002 | 0x81810624: |
| 09_hssrx_dfe_smpl_snap1 | 00000000 | |
| 0x81810628: 0A_hssrx_dfe_smpl_snap2 | 00008000 | 0x8181062c: |
| 0B_hssrx_vga_ctl1 | 0000400b | |
| 0x81810630: 0C_hssrx_vga_ctl2 | 00007aa0 | 0x81810634: |
| 0D_hssrx_vga_ctl3 | 000009e4 | |
| 0x81810638: 0E_hssrx_pwr_mgmt_ctl | 0000001f | 0x8181063c: |
| 0F_hssrx_iqamp_ctl1 | 0000001a | |
| 0x81810640: 10_hssrx_iqamp_ctl2 | 00000007 | 0x81810644: |
| 11_hssrx_dacap_dacan_sel | 00000003 | |
| 0x81810648: 12_hssrx_dacap_dacan | 0000ff00 | 0x8181064c: |
| 13_hssrx_daca_min | 00000000 | |
| 0x81810650: 14_hssrx_adac_ctl | 00000000 | 0x81810654: |
| 15_hssrx_ac_cp_ctl | 000031c3 | |
| 0x81810658: 16_hssrx_ac_cp_val | 00000045 | 0x8181065c: |
| 17_hssrx_dfe_h1h2h3_lcl_off_ch | 00000014 | |
| 0x81810660: 18_hssrx_dfe_h1h2h3_lcl_off_val | 00000000 | 0x81810664: |
| 19_hssrx_peaked_intg | 000000ff | |
| 0x81810668: 1A_hssrx_cdr_analog_sw | 0000ce00 | 0x8181066c: |
| 1B_hssrx_peaking_amp_init_c_PHY | 00000000 | |
| 0x81810670: 1C_hssrx_dac_dpc | 00000040 | 0x81810674: |
| 1D_hssrx_ddc | 00000000 | |
| 0x81810678: 1E_hssrx_int_stat_PHY | 00000c0f | 0x8181067c: |
| 1F_hssrx_dfe_func_ctl1_PHY | 0000ffff | |
| 0x81810680: 20_hssrx_dfe_func_ctl2_INV | 00007eff | 0x81810684: |
| 21_hssrx_ofs_ch_dcc_qcc_idx | 00002000 | |
| 0x81810688: 22_hssrx_dfe_ofs_val | 00000901 | 0x8181068c: |
| 23_hssrx_h_coeff_bist | 0000040d | |
| 0x81810690: 24_hssrx_ac_cap_bist | 00000000 | 0x81810694: |
| 25_hssrx_max_gain_path_idx_res | 00007800 | |
| 0x81810698: 26_hssrx_loff_ctl | 00000040 | 0x8181069c: |
| 27_hssrx_sigdet_ctl | 00002180 | |
| 0x818106a0: 28_hssrx_ana_ctl_sw | 00000000 | 0x818106a4: |
| 29_hssrx_intg_dac_ofs | 0000aee6 | |
| 0x818106a8: 2A_hssrx_eye_ctl | 00000000 | 0x818106ac: |
| 2B_hssrx_eye_met | 00000004 | |
| 0x818106b0: 2C_hssrx_eye_met_err_cnt | 00000000 | 0x818106b4: |
| 2D_hssrx_eye_met_pdf_eyec | 00000000 | |
| 0x818106b8: 2E_hssrx_eye_met_pat_len | 0000007f | 0x818106bc: |
| 2F_hssrx_dfe_func_ctl3 | 0000dfff | |
| 0x818106c0: 30_hssrx_dfe_tap_ctl_idx_ptr | 00000008 | 0x818106c4: |
| 31_hssrx_dfe_tap | 00003030 | |
| 0x818106c8: 32_hssrx_lte_ctl_TUNE | 00001601 | 0x818106e4: |
| 39_hssrx_int_stat2 | 0000c1ff | |
| 0x818106e8: 3A_hssrx_ac_cpl_cur_src_adj | 00000040 | 0x818106ec: |
| 3B_hssrx_dcd_ctl | 00007c81 | |

```

0x818106f0: 3C_hssrx_dcc_ctl          00000d81    0x818106f4:
3D_hssrx_qcc_ctl          0000698c
0x818106f8: 3E_hssrx_mac_test_ctl2      00000000    0x818106fc:
3F_hssrx_mac_test_ctl1    00000000
0x81810648: 12_hssrx_dacap_dacan[02]     00fd ff00
0x81810660: 18_hssrx_dfe_h1h2h3_lcl_off_va[00] 0000 0000 0000
0000 0000 0000 0000 0000
0x81810660: 18_hssrx_dfe_h1h2h3_lcl_off_va[08] 0000 0000 0000
0000 0000 0000 0000 0000
0x81810660: 18_hssrx_dfe_h1h2h3_lcl_off_va[16] 0000 0000 0000
0000 0000
0x81810688: 22_hssrx_dfe_ofs_val[00][00] 0901 0000 7f7b
0000 0778 7f01
0x81810688: 22_hssrx_dfe_ofs_val[03][00] 7f06 0000 017e
0000 7f7a 0000
0x81810688: 22_hssrx_dfe_ofs_val[06][00] 0006 0000 0103
0000 7b09 0000
0x81810688: 22_hssrx_dfe_ofs_val[09][00] 7b79 0000 7b7d
0000 7d7d 0000
0x81810688: 22_hssrx_dfe_ofs_val[12][00] 0379 0000 7d01
0000 0000 0000
0x81810688: 22_hssrx_dfe_ofs_val[15][00] 7f05 0000 0579
7f00 0702 7f00
0x81810688: 22_hssrx_dfe_ofs_val[18][00] 7d7b 0000 7e01
0000 007d 0000
0x81810688: 22_hssrx_dfe_ofs_val[21][00] 007d 0000 007d
0000 007d 0000
0x81810688: 22_hssrx_dfe_ofs_val[24][00] 7b7e 0000 7a7f
0000 7f77 0000
0x81810694: 25_hssrx_max_gain_path_idx_res[00] 005f 0854 1111
1890 20d0 28a0 308b 3800
0x81810694: 25_hssrx_max_gain_path_idx_res[08] 40c0 4890 5082
5800 6040 6800 70fa 7800
0x818106c4: 31_hssrx_dfe_tap[00]         fffe 8080 0000
0000 0030 0030 3030 3030
0x818106c4: 31_hssrx_dfe_tap[08]         3030 3030 3030
0000
0x818106e8: 3A_hssrx_ac_cpl_cur_src_adj[00] 0040 0040 0040
0040
0x818106ec: 3B_hssrx_dcd_ctl[00]         7c81 5c00 7c42
5c00 7c00
0x818106f0: 3C_hssrx_dcc_ctl[00]         0d81 0d43 0d82
0d43
0x818106f4: 3D_hssrx_qcc_ctl[00]         6942 698c

```

xfipcs, fec, aec, & aet registers

=====

```

0x81c90400: xfipcs_reg [00] 00002040 00000080 00000000
00000000 00000001 00000008 00000000 00000000
0x81c90420: xfipcs_reg [08] 00008401 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c90440: xfipcs_reg [16] 00000000 00000000 00000000
00000000 00000040 00000000 00000000 00000000
0x81c90460: xfipcs_reg [24] 00000000 00000000 00000000

```

```

00000000 00000000 00000000 00000000 00000000
0x81c90480: xfipcs_reg [32] 00000004 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c90620: fec_32g_128g_reg [08] 00000000 00008003 00000000
00000000 00000000 00000000 00000000
0x81c90648: fec_32g_128g_reg [18] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c90a00: aec_reg [00] 00000000 00000000 00000000
00000000 00000040 00000000 00000000 00002490
0x81c90c00: aet_reg [00] 000000b0 00007000 000008c4
00000000 00000000

```

bbc registers

=====

```

0x81c91800: bbc_trc 0 0 0 0 0 0 0
0
0x81c91840: bbc_trc 0 0 0 0 0 0 0
0
0x81c91880: bbc_trc 0 0 0 0 0 0 0
0
0x81c918c0: bbc_trc 0 0 0 0 0 0 0
0
0x81c91900: bbc_trc 0 0 0 0 0 0 0
0
0x81c91804: bbc_mbc 0 0 0 0 0 0 0
0
0x81c91844: bbc_mbc 0 0 0 0 0 0 0
0
0x81c91884: bbc_mbc 0 0 0 0 0 0 0
0
0x81c918c4: bbc_mbc 0 0 0 0 0 0 0
0
0x81c91904: bbc_mbc 0 0 0 0 0 0 0
0
0x81c91a00: bbc_rcc 0 0 0 0 0 0 0
0
0x81c91a20: bbc_rcc 0 0 0 0 0 0 0
0
0x81c91a40: bbc_rcc 0 0 0 0 0 0 0
0
0x81c91a60: bbc_rcc 0 0 0 0 0 0 0
0
0x81c91a80: bbc_rcc 0 0 0 0 0 0 0
0
0x81c91c00: bbc_rqc 0 0 0 0 0 0 0
0
0x81c91c20: bbc_rqc 0 0 0 0 0 0 0
0
0x81c91c40: bbc_rqc 0 0 0 0 0 0 0
0
0x81c91c60: bbc_rqc 0 0 0 0 0 0 0
0
0x81c91c80: bbc_rqc 0 0 0 0 0 0 0
0

```

| | | |
|-------------------------------------|----------|----------------------|
| 0x81c91d00: bbc_fbpc | 00000000 | 0x81c91d04: bbc_csc |
| 00000000 | | |
| 0x81c91d08: bbc_rcc_inc | 00000000 | 0x81c91d0c: |
| bbc_rqc_inc | 00000000 | |
| 0x81c91d10: bbc_fbpc_inc | 00000000 | 0x81c91d14: |
| bbc_tmc_inc | 00000000 | |
| 0x81c91d18: bbc_threshold | 00080100 | 0x81c91d1c: |
| bbc_counter_clr | 00000000 | |
| 0x81c91d20: bbc_debug_en | 00000000 | 0x81c91d24: bbc_ctrl |
| 00200120 | | |
| 0x81c91d28: bbc_rqc_rcc_thresh | 00000055 | 0x81c91d34: |
| bbc_bb_sc_n | 00000000 | |
| 0x81c91d38: bbc_crd_reco_debug | 00000000 | 0x81c91d3c: |
| bbc_crd_reco_debug_data | 00000000 | |
| 0x81c91d40: bbc_multi_frm_loss_cnt | 00000000 | 0x81c91d44: |
| bbc_multi_rdy_loss_cnt | 00000000 | |
| 0x81c91d48: bbc_1frm_loss_recov_cnt | 00000000 | 0x81c91d4c: |
| bbc_1rdy_loss_recov_cnt | 00000000 | |
| 0x81c91d58: bbc_int_status | 00000000 | 0x81c91d5c: |
| bbc_int_set | 00000000 | |
| 0x81c91d60: bbc_int_first | 00000000 | 0x81c91d64: |
| bbc_frm_rdy_rx_err_addr | 00000000 | |
| 0x81c91d68: bbc_frm_rdy_tx_err_addr | 00000000 | 0x81c91d6c: |
| bbc_trc_mbc_err_addr | 00000000 | |
| 0x81c91d70: bbc_frm_rdy_rx_dbl_ecc | 00000000 | 0x81c91d74: |
| bbc_frm_rdy_tx_dbl_ecc | 00000000 | |
| 0x81c91d78: bbc_trc_mbc_dbl_ecc | 00000000 | |
| 0x81c91d7c: bbc_fsm_status | 00001011 | 0x81c91d80: |
| bbc_force_err | 00000000 | |
| 0x81c91d84: bbc_crdt_avail0 | 00000000 | 0x81c91d88: |
| bbc_crdt_avail1 | 00000000 | |
| 0x81c91d8c: bbc_scratch | 00000000 | |

FPS registers

=====

| | | |
|--------------------------------|----------|-------------|
| 0x81c90004: fps_er_enc_in | 00000000 | 0x81c90008: |
| fps_er_crc | 00000000 | |
| 0x81c9000c: fps_er_trunc | 00000000 | 0x81c90010: |
| fps_er_toolong | 00000000 | |
| 0x81c90014: fps_er_bad_eof | 00000000 | 0x81c90018: |
| fps_er_enc_out | 00000000 | |
| 0x81c9001c: fps_er_bad_os | 00000000 | 0x81c90020: |
| fps_er_flush | 00000000 | |
| 0x81c90024: fps_er_ifg | 00000000 | 0x81c90038: |
| fps_er_crc_good_eof | 00000000 | |
| 0x81c9003c: fps_inv_arb | 00000000 | 0x81c90040: |
| fps_slow_sts_status | 00000000 | |
| 0x81c90044: fps_tx_frm_cnt | 00000000 | 0x81c90048: |
| fps_rx_frm_cnt | 00000000 | |
| 0x81c90050: fps_tx_word_cnt_hi | 00000000 | 0x81c9004c: |
| fps_tx_word_cnt_lo | 00000000 | |
| 0x81c90058: fps_rx_word_cnt_hi | 00000000 | 0x81c90054: |
| fps_rx_word_cnt_lo | 00000000 | |

BAL registers

=====

| | | |
|---------------------------------|----------|-------------|
| 0x81c97000: bal_desired_buf | 00000000 | 0x81c97004: |
| bal_alloc_buf | 00000000 | |
| 0x81c97008: bal_busy_buf | 00000000 | 0x81c9700c: |
| bal_usable_buf | 00000000 | |
| 0x81c97010: bal_max_bor_buf | 00000000 | |
| 0x81c97014: bal_busy_buf_thresh | 00000002 | |

TXQ registers

=====

| | | |
|-------------------------------------|------------------------|--|
| 0x81c93004: txq_phys_port_ctl | 00420000 | |
| 0x81c93050: txq_link_skew | 00000000 | |
| 0x81c93068: txq_cr_lk_dttm_intr_sts | [00] 00000000 00000000 | |
| 0x81c93070: txq_cr_lk_dttm_intr_en | [00] 00000000 00000000 | |
| 0x81c93024: txq_disc_frm_trap_cnt | 00000014 | |

FDS registers

=====

| | | |
|------------------------------------|----------|-------------|
| 0x81c94000: fds_rxf_ctl | 00000002 | 0x81c94004: |
| fds_rxf_wait_thresh | 00000909 | |
| 0x81c94018: fds_rxf_first_error | 00000000 | 0x81c9401c: |
| fds_rxf_first_error_info | 00000000 | |
| 0x81c94020: fds_rxf_inout_pkt_cnt | 00000000 | |
| 0x81c94008: fds_rxf_err_int_status | 00000000 | 0x81c94024: |
| fds_rxf_fifo_status | 00888888 | |
| 0x81c95000: fds_txf_ctl | 0000003a | 0x81c95004: |
| fds_txf_wait_ifg_thresh | 00a00106 | |
| 0x81c95008: fds_txf_err_int_status | 00000000 | 0x81c95024: |
| fds_txf_fifo_status | 00088888 | |
| 0x81c9502c: fds_txf_bbc_scs | 00000000 | |

Logical TXQ registers

=====

| | | |
|------------------------------------|---------------------------------|-------------|
| 0x81c93000: txq_log_port_ctl | 00000002 | 0x81c93008: |
| txq_port_status | 00000000 | |
| 0x81c9300c: txq_todo_flags | [00] 00000000 00000000 | |
| 0x81c93014: txq_spd_match_desc | [00] 00000000 00000000 00000000 | |
| 00000000 | | |
| 0x81c93024: txq_spd_match_desc | [04] 00000014 | |
| 0x81c93028: txq_vc_weight | [00] 01010101 01010101 01010101 | |
| 01010101 | | |
| 0x81c93038: txq_vc_weight | [04] 01010101 01010101 01010101 | |
| 01010101 | | |
| 0x81c93048: txq_vc_weight | [08] 01010101 00010101 | |
| 0x81c93054: txq_cong_dttm_ctrl | 00000106 | |
| 0x81c93058: txq_cong_dttm_intr_sts | [00] 00000000 00000000 | |
| 0x81c93060: txq_cong_dttm_intr_en | [00] 00000000 00000000 | |
| 0x81c93078: txq_bw_limit_en_reg | [00] 00000000 00000000 | |
| 0x81c93080: txq_bw_gua_en_reg | [00] 00000000 00000000 | |
| 0x81c93088: txq_vc_group | [00] 03030300 03030303 03030303 | |
| 03030303 | | |
| 0x81c93098: txq_vc_group | [04] 03030303 03030303 03030303 | |
| 03030303 | | |

| | | | | |
|---------------------------------|------|----------|----------|----------|
| 0x81c930a8: txq_vc_group | [08] | 03030303 | 03030303 | 00000000 |
| 00000000 | | | | |
| 0x81c930b0: txq_bw_thresh_group | [00] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c930c0: txq_bw_thresh_group | [04] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c930d0: txq_bw_thresh_group | [08] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c930e0: txq_bw_thresh_group | [12] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c930f0: txq_bw_thresh_group | [16] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c93100: txq_bw_thresh_group | [20] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c93110: txq_bw_thresh_group | [24] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c93120: txq_bw_thresh_group | [28] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c93130: txq_bw_thresh_group | [32] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c93140: txq_bw_thresh_group | [36] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |

txq Congestion detection Statistics RAM

=====

| | | |
|--------------------|----------|--------------------|
| 0x81090b40: vc[0] | 00000000 | 0x81090b44: vc[1] |
| 00000000 | | |
| 0x81090b48: vc[2] | 00000000 | 0x81090b4c: vc[3] |
| 00000000 | | |
| 0x81090b50: vc[4] | 00000000 | 0x81090b54: vc[5] |
| 00000000 | | |
| 0x81090b58: vc[6] | 00000000 | 0x81090b5c: vc[7] |
| 00000000 | | |
| 0x81090b60: vc[8] | 00000000 | 0x81090b64: vc[9] |
| 00000000 | | |
| 0x81090b68: vc[10] | 00000000 | 0x81090b6c: vc[11] |
| 00000000 | | |
| 0x81090b70: vc[12] | 00000000 | 0x81090b74: vc[13] |
| 00000000 | | |
| 0x81090b78: vc[14] | 00000000 | 0x81090b7c: vc[15] |
| 00000000 | | |
| 0x81090b80: vc[16] | 00000000 | 0x81090b84: vc[17] |
| 00000000 | | |
| 0x81090b88: vc[18] | 00000000 | 0x81090b8c: vc[19] |
| 00000000 | | |
| 0x81090b90: vc[20] | 00000000 | 0x81090b94: vc[21] |
| 00000000 | | |
| 0x81090b98: vc[22] | 00000000 | 0x81090b9c: vc[23] |
| 00000000 | | |
| 0x81090ba0: vc[24] | 00000000 | 0x81090ba4: vc[25] |
| 00000000 | | |
| 0x81090ba8: vc[26] | 00000000 | 0x81090bac: vc[27] |
| 00000000 | | |
| 0x81090bb0: vc[28] | 00000000 | 0x81090bb4: vc[29] |

```

00000000
0x81090bb8: vc[30]      00000000      0x81090bbc: vc[31]
00000000
0x81090bc0: vc[32]      00000000      0x81090bc4: vc[33]
00000000
0x81090bc8: vc[34]      00000000      0x81090bcc: vc[35]
00000000
0x81090bd0: vc[36]      00000000      0x81090bd4: vc[37]
00000000
0x81090bd8: vc[38]      00000000      0x81090bdc: vc[39]
00000000

```

Logical STS registers

=====

```

0x81584e04: sts_ftb_type1_miss  00000000
0x81584e08: sts_ftb_type2_miss  00000000
0x81584e0c: sts_ftb_type6_miss  00000000
0x81584e10: sts_hard_zoning_miss 00000000
0x81584e14: sts_lun_zoning_miss  00000000
0x81584e1c: sts_unroutable       00000000
0x81581e34: sts_rte_cl2          00000000      0x81581e38:
sts_rte_cl3          00000000      0x81581e3c: sts_rte_link_ctl
00000000      0x81584e28: sts_tx_timeout      00000000

```

Logical STS filter registers

=====

```

0x81584d80: stsflt_trig [00] 00000000 00000000 00000000
00000000
0x81584d90: stsflt_trig [04] 00000000 00000000 00000000
00000000
0x81584da0: stsflt_trig [08] 00000000 00000000 00000000
00000000
0x81584db0: stsflt_trig [12] 00000000 00000000 00000000
00000000
0x81584dc0: stsflt_trig [16] 00000000 00000000 00000000
00000000
0x81584dd0: stsflt_trig [20] 00000000 00000000 00000000
00000000
0x81584de0: stsflt_trig [24] 00000000 00000000 00000000
00000000
0x81584df0: stsflt_trig [28] 00000000 00000000 00000000
00000000
0x81584e00: stsflt_trig [32]

```

Logical STS discard registers

=====

```

0x81582a28: disc_mcast_wka 00000000      0x81582a2c:
disc_inv_did      00000000
0x81582a30: disc_cl1_cl4   00000000      0x81582a34:
disc_sid_chk_fail 00000000
0x81582a38: disc_inv_dom_egid_txpt 00000000      0x81582a3c:
disc_vft_hop_cnt_1 00000000
0x81582a40: disc_classf    00000000      0x81582a44:

```

```

disc_fcp_cdb_inv          00000000
0x81582a48: disc_vfid_trap_enabled 00000000 0x81582a4c:
disc_vfid_hdr_chk_fail  00000000
0x81582a50: disc_shim_cksum_fail  00000000 0x81582a54:
disc_fed_edit_cmd_err   00000000
0x81582a58: disc_ftb_vm_mode      00000000 0x81582a5c:
disc_ftb_agnt2_miss     00000000
0x81582a60: disc_ecb_reserved    00000000 0x81582a64:
disc_ecb_de_pad_err     00000000
0x81582a68: disc_ecb_de_tag_err   00000000 0x81582a6c:
disc_ecb_de_seq_err     00000000
0x81582a70: disc_ecb_err         00000000 0x81582a74:
disc_ftb_type4_match    00000000
0x81582a78: disc_fcp_rsp_ftb_type4 00000000 0x81582a7c:
disc_ftb_type5_match    00000000
0x81582a80: disc_ftb_type3_match  00000000 0x81582a84:
disc_els_ftb_type3      00000000
0x81582a88: disc_ftb_type1_match  00000000 0x81582a8c:
disc_els_rsp_ex_port    00000000
0x81582a90: disc_inv_drp_dps     00000000 0x81582a94:
disc_did_lookup_miss    00000000
0x81582a98: disc_ftb_type2_match  00000000 0x81582a9c:
disc_trpd_plogi_pdisc   00000000
0x81582aa0: disc_type2_lookup_miss 00000000 0x81582aa4:
disc_ftb_type6_match    00000000
0x81582aa8: disc_els_rep_ex_port  00000000 0x81582aac:
disc_els_sid_lkup_bit1  00000000
0x81582ab0: disc_els_sid_lkup_bit0 00000000 0x81582ab4:
disc_bls_frm_trap_bit1  00000000
0x81582ab8: disc_ftb_token_err    00000000 0x81582abc:
disc_asic_internal_err  00000000
0x81582ac0: disc_hard_zone_miss   00000000 0x81582ac4:
disc_lun_zone_miss      00000000
0x81582ac8: disc_flt_frame_disc   00000000 0x81582acc:
disc_flt_parity_err     00000000
0x81582ad0: disc_frame_marked_du  00000000 0x81582ad4:
disc_frame_marked_to    00000000
0x81582ad8: disc_lkup_rte_prty_err 00000000

```

portstatsshow 42

```

stat_wtx          0          4-byte words transmitted
stat_wrx          0          4-byte words received
stat_ftx          0          Frames transmitted
stat_frx          0          Frames received
stat_c2_frx       0          Class 2 frames received
stat_c3_frx       0          Class 3 frames received
stat_lc_rx        0          Link control frames
received
stat_mc_rx        0          Multicast frames
received
stat_mc_to        0          Multicast timeouts
stat_mc_tx        0          Multicast frames
transmitted

```


| | | | | |
|------------------------------|------------|---------|----------|-------------------------|
| tim_txcrd_z | 0 | | | Time TX Credit Zero |
| (2.5Us ticks) | | | | |
| tim_txcrd_z_vc 0- 3: | 0 | 0 | 0 | 0 |
| tim_txcrd_z_vc 4- 7: | 0 | 0 | 0 | 0 |
| tim_txcrd_z_vc 8-11: | 0 | 0 | 0 | 0 |
| tim_txcrd_z_vc 12-15: | 0 | 0 | 0 | 0 |
| lat_tot_pkt_vc 0- 3: | 1 | 1 | 1 | 1 |
| lat_tot_pkt_vc 4- 7: | 1 | 1 | 1 | 1 |
| lat_tot_pkt_vc 8-11: | 1 | 1 | 1 | 1 |
| lat_tot_pkt_vc 12-15: | 1 | 1 | 1 | 1 |
| lat_hi_time_vc 0- 3: | 0 | 0 | 0 | 0 |
| lat_hi_time_vc 4- 7: | 0 | 0 | 0 | 0 |
| lat_hi_time_vc 8-11: | 0 | 0 | 0 | 0 |
| lat_hi_time_vc 12-15: | 0 | 0 | 0 | 0 |
| lat_lo_time_vc 0- 3: | 1 | 1 | 1 | 1 |
| lat_lo_time_vc 4- 7: | 1 | 1 | 1 | 1 |
| lat_lo_time_vc 8-11: | 1 | 1 | 1 | 1 |
| lat_lo_time_vc 12-15: | 1 | 1 | 1 | 1 |
| max_latency_vc 0- 3: | 1 | 1 | 1 | 1 |
| max_latency_vc 4- 7: | 1 | 1 | 1 | 1 |
| max_latency_vc 8-11: | 1 | 1 | 1 | 1 |
| max_latency_vc 12-15: | 1 | 1 | 1 | 1 |
| latency_dma_ts | 09-09-2024 | UTC Mon | 08:47:24 | TXQ |
| Latency DMA TimeStamp | | | | |
| fec_cor_detected | 0 | | | Count of blocks that |
| were corrected by FEC | | | | |
| fec_uncor_detected | 0 | | | Count of blocks that |
| were left uncorrected by FEC | | | | |
| er_enc_in | 0 | | | Encoding errors inside |
| of frames | | | | |
| er_crc | 0 | | | Frames with CRC errors |
| er_trunc | 0 | | | Frames shorter than |
| minimum | | | | |
| er_toolong | 0 | | | Frames longer than |
| maximum | | | | |
| er_bad_eof | 0 | | | Frames with bad end-of- |
| frame | | | | |
| er_enc_out | 0 | | | Encoding error outside |
| of frames | | | | |
| er_bad_os | 0 | | | Invalid ordered set |
| er_pcs_blk | 0 | | | PCS block errors |
| er_rx_c3_timeout | 0 | | | Class 3 receive frames |
| discarded due to timeout | | | | |
| er_tx_c3_timeout | 0 | | | Class 3 transmit frames |
| discarded due to timeout | | | | |
| er_unroutable | 0 | | | Frames that are |
| unroutable | | | | |
| er_unreachable | 0 | | | Frame with unreachable |
| destination | | | | |
| er_other_discard | 0 | | | Other discards |
| er_type1_miss | 0 | | | frames with FTB type 1 |
| miss | | | | |
| er_type2_miss | 0 | | | frames with FTB type 2 |
| miss | | | | |

| | | |
|-----------------------|-----------------------------|--------------------------|
| er_type6_miss | 0 | frames with FTB type 6 |
| miss | | |
| er_zone_miss | 0 | frames with hard zoning |
| miss | | |
| er_lun_zone_miss | 0 | frames with LUN zoning |
| miss | | |
| er_crc_good_eof | 0 | Crc error with good eof |
| er_inv_arb | 0 | Invalid ARB |
| er_single_credit_loss | 0 | Single vcrdy/frame loss |
| on link | | |
| er_multi_credit_loss | 0 | Multiple vcrdy/frame |
| loss on link | | |
| other_credit_loss | 0 | Link timeout/complete |
| credit loss | | |
| phy_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | Timestamp of |
| phy_port stats clear | | |
| lgc_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | Timestamp of |
| lgc_port stats clear | | |
| fec_corrected_rate | 0 | FEC Corrected blocks per |
| second | | |

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| | | |
|---------------|---|--|
| stat64_wtx | 0 | top_int : 4-byte words transmitted |
| | 0 | bottom_int : 4-byte words transmitted |
| stat64_wrx | 0 | top_int : 4-byte words received |
| | 0 | bottom_int : 4-byte words received |
| stat64_ftx | 0 | top_int : Frames transmitted |
| | 0 | bottom_int : Frames transmitted |
| stat64_frx | 0 | top_int : Frames received |
| | 0 | bottom_int : Frames received |
| stat64_c2_frx | 0 | top_int : Class 2 frames received |
| | 0 | bottom_int : Class 2 frames received |
| stat64_c3_frx | 0 | top_int : Class 3 frames received |
| | 0 | bottom_int : Class 3 frames received |
| stat64_lc_rx | 0 | top_int : Link control frames received |
| | 0 | bottom_int : Link control frames |
| received | | |
| stat64_mc_rx | 0 | top_int : Multicast frames received |
| | 0 | bottom_int : Multicast frames received |
| stat64_mc_to | 0 | top_int : Multicast timeouts |
| | 0 | bottom_int : Multicast timeouts |
| stat64_mc_tx | 0 | top_int : Multicast frames transmitted |
| | 0 | bottom_int : Multicast frames |
| transmitted | | |
| tim64_rdy_pri | 0 | top_int : Time R_RDY high priority |
| | 0 | bottom_int : Time R_RDY high priority |
| tim64_txcrd_z | 0 | top_int : Time BB_credit zero |
| | 0 | bottom_int : Time BB_credit zero |
| er64_enc_in | 0 | top_int : Encoding errors inside of |
| frames | | |
| | 0 | bottom_int : Encoding errors inside of |
| frames | | |
| er64_crc | 0 | top_int : Frames with CRC errors |
| | 0 | bottom_int : Frames with CRC errors |

| | | |
|---|---|--|
| er64_trunc | 0 | top_int : Frames shorter than minimum |
| | 0 | bottom_int : Frames shorter than minimum |
| er64_toolong | 0 | top_int : Frames longer than maximum |
| | 0 | bottom_int : Frames longer than maximum |
| er64_bad_eof | 0 | top_int : Frames with bad end-of-frame |
| | 0 | bottom_int : Frames with bad end-of- |
| frame | | |
| er64_enc_out | 0 | top_int : Encoding error outside of |
| frames | | |
| | 0 | bottom_int : Encoding error outside of |
| er64_disc_c3 | 0 | top_int : Class 3 frames discarded |
| | 0 | bottom_int : Class 3 frames discarded |
| er64_pcs_blk | 0 | top_int : PCS block errors |
| | 0 | bottom_int : PCS block errors |
| stat64_rateTxFrame | 0 | Tx frame rate (fr/sec) |
| stat64_rateRxFrame | 0 | Rx frame rate (fr/sec) |
| stat64_rateTxPeakFrame | 0 | Tx peak frame rate (fr/sec) |
| stat64_rateRxPeakFrame | 0 | Rx peak frame rate (fr/sec) |
| stat64_rateTxWord | 0 | Tx Word rate (words/sec) |
| stat64_rateRxWord | 0 | Rx Word rate (words/sec) |
| stat64_rateTxPeakWord | 0 | Tx peak Word rate (words/sec) |
| stat64_rateRxPeakWord | 0 | Rx peak Word rate (words/sec) |
| stat64_PRJTFrames | 0 | top_int : Number of PRJT frames |
| returned to this port | | |
| | 0 | bottom_int : Number of PRJT |
| frames returned to this port | | |
| stat64_PBSYFrames | 0 | top_int : Number of PBSY frames |
| returned to this port | | |
| | 0 | bottom_int : Number of PBSY |
| frames returned to this port | | |
| stat64_inputBuffersFull | 0 | top_int : Number of occurrences |
| when all input buffers full | | |
| | 0 | bottom_int : Number of |
| occurrences when all input buffers full | | |
| stat64_rxClass1Frames | 0 | top_int : Number of class 1 |
| frames received | | |
| | 0 | bottom_int : Number of class 1 |
| frames received | | |
| stat64_aveTxFrameSize | 0 | Average Tx Frame size |
| stat64_aveRxFrameSize | 0 | Average Rx Frame size |
| Lr_in | 0 | top_int |
| | 0 | bottom_int |
| Ols_in | 0 | top_int |
| | 0 | bottom_int |
| Lr_out | 0 | top_int |
| | 0 | bottom_int |
| Ols_out | 0 | top_int |
| | 0 | bottom_int |
| Link_failure | 0 | top_int |
| | 0 | bottom_int |
| Invalid_CRC | 0 | top_int |
| | 0 | bottom_int |
| Invalid_word | 0 | top_int |

```

Protocol_err      0          bottom_int
                  0          top_int
Loss_of_sig       0          bottom_int
                  0          top_int
Loss_of_sync      0          bottom_int
                  0          top_int
er_bad_os         0          bottom_int
                  0          top_int : Invalid ordered set
                  0          bottom_int: Invalid ordered set

```

```

portrouteshow 42
port address ID: 0x012a00
external unicast routing table:
  0: Embedded
 255: Embedded
internal unicast routing table:
  0: Embedded

```

portcamshow 42

```

-----
Port  SID used  DID used  SID entries  DID entries
42    0         0         000000      000000
-----

```

ptbufshow, ptcreditshow, ptdatashow, ptstatsshow 42

```

S:
S:VF Enable:          1
S:
S:C4 Global Variable:
S:-----

```

```

S:trace_stop:        0
S:
S:C4 Phy Data Pointers: c4_phyp = 0xb6ad9040
S:-----

```

```

S:tnodep              0xbb83fd20      pt
   0x43028012
S:proto_phyp          0xb88096c0      phy_cfg
0xb6ada080
S:c4_chp              0x97e28000      c4_lgcp
0x97f90000
S:c4_phy_regp         0x81c90000      proc_dir
0xb8519be0
S:-----

```

```

S:magic_id            0xc4345678      num_port_timer      12
S:prev_if_id         0x43020012      S:ftx                0
   tov              0
S:initialized         1          port_idx             18
S:ui_idx              42          slot_no
   0
S:blade_idx           18          sw_usr_ports         400

```

| | | | |
|------------------------------|------------|-----------------------|-----|
| S:unused | 0 | intr_debounced | |
| 0 | | | |
| S:aec_status | 0x0 | reason_code | |
| 0 | | | |
| S:debug | 0x00000004 | debug_trc_line | 0 |
| S:rxbuf_list_head | 0xffffffff | rxbuf_list_tail | |
| 0xffffffff | | | |
| S:isAePort | 0 | port_misc_data | |
| 0 | | | |
| S:num_fault1_rx_disc | 0 | num_fault2_rx_disc | 0 |
| S:p_lli_cause0 | 0 | p_sig_regained | 0 |
| S:p_sync_regained | 0 | enc_out | |
| 0x0 | | | |
| S:cached_fps_status | 0 | cached_sts_status | 0 |
| S:cached_er_crc_good_eof | 0 | | |
| S:cached_er_bad_os | 0 | cached_er_too_long | 0 |
| S:cached_er_trunc | 0 | | |
| cached_tot_er_crc_good_eof | 0 | | |
| S:num_pt_excess_intr | 0 | num_no_fid | 0 |
| S:num_fault1_cnt | 0 | num_fault2_cnt | |
| 0 | | | |
| S:num_fault_lip | 0 | num_fault_lli | 0 |
| S:num_fault_rx_fifo | 0 | num_fault_hss | 0 |
| S:num_fault_bwait | 0 | lli_intr_prim | |
| 0 | | | |
| S:num_sw_link_to | 0 | | |
| be_link_err_mon_count | 0 | | |
| S:ecb_enc_enabled | 0 | ecb_comp_enabled | |
| 0 | | | |
| S:ecb_rsv_enc | 0 | ecb_rsv_comp | 0 |
| S:ecb_enc_bm | 0x0 | ecb_key_index | |
| 0xffffffff | | | |
| S:fab_idx | 0 | | |
| S:num_be_lto | 0 | lto_count_reset_intvl | |
| 0 | | | |
| S:lr_count_reset_intvl | 0 | num_be_lr | |
| 0 | | | |
| S:num_fault_qsfm | 0 | check_lto | |
| 0 | | | |
| S:credit_loaded | 0 | num_credit_overrun | |
| 0 | | | |
| S:fec_enabled | 0x0 | fec_los_to_flag | 0x0 |
| S:phy_stats_clear_ts | 1725611419 | pcs_err_online | |
| 0 | | | |
| S:pcs_err_light_det | 0 | pcs_err_ignore | |
| 0 | | | |
| S:pcs_blk_err | 0 | pcs_hiber | 0 |
| S:phy_port_status | 0 | ecb_enc_lr_count | |
| 0 | | | |
| S:dport_mode | 0 | avoid_lto_det | 0 |
| S:sn_debounced | 0x0 | sn_started_kr_reqd | 0 |
| S:major_timer_started | 0x0 | ready_bm | 0x0 |
| S:parln_1_bm | 0x0 | parln_0_bm | 0x0 |
| S:be_los_of_sync_event_intvl | | 0 | |

```

be_los_of_sync_event          0
S:errataPtenable_cntr        0          errataPoll_cntr
    0
S:jda_rx_sig_loss_det        0          jda_rx_sig_loss_cnt
    0
S:encrypt_blk_error          0
S:
S:      c4_trunk
S:=====
S:mark_ts                    0x0          deskew          0x0
S:master_phyp                0x0
S:
S:adelay[00]: 0x00000000 0x00000000 0x00000000 0x00000000
S:adelay[04]: 0x00000000 0x00000000 0x00000000 0x00000000
S:
S:      c4_buf
S:=====
S:tx_csc                      0          rx_csc
    0
S:ld_vc_credits              0          tx_flag          0x0
S:alloc_buffers              0          req_buffers      0
S:est_buffers                20         ld_use_est      0
S:bb_sc_n                    0          rx_bb_sc_n
    0
S:data_cr                    5          nondata_cr
    6
S:cr_enable                  0
S:ld_nondata_cr              6          tnodep
0xbb83fe00
S:tx_credits[0] 0 0 0 0 0 0 0 0
S:tx_credits[8] 0 0 0 0 0 0 0 0
S:tx_credits[16] 0 0 0 0 0 0 0 0 0 0
S:tx_credits[24] 0 0 0 0 0 0 0 0 0 0
S:tx_credits[32] 0 0 0 0 0 0 0 0 0 0
S:rx_credits[0] 0 0 0 0 0 0 0 0
S:rx_credits[8] 0 0 0 0 0 0 0 0
S:rx_credits[16] 0 0 0 0 0 0 0 0 0 0
S:rx_credits[24] 0 0 0 0 0 0 0 0 0 0
S:rx_credits[32] 0 0 0 0 0 0 0 0 0 0
S:tx_mbc[0] 0 0 0 0 0 0 0 0
S:tx_mbc[8] 0 0 0 0 0 0 0 0
S:tx_mbc[16] 0 0 0 0 0 0 0 0
S:tx_mbc[24] 0 0 0 0 0 0 0 0
S:tx_mbc[32] 0 0 0 0 0 0 0 0
S:rx_mbc[0] 0 0 0 0 0 0 0 0
S:rx_mbc[8] 0 0 0 0 0 0 0 0
S:rx_mbc[16] 0 0 0 0 0 0 0 0
S:rx_mbc[24] 0 0 0 0 0 0 0 0
S:rx_mbc[32] 0 0 0 0 0 0 0 0
S:
S:C4 Chip Variables: c4_phyp->c4_chp = 0x97e28000
S:-----
-----
S:version = 2.1

```

| | | | |
|---------------------------|---|-------------------------|-----|
| S:magic_id | 0xc4234567 | init_state | 0x8 |
| S:reset_reg_mem | 0x1 | | |
| S:ch_int0_en_bm | 0x0 | intr0_cause | 0x0 |
| S:ch_int1_en_bm | 0x0 | intr1_cause | 0x0 |
| S:ch_int2_en_bm | 0x0 | intr2_cause | 0x0 |
| S:ch | 0x43010080 | ch_cfg | |
| 0xb7013ba0 | | | |
| S:raslog_hndl.hndl | 0x0 | obj_halted | 0x0 |
| S:c4_chip_regp | 0x80000000 | c4_fpg_regp | |
| 0x81800000 | | | |
| S:num_chip_timer | 0x5 | | |
| S:hi_task_bm | 0x0 | lo_task_bm | 0x0 |
| S:c4_deferq.q_head | 0x0 | c4_deferq.q_tail | 0x0 |
| S:c4_tmrq.q_head | 0x0 | c4_tmrq.q_tail | 0x0 |
| slot_no | 0 | | |
| S:chip_inst | 0 | chip_idx | 0 |
| S:pll_initialized | 1 | | |
| pll_serdes_initialized | 1 | | |
| S:init_tries | 0 | init_ptEnableBM | |
| 0xba01b488 | | | |
| S:tick_polling | 0xb980c9c0 | sec_polling | |
| 0xb980c960 | | | |
| S:bb_fid | 129 | | |
| S:ecb_key_bm[0] | 0x0 | ecb_key_bm[1] | 0x0 |
| S:ecb_key_bm[2] | 0x0 | ecb_key_bm[3] | 0x0 |
| S:is_chip_enc_enabled | | 0 | |
| is_chip_comp_enabled | 0x0 | | |
| S:ftb_rsrcp->ftb_flags | 0x0 | act_rsrcp->act_flag | 0x1 |
| S:lue_rsrcp->lue_flags[0] | 0x0 | lue_rsrcp->lue_flags[1] | 0x0 |
| S:c4_phyp[00]: | 0xb6ab0000 0xb6ab2080 0xb6ab4100 0xb6ab6180 | | |
| S:c4_phyp[04]: | 0xb6ab9040 0xb6abb0c0 0xb6abd140 0xb6ac0000 | | |
| S:c4_phyp[08]: | 0xb6ac2080 0xb6ac4100 0xb6ac6180 0xb6ac9040 | | |
| S:c4_phyp[12]: | 0xb6acb0c0 0xb6acd140 0xb6ad0000 0xb6ad2080 | | |
| S:c4_phyp[16]: | 0xb6ad4100 0xb6ad6180 0xb6ad9040 0xb6adb0c0 | | |
| S:c4_phyp[20]: | 0xb6add140 0xb6ae0000 0xb6ae2080 0xb6ae4100 | | |
| S:c4_phyp[24]: | 0xb6ae6180 0xb6ae9040 0xb6aeb0c0 0xb6aed140 | | |
| S:c4_phyp[28]: | 0xb6af0000 0xb6af2080 0xb6af4100 0xb6af6180 | | |
| S:c4_phyp[32]: | 0xb6af9040 0xb6afb0c0 0xb6afd140 0xb6b00000 | | |
| S:c4_phyp[36]: | 0xb6b02080 0xb6b04100 0xb6b06180 0xb6b09040 | | |
| S:c4_phyp[40]: | 0xb6b0b0c0 0xb6b0d140 0xb6b10000 0xb6b12080 | | |
| S:c4_phyp[44]: | 0xb6b14100 0xb6b16180 0xb6b19040 0xb6b1b0c0 | | |
| S:c4_phyp[48]: | 0xb6b1d140 0xb6b20000 0xb6b22080 0xb6b24100 | | |
| S:c4_phyp[52]: | 0xb6b26180 0xb6b29040 0xb6b2b0c0 0xb6b2d140 | | |
| S:c4_phyp[56]: | 0xb6b30000 0xb6b32080 0xb6b34100 0xb6b36180 | | |
| S:c4_phyp[60]: | 0xb6b39040 0xb6b3b0c0 0xb6b3d140 0xb6b40000 | | |
| S:c4_lgcp[00]: | 0x97f48000 0x97f4c000 0x97f50000 0x97f54000 | | |
| S:c4_lgcp[04]: | 0x97f58000 0x97f5c000 0x97f60000 0x97f64000 | | |
| S:c4_lgcp[08]: | 0x97f68000 0x97f6c000 0x97f70000 0x97f74000 | | |
| S:c4_lgcp[12]: | 0x97f78000 0x97f7c000 0x97f80000 0x97f84000 | | |
| S:c4_lgcp[16]: | 0x97f88000 0x97f8c000 0x97f90000 0x97f94000 | | |
| S:c4_lgcp[20]: | 0x97f98000 0x97f9c000 0x97fa0000 0x97fa4000 | | |
| S:c4_lgcp[24]: | 0x97fa8000 0x97fac000 0x97fb0000 0x97fb4000 | | |
| S:c4_lgcp[28]: | 0x97fb8000 0x97fbc000 0x97fc0000 0x97fc4000 | | |

```

S:c4_lgcp[32]: 0x97fc8000 0x97fcc000 0x97fd0000 0x97fd4000
S:c4_lgcp[36]: 0x97fd8000 0x97fdc000 0x97fe0000 0x97fe4000
S:c4_lgcp[40]: 0x97fe8000 0x97fec000 0x97ff0000 0x97ff4000
S:c4_lgcp[44]: 0x97ff8000 0x97ffc000 0x8e000000 0x8e004000
S:c4_lgcp[48]: 0x8e008000 0x8e00c000 0x8e010000 0x8e014000
S:c4_lgcp[52]: 0x8e018000 0x8e01c000 0x8e020000 0x8e024000
S:c4_lgcp[56]: 0x8e028000 0x8e02c000 0x8e030000 0x8e034000
S:c4_lgcp[60]: 0x8e038000 0x8e03c000 0x8e040000 0x8e044000
S:chip_timers[00]: 0xb980c720 0xb980c780 0xb980c7e0 0xb980c840
S:chip_timers[04]: 0xb980c8a0 0xb980c900
S:disc_trap_enable_required      0x0          rxlp_disc_log_stop
      0x0
S:curr_rxlp_frm_cnt      0x0          curr_rxlp_disc_frm_cnt  0x0
S:sw_disc_frm_cnt      0x0          last_disc_frm_cnt      0x0
S:txq_nopop_pr_cnt      0x0          pollErrataDfe_ptBM
0xba01b4b0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][0]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][1] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][2]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][0] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][1]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][2] 0x0
S:
S:C4 Logical Port Variables
S:-----
-----
S:c4_lgc_regp      0x81c90000
S:c4_phyp:
S:      0xb6ad9040      0x0          0x0          0x0

S:      0x0          0x0          0x0          0x0

S:master_phyp      0xb6ad9040      if_id
0x43020012
S:min_phyp      0x0          max_phyp      0x0
S:num_phy_ports      1          lgc_num      18
S:num_iu_to      0          sw_txq_bm
0
S:port_fid      128          unused      0
S:port_group      2          lgc_stats_clear_ts
1725611419
S:domain_tbl_sel      0          area_tbl_sel
0
S:egid_tbl_sel      0
S:serv_lo_bm      0x0
S:
S:Proto Phy Variables:
S:-----
-----
S:magic_id      0xc4123456      asic_phyp
0xb6ad9040
S:port_id      0x43028012      phy_cfg
0xb6ada080
S:upsm_hdl      0xb80155a0      physm_hdl

```



```

0xb8015320
S:ov_snsn_hdl          0xb80151e0      sw_snsn_hdl
0xb8015280
S:ov_lksm_hdl         0xb80153c0      sw_lksm_hdl
0xb8015460
S:trksm_hdl          0xb8015500      lr_flag          0x0
S:lr_active          0x0              qsfm_tsr_x_rate_sel
0x0
S:
S:UPSM      UP00: UPST_PORT_DISABLED  --> UP01:
UPST_START_PORT_INIT
S:SNSM(OV)  SN00: OV_SNST_STOPPED      --> SN00: OV_SNST_STOPPED
S:SNSM(SW)  SW00: SW_SNST_STAGE_WS    --> SW00: SW_SNST_STAGE_WS
S:PHYSM     UNKNOWN      --> PP03: PHYST_NO_SIGNAL
S:LKSM(OV)  LK00: OV_LKST_INACTIVE    --> LK00: OV_LKST_INACTIVE
S:LKSM(SW)  SW13: INACTIVE            --> SW13: INACTIVE
S:TRKSM     TRK0: TRKST_INIT         --> TRK0: TRKST_INIT
S:
S:phym variables:
S:-----
-----
S:proto_phyp          0xb88096c0      phym_hdl
0xb8015320
S:force_offline      0              copper          0
S:fault_reason       0: UNKNOWN
S:phy_media_present  1
S:
S:snsn variables:
S:-----
-----
S:speed              0xff           proto_phyp
0xb88096c0
S:hw_sn_tries_left  0x0           sw_sn_tries_left  0x0
S:curr_txsp_count   0x0
S:tx_max            0x0           curr_tx_indx
0x0
S:curr_tx           0x0           curr_rxsp_count
0x0
S:rx_max            0x0           curr_rx_indx
0x0
S:curr_rx           0x0           rx_mem
0x0
S:rxsp_rec_count    0x0
S:nc_start          0x0           tx_start          0x0
S:sync_start        0x0           sync_present      0x0
S:diag_auto         0x0           diag_speed        0xff
S:striped_wd_tov    3000          hw_wd_tov
3000
S:step              0x0           qsfm28_speed_mode
0x0
S:qsfm_mode0_hw_sn_tries_left  0x0
S:qsfm_mode1_hw_sn_tries_left  0x0
S:
S:lksm variables:

```

```

S:-----
-----
S:proto_phyph          0xb88096c0      ov_lksm_hdl
0xb80153c0
sw_lksm_hdl           0xb8015460
num_lf1               0
S:hw_link_tries_left  0              sw_link_tries_left    0
S:buf_ptype           0x0           stored_entry_state     0x6
S:handshake_owner     0x0           0x0                   mark_unsent
0x0
S:busybuf_stuck       0x0           lr_wait                0x0
S:
S:trksm variables:
S:-----

```

```

S:Not a trunk port
S:
S:upsm variables:
S:-----

```

```

S:proto_phyph          0xb88096c0      upsm_hdl
0xb80155a0
S:bb_credits          0              port_beacon            0
S:port_diag_flag      0              0                      force_offline
0
S:port_fault_rsn      0: PORT_NO_FAULT
S:retry_init_rsn      0: UNKNOWN
S:limit_reason        0              linit_result           0
S:ie_fctl_mode        0              fec_in_sync_tries_left 0
S:retry_sn_fail_init  0
retry_link_fail_init  0
S:excess_lr_count     0
S:
S:c4_ch_cfg
S:-----

```

```

S:c4_desc_ring_size   256           292           256           256           292
292           2           292           292
S:thresh_def          0              16             1              0
S:intr_tries          500           cmem_pattern
0xdeadbeef
S:cmem_pattern_upwd   2              cmem_init_time        16
S:cmem_init_tries     5
S:ctrl_par_thresh     2              data_par_thresh
4
S:cam_par_thresh      4              buf_loss_thresh
12
S:crit_par_thresh     2              non_crit_par_thresh
6
S:pci_abort_thresh    10            pci_err_thresh        5
S:excess_chintr_thresh 8              sw_err_thresh         20
S:err_sample_period   300           intr_sleep
20000
S:frame_timeout       2500          proxy_dev             16384

```

```

S:vf_route      81920          qos          2048
S:stats 2048    f_redirect    2048
S:rsp_trap      2048          lun_zoning    20480
S:area_mode     0          ftb_max_loop[0] 0
S:ftb_max_loop[1] 6          ftb_max_loop[2] 9
S:ftb_max_loop[3] 10         ftb_max_loop[4] 10
S:ftb_max_loop[5] 5          ftb_max_loop[6] 6
S:ftb_seg_size[0] 0          ftb_seg_size[1] 16384
S:ftb_seg_size[2] 65536       ftb_seg_size[3] 16384
S:ftb_seg_size[4] 16384       ftb_seg_size[5] 65536
S:ftb_seg_size[6] 16384       ftb_seg_base[0] 0
S:ftb_seg_base[1] 0          ftb_seg_base[2] 65536
S:ftb_seg_base[3] 16384       ftb_seg_base[4] 32768
S:ftb_seg_base[5] 131072      ftb_seg_base[6] 49152
asic_err_monitor_period1    300
asic_err_monitor_period2    86400
zone_chk_to_poll_period 25
zone_chk_class2_reject_tov  220
S:
S:c4_phy_cfg
S:-----
-----
S:version = 2.1
S:pt          0x43028012    fab_ptr
0x9a800000
S:fabattr          0x9a8000d4    fab_iop
0x9a800050
S:cfgbm          0xbb83fb64    port_ctrl
0xb6ada098
S:pcap.pcap_bm    0x8d215547    pcap.pcap2_bm
0x588289
S:pcap.pcap3_bm    0x1bebe0c
ui_idx          42          S:slot_no
0
is_icl          0          S:sw_usr_ports    400
S:neg_speed      0 0 0 0 0 0
S:my_domain      0x1          port_mode          0x0
S:hw_sn_maxtries 100          sw_sn_maxtries
0
S:hw_link_maxtries 10          sw_link_maxtries 5
S:rx_cyc_tov     28          rttov             300
S:bufrdy_tov     300         busybuf_tov       286
S:mark_tov       300         lksm_tov          3000
S:buf_dealloc_wait 4          hw_wd_tov         3000
S:hw_lk_train_tov 150        540          hw_lk_test_tov
150
S:syswait_tx_12_lips 1          lip_rx_tov        55
S:al_time_tov    15          lp_tov            2000

```

```

S:intr_tries_port          500          intr_mod_debounce
    250
S:intr_lsrflt_debounce    500          intr_efifo_debounce    100
S:port_no_fid             3           excess_ptintr_thresh   8
S:port_fault1_thresh     100          port_fault1_spur_thresh 250
S:port_fault1_disc_thresh 500
port_fault1_disc_spur_thresh 1000
S:port_fault2_thresh     5           losync_tov             100
S:port_sw_link_to        15          en_8g_scramble
    1
frc_hw_sn_mode           0x1
S:enc_poll_thresh        0           fec_enable
    0
S:fec_in_sync_to         50          fec_in_sync_try_max
    4
S:port_be_lto_threshold  100          port_be_lr_threshold
    2
S:be_cr_in_sync_to       5
port_credit_overrun_thresh 50
S:jda_sfp_losig_tov      400
jda_sfp_losig_try_max    30
S:striped_wd_tov         3000
no_sync_debounce         1200
S:
S:    fab_iop
S:=====
S:fab_iop->interop_mode  0x0          fab_iop->lab_mode      0x0
S:fab_iop->fl_bbc         0x0          fab_iop->fl_fan
    0x0
S:fab_iop->fl_cls         0x4          fab_iop->fl_rscn
    0x0
S:fab_iop->domain_id_offset 0x60        fab_iop-
>mcdt_fabric_mode        0x0
S:fab_iop->mcdt_default_zone 0x0          fab_iop-
>mcdt_safe_zone          0x0
S:
S:    port_ctrl
S:=====
S:port_ctrl.port_type     1           port_ctrl.port_grp     2
S:port_ctrl.port_number  42          port_ctrl.vc_mode       1
S:
S:    port_ctrl.lcap
S:=====
S:has_serdes              0           has_media              1
S:topology                 1           skip_nego              0
S:skip_pnego              0           skip_init_event        0
S:en_shim                  0           speed_neg
    1
S:loop_back                0           num_speeds             5
S:fec_enable                0
S:
S:    port_ctrl.speed_list array
S:=====
S:speed_list[0].auto_neg  1           speed_list[0].lnk_speed 0x0000000a

```

```

S:speed_list[1].auto_neg 1 speed_list[1].lnk_speed 0x00000008
S:speed_list[2].auto_neg 0 speed_list[2].lnk_speed 0x00000006
S:speed_list[3].auto_neg 1 speed_list[3].lnk_speed 0x00000005
S:speed_list[4].auto_neg 0 speed_list[4].lnk_speed 0x00000003
S:speed_list[5].auto_neg 0 speed_list[5].lnk_speed 0x00000000

```

S:

S: port_ctrl.cm

S:=====

```

S:port_ctrl.cm.num_vcs 8
S:port_ctrl.cm.min_bufs 8
S:port_ctrl.cm.cr_shar_bufs 0
S:port_ctrl.vc_alloc
S:port_ctrl.vc_alloc 2 0 1 1 1 1 1 1
S:port_ctrl.vc_alloc 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.norm_vc_alloc
S:port_ctrl.norm_vc_alloc 4 0 5 5 5 5 1 1
S:port_ctrl.norm_vc_alloc 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.cm.skip_bb_credit 0
S:port_ctrl.cm.use_shim_based_sublist 0

```

S:

S: port_ctrl.serdes_set

S:=====

```

S:serdes_type 0x8
S:serdes_data_t.ibm_hss_serdes.tx_drive_power 0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b_sign 0x1
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b 0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_a 0x0
S:serdes_data_t.ibm_hss_serdes.rxeq 0x0

```

S:

S: cfgbm

S:=====

```

S:old_distance 0x0 gport_lockdown 0x0
S:tport 0x1 speed 0x0
S:disable_eport 0x0 fcacc 0x0
S:lport_lockdown 0x0 priv_lport_lockdown
0x0
S:vcxlt_linit 0x0 delay_flogi 0x0
S:isl_interop 0x0 distance 0x0
S:BufStarvFlag 0x0 credit_sharing 0x0
S:lport_halfduplex 0x0 lport_fairness 0x0
S:soft_neg 0x0 asn_frc_hwretry 0x0
S:cr_recov 0x0 fport_buffers 0x0
S:export 0x0 export_mode
0x0
S:csctl_en 0x0 mirror_port 0x0
S:fault_delay 0x0 non_dfe 0x0
S:fec_configured*(0=ENAB) 0 fec_tts
0

```

S:port_persistently_disabled (permanently) 0 (0)

S:

S: cfg property

S:=====

```

S:priv_pcfg_bm          0x00000000      lgcl_pcfg_bm
0xbb83fba4
S:fport_buffer         0x00000000
S:
S:
S:C4 Discard Cntrs: rxlp_stats = 0xb6ad93f0
S:-----
-----
S:disc_mcast_wka      0x0          disc_inv_did      0x0
S:disc_cl1_cl4       0x0          disc_sid_chk_fail 0x0
S:disc_inv_dom_egid_txpt 0x0          disc_vft_hop_cnt_1
0x0
S:disc_classf        0x0          disc_fcp_cdb_inv  0x0
S:disc_vfid_trap_enabled 0x0
disc_vfid_hdr_chk_fail 0x0
S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err 0x0
S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err 0x0
S:disc_ftb_vm_mode   0x0          disc_ftb_agn_t2_miss 0x0
S:disc_ecb_de_pad_err 0x0          disc_ecb_de_tag_err  0x0
S:disc_ecb_de_seq_err 0x0          disc_ecb_err         0x0
S:disc_ftb_type4_match 0x0          disc_fcp_rsp_ftb_type4 0x0
S:disc_fcp_rsp_ftb_type4 0x0          disc_ftb_type5_match
0x0
S:disc_ftb_type3_match 0x0          disc_els_ftb_type3   0x0
S:disc_ftb_type1_match 0x0          disc_els_rsp_ex_port 0x0
S:disc_inv_drp_dps   0x0          disc_did_lookup_miss 0x0
S:disc_ftb_type2_match 0x0          disc_trpd_plogi_pdisc 0x0
S:disc_type2_lookup_miss 0x0          disc_ftb_type6_match
0x0
S:disc_els_rep_ex_port 0x0          disc_els_sid_lkup_bit1 0x0
S:disc_els_sid_lkup_bit0 0x0
disc_bls_frm_trap_bit1 0x0
S:disc_ftb_token_err 0x0          disc_asic_internal_err 0x0
S:disc_hard_zone_miss 0x0          disc_lun_zone_miss   0x0
S:discflt_frame_disc 0x0          discflt_parity_err   0x0
S:disc_frame_marked_du 0x0          disc_frame_marked_to 0x0
E:Connection type: FE
E:Port type: F_port
E:Trunk port: No
E:Configured Speed: AUTO_SPEED_NEGO
E:Max Capable Speed: 32G
E:Current SNSM Speed: UNDEFINED
E:Hardware TX Speed: 32G (0x00000004)
E:Hardware RX Speed: 32G (0x00000040)
E:
E:Interrupts: 0          Link_failure: 0
Loss_of_sync: 0          Loss_of_sig: 0
E:Lli: 0          Invalid_word: 0
E:trapped_frm: 0          fwd_status_ok: 0
E:fwd_timeout: 0          fwd_tx_unavail: 0
E:fwd_unroutable: 0          fwd_zone_out: 0
E:fwd_other_err: 0          frm_err_discard: 0
E:Fltr listA: 0          Fltr listB: 0
E:Zone trap fwd: 0          Zone trap disc: 0

```

| | | | |
|-----------------|---|------------|---|
| E:shim_csum: | 0 | RTE_perr: | 0 |
| E:Invalid_crc: | 0 | Delim_err: | 0 |
| E:Protocol_err: | 0 | | |
| E:Lr_in: | 0 | Lr_out: | 0 |
| E:Ols_in: | 0 | Ols_out: | 0 |

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FILTER DATA

Shadow settings:

Filter Enable: 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass: 0x00000000

Real settings:

Enable RAM: 0x00000000, 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000

Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass RAM: 0x00000000

Shadowed filters:

Filter 0: Not Installed (MIRROR1)(LISTA)
c4_fldenable[0] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[0] = 0x00000000,c4_fltr_config[0] = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
c4_fldenable[1] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[1] = 0x00000000,c4_fltr_config[1] = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
c4_fldenable[2] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[2] = 0x00000000,c4_fltr_config[2] = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
c4_fldenable[3] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[3] = 0x00000000,c4_fltr_config[3] = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
c4_fldenable[4] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[4] = 0x00000000,c4_fltr_config[4] = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
c4_fldenable[5] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[5] = 0x00000000,c4_fltr_config[5] = 0x00000000

Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
c4_fldenable[6] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[6] = 0x00000000,c4_fltr_config[6] = 0x00000000

Filter 7: Not Installed (TIN TRAP)(LISTA)
c4_fldenable[7] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[7] = 0x00000000,c4_fltr_config[7] = 0x00000000

Filter 8: Not Installed (FICON CUP)(LISTA)
c4_fldenable[8] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[8] = 0x00000000,c4_fltr_config[8] = 0x00000000

Filter 9: Not Installed (FICON CUP DST)(LISTA)
c4_fldenable[9] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[9] = 0x00000000,c4_fltr_config[9] = 0x00000000

Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
c4_fldenable[10] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[10] = 0x00000000,c4_fltr_config[10] =
0x00000000

Filter 11: Not Installed (SIM)(LISTA)
c4_fldenable[11] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[11] = 0x00000000,c4_fltr_config[11] =
0x00000000

Filter 12: Not Installed (UNUSED)(LISTA)
c4_fldenable[12] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[12] = 0x00000000,c4_fltr_config[12] =
0x00000000

Filter 13: Not Installed (UNUSED)(LISTA)
c4_fldenable[13] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[13] = 0x00000000,c4_fltr_config[13] =
0x00000000

Filter 14: Not Installed (UNUSED)(LISTA)
c4_fldenable[14] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[14] = 0x00000000,c4_fltr_config[14] =
0x00000000

Filter 15: Not Installed (UNUSED)(LISTA)
c4_fldenable[15] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[15] = 0x00000000,c4_fltr_config[15] =
0x00000000

Filter 16: Not Installed (PERF1)(LISTA)
c4_fldenable[16] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[16] = 0x00000000,c4_fltr_config[16] =
0x00000000

Filter 17: Not Installed (PERF2)(LISTA)
c4_fldenable[17] = 0x00000000 0x00000000 0x00000000
0x00000000

```
    c4_fldnegate[17] = 0x00000000,c4_fltr_config[17] =
0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
    c4_fldenable[18] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[18] = 0x00000000,c4_fltr_config[18] =
0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
    c4_fldenable[19] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[19] = 0x00000000,c4_fltr_config[19] =
0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
    c4_fldenable[20] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[20] = 0x00000000,c4_fltr_config[20] =
0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
    c4_fldenable[21] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[21] = 0x00000000,c4_fltr_config[21] =
0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
    c4_fldenable[22] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[22] = 0x00000000,c4_fltr_config[22] =
0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
    c4_fldenable[23] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[23] = 0x00000000,c4_fltr_config[23] =
0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
    c4_fldenable[24] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[24] = 0x00000000,c4_fltr_config[24] =
0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
    c4_fldenable[25] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[25] = 0x00000000,c4_fltr_config[25] =
0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
    c4_fldenable[26] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[26] = 0x00000000,c4_fltr_config[26] =
0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
    c4_fldenable[27] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[27] = 0x00000000,c4_fltr_config[27] =
0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
    c4_fldenable[28] = 0x00000000 0x00000000 0x00000000
```

```
0x00000000
    c4_fldnegate[28] = 0x00000000,c4_fltr_config[28] =
0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
    c4_fldenable[29] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[29] = 0x00000000,c4_fltr_config[29] =
0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    c4_fldenable[30] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[30] = 0x00000000,c4_fltr_config[30] =
0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    c4_fldenable[31] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[31] = 0x00000000,c4_fltr_config[31] =
0x00000000
```

Real filters:

```
Filter 0: Not Installed (MIRROR1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
```

Filter 8: Not Installed (FICON CUP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 9: Not Installed (FICON CUP DST)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 11: Not Installed (SIM)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 12: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 13: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 14: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 15: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 16: Not Installed (PERF1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 17: Not Installed (PERF2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 18: Not Installed (PERF3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 19: Not Installed (PERF4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 20: Not Installed (PERF5)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 21: Not Installed (PERF6)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,

0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter dirty indicator: 0x00000000
Performance filters: 0
Port Mirror filters: 0 (0x0)

FIELD DATA

Shadowed fields:

fldoffset[0] = 0x00, fldmask[0] = 0x00, fldvalue_dyna[0]: 0x00 0x00

```
0x00 0x00
fldcontrol[0].inuse = 0x0  fldcontrol[0].refcnt = 0x00 0x00 0x00
0x00
fldoffset[1] = 0x00, fldmask[1] = 0x00, fldvalue_dyna[1]:0x00 0x00
0x00 0x00
fldcontrol[1].inuse = 0x0  fldcontrol[1].refcnt = 0x00 0x00 0x00
0x00
fldoffset[2] = 0x00, fldmask[2] = 0x00, fldvalue_dyna[2]:0x00 0x00
0x00 0x00
fldcontrol[2].inuse = 0x0  fldcontrol[2].refcnt = 0x00 0x00 0x00
0x00
fldoffset[3] = 0x00, fldmask[3] = 0x00, fldvalue_dyna[3]:0x00 0x00
0x00 0x00
fldcontrol[3].inuse = 0x0  fldcontrol[3].refcnt = 0x00 0x00 0x00
0x00
fldoffset[4] = 0x00, fldmask[4] = 0x00, fldvalue_dyna[4]:0x00 0x00
0x00 0x00
fldcontrol[4].inuse = 0x0  fldcontrol[4].refcnt = 0x00 0x00 0x00
0x00
fldoffset[5] = 0x00, fldmask[5] = 0x00, fldvalue_dyna[5]:0x00 0x00
0x00 0x00
fldcontrol[5].inuse = 0x0  fldcontrol[5].refcnt = 0x00 0x00 0x00
0x00
fldoffset[6] = 0x00, fldmask[6] = 0x00, fldvalue_dyna[6]:0x00 0x00
0x00 0x00
fldcontrol[6].inuse = 0x0  fldcontrol[6].refcnt = 0x00 0x00 0x00
0x00
fldoffset[7] = 0x00, fldmask[7] = 0x00, fldvalue_dyna[7]:0x00 0x00
0x00 0x00
fldcontrol[7].inuse = 0x0  fldcontrol[7].refcnt = 0x00 0x00 0x00
0x00
fldoffset[8] = 0x00, fldmask[8] = 0x00, fldvalue_dyna[8]:0x00 0x00
0x00 0x00
fldcontrol[8].inuse = 0x0  fldcontrol[8].refcnt = 0x00 0x00 0x00
0x00
fldoffset[9] = 0x00, fldmask[9] = 0x00, fldvalue_dyna[9]:0x00 0x00
0x00 0x00
fldcontrol[9].inuse = 0x0  fldcontrol[9].refcnt = 0x00 0x00 0x00
0x00
fldoffset[10] = 0x00, fldmask[10] = 0x00, fldvalue_dyna[10]:0x00 0x00
0x00 0x00
fldcontrol[10].inuse = 0x0  fldcontrol[10].refcnt = 0x00 0x00 0x00
0x00
fldoffset[11] = 0x00, fldmask[11] = 0x00, fldvalue_dyna[11]:0x00 0x00
0x00 0x00
fldcontrol[11].inuse = 0x0  fldcontrol[11].refcnt = 0x00 0x00 0x00
0x00
fldoffset[12] = 0x00, fldmask[12] = 0x00, fldvalue_dyna[12]:0x00 0x00
0x00 0x00
fldcontrol[12].inuse = 0x0  fldcontrol[12].refcnt = 0x00 0x00 0x00
0x00
fldoffset[13] = 0x00, fldmask[13] = 0x00, fldvalue_dyna[13]:0x00 0x00
0x00 0x00
fldcontrol[13].inuse = 0x0  fldcontrol[13].refcnt = 0x00 0x00 0x00
```


FDB reference count fdb: 0 [0 0 0 0]
FDB reference count fdb: 1 [0 0 0 0]
FDB reference count fdb: 2 [0 0 0 0]
FDB reference count fdb: 3 [0 0 0 0]
FDB reference count fdb: 4 [0 0 0 0]
FDB reference count fdb: 5 [0 0 0 0]
FDB reference count fdb: 6 [0 0 0 0]
FDB reference count fdb: 7 [0 0 0 0]
FDB reference count fdb: 8 [0 0 0 0]
FDB reference count fdb: 9 [0 0 0 0]
FDB reference count fdb: 10 [0 0 0 0]
FDB reference count fdb: 11 [0 0 0 0]
FDB reference count fdb: 12 [0 0 0 0]
FDB reference count fdb: 13 [0 0 0 0]
FDB reference count fdb: 14 [0 0 0 0]
FDB reference count fdb: 15 [0 0 0 0]
FDB reference count fdb: 16 [0 0 0 0]
FDB reference count fdb: 17 [0 0 0 0]
FDB reference count fdb: 18 [0 0 0 0]
FDB reference count fdb: 19 [0 0 0 0]

Filter counters:

Filter counter 0: 0 (MIRROR1)
Filter counter 1: 0 (MIRROR2)
Filter counter 2: 0 (MIRROR3)
Filter counter 3: 0 (MIRROR4)
Filter counter 4: 0 (AEPORT_NON_MIRR_DROP)
Filter counter 5: 0 (ZONING TRAP)
Filter counter 6: 0 (FCR_EXPORT_DC)
Filter counter 7: 0 (TIN TRAP)
Filter counter 8: 0 (FICON CUP)
Filter counter 9: 0 (FICON CUP DST)
Filter counter 10: 0 (WELL KNOWN ADDR)
Filter counter 11: 0 (SIM)
Filter counter 12: 0 (UNUSED)
Filter counter 13: 0 (UNUSED)
Filter counter 14: 0 (UNUSED)
Filter counter 15: 0 (UNUSED)
Filter counter 16: 0 (PERF1)
Filter counter 17: 0 (PERF2)
Filter counter 18: 0 (PERF3)
Filter counter 19: 0 (PERF4)
Filter counter 20: 0 (PERF5)
Filter counter 21: 0 (PERF6)
Filter counter 22: 0 (PERF7)
Filter counter 23: 0 (PERF8)
Filter counter 24: 0 (PERF9)
Filter counter 25: 0 (PERF10)
Filter counter 26: 0 (PERF11)
Filter counter 27: 0 (PERF12)
Filter counter 28: 0 (OPM1)
Filter counter 29: 0 (OPM2)
Filter counter 30: 0 (IPM1)

Filter counter 31: 0 (IPM2)

ACL DATA

Logical port 18: Hard Zoning disabled, Soft Zoning disabled
Zone type: WWN Zoning
Frames with hard zone miss: 0

*** Please use filterportshow on user port 56 to display ACL hash tables and Mirroring resources of thischip.
***We show this data only for the first physical port which is an external port.

portFcPortCmdShow --slot 0 43 3
doing portFcPortCmdShow: arg1 = 3, arg2 = -2

portshow 43
portDisableReason: None
portCFlags: 0x1
portFlags: 0x1 PRESENT U_PORT
LocalSwcFlags: 0x0
portType: 26.0
POD Port: Port is licensed
portState: 2 Offline
Protocol: FC
portPhys: 4 No_Light portScn: 2 Offline
port generation number: 0
state transition count: 1

portId: 012b00
portIfId: 43020011
portWwn: 20:2b:d8:1f:cc:2c:99:90
portWwn of device(s) connected:
16b Area list:
Distance: normal
portSpeed: N32Gbps

FEC: Inactive
Credit Recovery: Inactive
LE domain: 0
Peer beacon: Off
FC Fastwrite: OFF

| | | | | |
|-------------|---|---------------|---|-------|
| Interrupts: | 0 | Link_failure: | 0 | Frjt: |
| 0 | | | | |
| Unknown: | 0 | Loss_of_sync: | 0 | Fbsy: |
| 0 | | | | |
| Lli: | 0 | Loss_of_sig: | 0 | |
| Proc_rqrd: | 0 | Protocol_err: | 0 | |
| Timed_out: | 0 | Invalid_word: | 0 | |
| Tx_unavail: | 0 | Invalid_crc: | 0 | |
| Delim_err: | 0 | Address_err: | 0 | |
| Lr_in: | 0 | Ols_in: | 0 | |
| Lr_out: | 0 | Ols_out: | 0 | |

portloginshow 43

| Type | PID | World Wide Name | credit | df_sz | cos |
|------|-----|-----------------|--------|-------|-----|
|------|-----|-----------------|--------|-------|-----|

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portloginshow 43 -history

| Type | PID | World Wide Name | logout time |
|------|-----|-----------------|-------------|
|------|-----|-----------------|-------------|

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portregshow 43

LED registers

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| | | |
|---------------------------|----------|-------------|
| 0x81c8a000: c4_led_status | 00000000 | 0x81c8a004: |
| c4_led_ctl | 00000000 | |

FPL registers

=====

| | | |
|---------------------------------|----------|-------------|
| 0x81c88200: fpl_port_config | 23298002 | |
| 0x81c8820c: fpl_port_id_ctl | 00000000 | 0x81c88210: |
| fpl_port_id_addr | 00012b00 | |
| 0x81c88214: fpl_port_speed | 00000004 | 0x81c8821c: |
| fpl_lli_ctl | 00000100 | |
| 0x81c88228: fpl_lli_os_ctl | bc94ffff | 0x81c8822c: |
| fpl_lli_send_word | bc95b5b5 | |
| 0x81c88230: fpl_lli_mark_rx | 00000000 | 0x81c88234: |
| fpl_lli_rnd_trip_time | 00000000 | |
| 0x81c88238: fpl_lli_ns_status | 00130007 | 0x81c8823c: |
| fpl_lli_intr_status | 00030007 | |
| 0x81c88244: fpl_lli_def | 00100000 | 0x81c88254: |
| fpl_lli_intr_enable_clr | 001c0000 | |
| 0x81c88258: fpl_err_intr_status | 00000000 | 0x81c88260: |
| fpl_err_intr_enable_clr | 00000000 | |
| 0x81c88268: fpl_err_first_error | 00000000 | 0x81c8826c: |
| fpl_speed_neg_ctl | 00000000 | |
| 0x81c88270: fpl_speed_neg_stat | 00000000 | 0x81c88274: |
| fpl_softasn_ctl | 0000000f | |
| 0x81c88278: fpl_link_init_ctl | 00000000 | 0x81c8827c: |
| fpl_link_init_stat | 00000000 | |
| 0x81c88280: fpl_aec_ctl | 001c1060 | 0x81c88284: |
| fpl_aec_ctl2 | 04009f60 | |
| 0x81c88288: fpl_pcs_ctl | 00000170 | 0x81c8828c: |
| fpl_fec_ctl | 00000424 | |
| 0x81c88290: fpl_fec_cor | 00000000 | 0x81c88294: |
| fpl_fec_uncor | 00000000 | |
| 0x81c88298: fpl_hss_link_ctl | 0031f040 | 0x81c8829c: |
| fpl_afifo_link_ctl | 00000a86 | |
| 0x81c882a0: fpl_echo_lb_ctl | 0000028c | 0x81c882a4: |
| fpl_scratch | 00000121 | |
| 0x81c882a8: fpl_debug | 00060005 | 0x81c882ac: |
| fpl_misc_debug | 00000800 | |
| 0x00000000: SW_shadow_reg | 00000000 | 0x00000000: |

SW_c4_phy->cfgptr 00030003

per-fpg (per octet) registers

=====

| | | | |
|-------------|-------------------------|----------|-------------|
| 0x8181382c: | fpg_serdes_ctla0 | 81a37be7 | 0x81813830: |
| | fpg_serdes_ctla1 | 81a37be7 | |
| 0x81813834: | fpg_serdes_ctlb0 | 81a1c3c3 | 0x81813838: |
| | fpg_serdes_ctlb1 | 81a1c3c3 | |
| 0x8181383c: | fpg_serdes_xgmii_1ms | 00067c28 | 0x81813840: |
| | fpg_serdes_regtimctl | 40e47946 | |
| 0x81813844: | fpg_serdes_asnrsttimctl | 00000102 | |

HSS PLL registers

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| | | | |
|-------------|----------------------------|----------|-------------|
| 0x81811400: | 00_hssplla_vco_coarse_cal0 | 00000000 | 0x81811404: |
| | 01_hssplla_vco_coarse_cal1 | 00000014 | |
| 0x81811408: | 02_hssplla_vco_coarse_cal2 | 00000000 | 0x8181140c: |
| | 03_hssplla_vco_coarse_cal3 | 00000000 | |
| 0x81811410: | 04_hssplla_vco_coarse_cal4 | 00000000 | 0x81811424: |
| | 09_hssplla_power_ctl | 00000000 | |
| 0x81811428: | 0A_hssplla_charge_pump_ctl | 00000004 | 0x81811438: |
| | 0E_hssplla_pll_misc_ctl | 00000000 | |
| 0x8181143c: | 0F_hssplla_pclk_ctl | 000000f8 | 0x81811440: |
| | 10_hssplla_eyem_intv_ctl | 00000000 | |
| 0x81811444: | 11_hssplla_eyem_intv_lim1 | 00000000 | 0x81811448: |
| | 12_hssplla_eyem_intv_lim2 | 00000000 | |
| 0x8181144c: | 13_hssplla_eyem_intv_lim3 | 00000000 | 0x81811450: |
| | 14_hssplla_eyem_intv_lim4 | 00000000 | |
| 0x818114f0: | 3C_hssplla_macro_tst_ctl4 | 00000000 | 0x818114f4: |
| | 3D_hssplla_macro_tst_ctl3 | 00000000 | |
| 0x818114f8: | 3E_hssplla_macro_tst_ctl2 | 00000000 | 0x818114fc: |
| | 3F_hssplla_macro_tst_ctl1 | 00000000 | |
| 0x81811500: | 00_hssppll_vco_coarse_cal0 | 0000000a | 0x81811504: |
| | 01_hssppll_vco_coarse_cal1 | 00000014 | |
| 0x81811508: | 02_hssppll_vco_coarse_cal2 | 00000000 | 0x8181150c: |
| | 03_hssppll_vco_coarse_cal3 | 00000000 | |
| 0x81811510: | 04_hssppll_vco_coarse_cal4 | 00000000 | 0x81811524: |
| | 09_hssppll_power_ctl | 00000000 | |
| 0x81811528: | 0A_hssppll_charge_pump_ctl | 00000004 | 0x81811538: |
| | 0E_hssppll_pll_misc_ctl | 00000000 | |
| 0x8181153c: | 0F_hssppll_pclk_ctl | 000000f8 | 0x81811540: |
| | 10_hssppll_eyem_intv_ctl | 00000000 | |
| 0x81811544: | 11_hssppll_eyem_intv_lim1 | 00000000 | 0x81811548: |
| | 12_hssppll_eyem_intv_lim2 | 00000000 | |
| 0x8181154c: | 13_hssppll_eyem_intv_lim3 | 00000000 | 0x81811550: |
| | 14_hssppll_eyem_intv_lim4 | 00000000 | |
| 0x818115f0: | 3C_hssppll_macro_tst_ctl4 | 00000000 | 0x818115f4: |
| | 3D_hssppll_macro_tst_ctl3 | 00000000 | |
| 0x818115f8: | 3E_hssppll_macro_tst_ctl2 | 00000000 | 0x818115fc: |
| | 3F_hssppll_macro_tst_ctl1 | 00000000 | |

HSS TX registers

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| | | | |
|-------------|-----------------------|----------|-------------|
| 0x81810100: | 00_hsstx_cfg_mode_PHY | 00009f48 | 0x81810104: |
|-------------|-----------------------|----------|-------------|

| | | |
|---|----------|-------------|
| 01_hsstx_test_ctl | 00000000 | |
| 0x81810108: 02_hsstx_coeff_ctl_INV | 00000000 | 0x8181010c: |
| 03_hsstx_drv_mode_ctl | 00000000 | |
| 0x81810110: 04_hsstx_drv_ovrd_ctl | 00000010 | 0x81810114: |
| 05_hsstx_dclk_align_ovrd | 00000080 | |
| 0x81810118: 06_hsstx_imp_cal_ovrd | 00000c0c | 0x8181011c: |
| 07_hsstx_dclk_drift_tol | 00000004 | |
| 0x81810120: 08_hsstx_tap0_coeff_TUNE | 00000000 | 0x81810124: |
| 09_hsstx_tap1_coeff_TUNE | 00000003 | |
| 0x81810128: 0A_hsstx_tap2_coeff_TUNE | 00000019 | 0x8181012c: |
| 0B_hsstx_tap3_coeff_TUNE | 00000003 | |
| 0x81810134: 0D_hsstx_pol_INV | 00000004 | 0x81810138: |
| 0E_hsstx_ae_cmd | 00000000 | |
| 0x8181013c: 0F_hsstx_ae_stat | 00000000 | 0x81810140: |
| 10_hsstx_ae_tap0_TUNE | 00000000 | |
| 0x81810144: 11_hsstx_ae_tap1_TUNE | 00000000 | 0x81810148: |
| 12_hsstx_ae_tap2_TUNE | 00000028 | |
| 0x8181014c: 13_hsstx_ae_tap3_TUNE | 00000000 | 0x81810154: |
| 15_hsstx_app_tune | 0000120e | |
| 0x81810158: 16_hsstx_analog_diag | 00000000 | 0x81810160: |
| 18_hsstx_4x_seg_app | 0000aa00 | |
| 0x81810164: 19_hsstx_2x_seg_app | 000000aa | 0x81810168: |
| 1A_hsstx_1x_seg_app | 0000f5e4 | |
| 0x8181016c: 1B_hsstx_seg_4x_term_app | 0000000f | 0x81810170: |
| 1C_hsstx_seg_2x1x_term_app | 00000001 | |
| 0x81810174: 1D_hsstx_tap_sign_app | 00000004 | 0x81810178: |
| 1E_hsstx_ext_addr_data | 00000001 | |
| 0x8181017c: 1F_hsstx_ext_addr_addr | 00000000 | 0x81810180: |
| 20_hsstx_pat_buf_bytes_1_0 | 00000000 | |
| 0x81810184: 21_hsstx_pat_buf_bytes_3_2 | 00000000 | 0x81810188: |
| 22_hsstx_pat_buf_bytes_5_4 | 00000000 | |
| 0x8181018c: 23_hsstx_pat_buf_bytes_7_6 | 00000000 | 0x8181019c: |
| 27_hsstx_8023az_ctl | 00000000 | |
| 0x818101a0: 28_hsstx_dcc_ctl | 000060c0 | 0x818101a4: |
| 29_hsstx_dcc_ovrd | 00000000 | |
| 0x818101a8: 2A_hsstx_dcc_app | 00000103 | 0x818101ac: |
| 2B_hsstx_dcc_timeout | 0000ffff | |
| 0x818101c0: 30_hsstx_tap_sign_ovrd | 00000000 | 0x818101c8: |
| 32_hsstx_seg_4x_ovrd | 00000000 | |
| 0x818101cc: 33_hsstx_seg_2x_ovrd | 00000000 | 0x818101d0: |
| 34_hsstx_seg_1x_ovrd | 00000000 | |
| 0x818101d8: 36_hsstx_tap_seg_4x_term_ovrd | 00000000 | 0x818101dc: |
| 37_hsstx_tap_seg_2x_term_ovrd | 00000000 | |
| 0x818101e0: 38_hsstx_tap_seg_1x_term_ovrd | 00000000 | 0x818101ec: |
| 3B_hsstx_mac_test_ctl5 | 00000000 | |
| 0x818101f0: 3C_hsstx_mac_test_ctl4 | 00000000 | 0x818101f4: |
| 3D_hsstx_mac_test_ctl3 | 00000000 | |
| 0x818101f8: 3E_hsstx_mac_test_ctl2 | 00000000 | 0x818101fc: |
| 3F_hsstx_mac_test_ctl1 | 000000c6 | |

HSS RX registers

=====

| | | |
|-----------------------------------|----------|-------------|
| 0x81810300: 00_hssrx_cfg_mode_PHY | 00009e78 | 0x81810304: |
| 01_hssrx_test_ctl | 00000000 | |

| | | |
|---|----------|-------------|
| 0x81810308: 02_hssrx_phs_rot_ctl | 0000cb80 | 0x8181030c: |
| 03_hssrx_phs_rot_ofs_ctl | 00001610 | |
| 0x81810310: 04_hssrx_phs_rot_posn1 | 00001b1c | 0x81810314: |
| 05_hssrx_phs_rot_posn2 | 0000000b | |
| 0x81810318: 06_hssrx_phs_rot_sta_ofs1 | 0000001f | 0x8181031c: |
| 07_hssrx_phs_rot_sta_ofs2 | 00000000 | |
| 0x81810320: 08_hssrx_dfe_ctl_PHY | 00002002 | 0x81810324: |
| 09_hssrx_dfe_smpl_snap1 | 00000000 | |
| 0x81810328: 0A_hssrx_dfe_smpl_snap2 | 00008000 | 0x8181032c: |
| 0B_hssrx_vga_ctl1 | 00004006 | |
| 0x81810330: 0C_hssrx_vga_ctl2 | 00007aa0 | 0x81810334: |
| 0D_hssrx_vga_ctl3 | 000009e4 | |
| 0x81810338: 0E_hssrx_pwr_mgmt_ctl | 0000001f | 0x8181033c: |
| 0F_hssrx_iqamp_ctl1 | 00000019 | |
| 0x81810340: 10_hssrx_iqamp_ctl2 | 00000004 | 0x81810344: |
| 11_hssrx_dacap_dacan_sel | 00000003 | |
| 0x81810348: 12_hssrx_dacap_dacan | 0000ffff | 0x8181034c: |
| 13_hssrx_daca_min | 00000000 | |
| 0x81810350: 14_hssrx_adac_ctl | 00000000 | 0x81810354: |
| 15_hssrx_ac_cp_ctl | 000031c3 | |
| 0x81810358: 16_hssrx_ac_cp_val | 00000051 | 0x8181035c: |
| 17_hssrx_dfe_h1h2h3_lcl_off_ch | 00000014 | |
| 0x81810360: 18_hssrx_dfe_h1h2h3_lcl_off_val | 00000000 | 0x81810364: |
| 19_hssrx_peaked_intg | 000000ff | |
| 0x81810368: 1A_hssrx_cdr_analog_sw | 0000ce00 | 0x8181036c: |
| 1B_hssrx_peaking_amp_init_c_PHY | 00000000 | |
| 0x81810370: 1C_hssrx_dac_dpc | 00000040 | 0x81810374: |
| 1D_hssrx_ddc | 00000000 | |
| 0x81810378: 1E_hssrx_int_stat_PHY | 00001c0f | 0x8181037c: |
| 1F_hssrx_dfe_func_ctl1_PHY | 0000ffff | |
| 0x81810380: 20_hssrx_dfe_func_ctl2_INV | 00007ebf | 0x81810384: |
| 21_hssrx_ofs_ch_dcc_qcc_idx | 00002000 | |
| 0x81810388: 22_hssrx_dfe_ofs_val | 00007f01 | 0x8181038c: |
| 23_hssrx_h_coeff_bist | 00000401 | |
| 0x81810390: 24_hssrx_ac_cap_bist | 00000000 | 0x81810394: |
| 25_hssrx_max_gain_path_idx_res | 00007800 | |
| 0x81810398: 26_hssrx_loff_ctl | 00000040 | 0x8181039c: |
| 27_hssrx_sigdet_ctl | 00002580 | |
| 0x818103a0: 28_hssrx_ana_ctl_sw | 00000000 | 0x818103a4: |
| 29_hssrx_intg_dac_ofs | 0000b1dc | |
| 0x818103a8: 2A_hssrx_eye_ctl | 00000000 | 0x818103ac: |
| 2B_hssrx_eye_met | 00000004 | |
| 0x818103b0: 2C_hssrx_eye_met_err_cnt | 00000000 | 0x818103b4: |
| 2D_hssrx_eye_met_pdf_eyec | 00000000 | |
| 0x818103b8: 2E_hssrx_eye_met_pat_len | 0000007f | 0x818103bc: |
| 2F_hssrx_dfe_func_ctl3 | 0000dfff | |
| 0x818103c0: 30_hssrx_dfe_tap_ctl_idx_ptr | 00000008 | 0x818103c4: |
| 31_hssrx_dfe_tap | 00003030 | |
| 0x818103c8: 32_hssrx_lte_ctl_TUNE | 00001601 | 0x818103e4: |
| 39_hssrx_int_stat2 | 0000c1ff | |
| 0x818103e8: 3A_hssrx_ac_cpl_cur_src_adj | 00000041 | 0x818103ec: |
| 3B_hssrx_dcd_ctl | 00007c49 | |
| 0x818103f0: 3C_hssrx_dcc_ctl | 00000d83 | 0x818103f4: |
| 3D_hssrx_qcc_ctl | 00006983 | |

```

0x818103f8: 3E_hssrx_mac_test_ctl2          00000000    0x818103fc:
3F_hssrx_mac_test_ctl1          00000000
0x81810348: 12_hssrx_dacap_dacan[02]          00ff ffff
0x81810360: 18_hssrx_dfe_h1h2h3_lcl_off_va[00] 0000 0000    0000
0000 0000 0000 0000 0000
0x81810360: 18_hssrx_dfe_h1h2h3_lcl_off_va[08] 0000 0000    0000
0000 0000 0000 0000 0000
0x81810360: 18_hssrx_dfe_h1h2h3_lcl_off_va[16] 0000 0000    0000
0000 0000
0x81810388: 22_hssrx_dfe_ofs_val[00][00]      7f01 0000    7905
007f 7b7d 0000
0x81810388: 22_hssrx_dfe_ofs_val[03][00]      7b03 0000    027c
0000 7b07 007f
0x81810388: 22_hssrx_dfe_ofs_val[06][00]      7d03 007f    0003
007f 0803 7f00
0x81810388: 22_hssrx_dfe_ofs_val[09][00]      7d05 0000    010b
007f 0307 0000
0x81810388: 22_hssrx_dfe_ofs_val[12][00]      037e 0000    7901
0000 7901 0000
0x81810388: 22_hssrx_dfe_ofs_val[15][00]      0701 7f00    017f
0000 7d03 0000
0x81810388: 22_hssrx_dfe_ofs_val[18][00]      7979 0000    0301
0000 0000 007f
0x81810388: 22_hssrx_dfe_ofs_val[21][00]      0000 007f    0000
007f 0000 007f
0x81810388: 22_hssrx_dfe_ofs_val[24][00]      7f03 7f00    7b7f
007f 047c 0000
0x81810394: 25_hssrx_max_gain_path_idx_res[00] 005a 0848    1112
18a0 20df 289a 3084 3800
0x81810394: 25_hssrx_max_gain_path_idx_res[08] 40bf 488f    5079
5800 6040 6800 70fe 7800
0x818103c4: 31_hssrx_dfe_tap[00]              fffe 8080    0000
0000 0030 0030 3030 3030
0x818103c4: 31_hssrx_dfe_tap[08]              3030 3030    3030
0000
0x818103e8: 3A_hssrx_ac_cpl_cur_src_adj[00]   0041 0041    0041
0041
0x818103ec: 3B_hssrx_dcd_ctl[00]              7c49 5c00    7c81
5c00 7c00
0x818103f0: 3C_hssrx_dcc_ctl[00]              0d83 0d82    0d81
0d00
0x818103f4: 3D_hssrx_qcc_ctl[00]              6987 6983

```

xfipcs, fec, aec, & aet registers

```

=====
0x81c88400: xfipcs_reg          [00] 00002040 00000080 00000000
00000000 00000001 00000008 00000000 00000000
0x81c88420: xfipcs_reg          [08] 00008401 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c88440: xfipcs_reg          [16] 00000000 00000000 00000000
00000000 00000040 00000000 00000000 00000000
0x81c88460: xfipcs_reg          [24] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c88480: xfipcs_reg          [32] 00000004 00000000 00000000

```

```

00000000 00000000 00000000 00000000 00000000
0x81c88620: fec_32g_128g_reg [08] 00000000 00008003 00000000
00000000 00000000 00000000 00000000
0x81c88648: fec_32g_128g_reg [18] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c88a00: aec_reg [00] 00000000 00000000 00000000
00000000 00000040 00000000 00000000 00002490
0x81c88c00: aet_reg [00] 000000b0 00007000 000008c4
00000000 00000000

```

bbc registers

=====

```

0x81c89800: bbc_trc 0 0 0 0 0 0 0
0
0x81c89840: bbc_trc 0 0 0 0 0 0 0
0
0x81c89880: bbc_trc 0 0 0 0 0 0 0
0
0x81c898c0: bbc_trc 0 0 0 0 0 0 0
0
0x81c89900: bbc_trc 0 0 0 0 0 0 0
0
0x81c89804: bbc_mbc 0 0 0 0 0 0 0
0
0x81c89844: bbc_mbc 0 0 0 0 0 0 0
0
0x81c89884: bbc_mbc 0 0 0 0 0 0 0
0
0x81c898c4: bbc_mbc 0 0 0 0 0 0 0
0
0x81c89904: bbc_mbc 0 0 0 0 0 0 0
0
0x81c89a00: bbc_rcc 0 0 0 0 0 0 0
0
0x81c89a20: bbc_rcc 0 0 0 0 0 0 0
0
0x81c89a40: bbc_rcc 0 0 0 0 0 0 0
0
0x81c89a60: bbc_rcc 0 0 0 0 0 0 0
0
0x81c89a80: bbc_rcc 0 0 0 0 0 0 0
0
0x81c89c00: bbc_rqc 0 0 0 0 0 0 0
0
0x81c89c20: bbc_rqc 0 0 0 0 0 0 0
0
0x81c89c40: bbc_rqc 0 0 0 0 0 0 0
0
0x81c89c60: bbc_rqc 0 0 0 0 0 0 0
0
0x81c89c80: bbc_rqc 0 0 0 0 0 0 0
0
0x81c89d00: bbc_fbpc 00000000 0x81c89d04: bbc_csc
00000000

```

| | | |
|-------------------------------------|----------|----------------------|
| 0x81c89d08: bbc_rcc_inc | 00000000 | 0x81c89d0c: |
| bbc_rqc_inc | 00000000 | |
| 0x81c89d10: bbc_fbpc_inc | 00000000 | 0x81c89d14: |
| bbc_tmc_inc | 00000000 | |
| 0x81c89d18: bbc_threshold | 00080100 | 0x81c89d1c: |
| bbc_counter_clr | 00000000 | |
| 0x81c89d20: bbc_debug_en | 00000000 | 0x81c89d24: bbc_ctrl |
| 00200120 | | |
| 0x81c89d28: bbc_rqc_rcc_thresh | 00000055 | 0x81c89d34: |
| bbc_bb_sc_n | 00000000 | |
| 0x81c89d38: bbc_crd_reco_debug | 00000000 | 0x81c89d3c: |
| bbc_crd_reco_debug_data | 00000000 | |
| 0x81c89d40: bbc_multi_frm_loss_cnt | 00000000 | 0x81c89d44: |
| bbc_multi_rdy_loss_cnt | 00000000 | |
| 0x81c89d48: bbc_1frm_loss_recov_cnt | 00000000 | 0x81c89d4c: |
| bbc_1rdy_loss_recov_cnt | 00000000 | |
| 0x81c89d58: bbc_int_status | 00000000 | 0x81c89d5c: |
| bbc_int_set | 00000000 | |
| 0x81c89d60: bbc_int_first | 00000000 | 0x81c89d64: |
| bbc_frm_rdy_rx_err_addr | 00000000 | |
| 0x81c89d68: bbc_frm_rdy_tx_err_addr | 00000000 | 0x81c89d6c: |
| bbc_trc_mbc_err_addr | 00000000 | |
| 0x81c89d70: bbc_frm_rdy_rx_dbl_ecc | 00000000 | 0x81c89d74: |
| bbc_frm_rdy_tx_dbl_ecc | 00000000 | |
| 0x81c89d78: bbc_trc_mbc_dbl_ecc | 00000000 | |
| 0x81c89d7c: bbc_fsm_status | 00001011 | 0x81c89d80: |
| bbc_force_err | 00000000 | |
| 0x81c89d84: bbc_crdt_avail0 | 00000000 | 0x81c89d88: |
| bbc_crdt_avail1 | 00000000 | |
| 0x81c89d8c: bbc_scratch | 00000000 | |

FPS registers

=====

| | | |
|--------------------------------|----------|-------------|
| 0x81c88004: fps_er_enc_in | 00000000 | 0x81c88008: |
| fps_er_crc | 00000000 | |
| 0x81c8800c: fps_er_trunc | 00000000 | 0x81c88010: |
| fps_er_toolong | 00000000 | |
| 0x81c88014: fps_er_bad_eof | 00000000 | 0x81c88018: |
| fps_er_enc_out | 00000000 | |
| 0x81c8801c: fps_er_bad_os | 00000000 | 0x81c88020: |
| fps_er_flush | 00000000 | |
| 0x81c88024: fps_er_ifg | 00000000 | 0x81c88038: |
| fps_er_crc_good_eof | 00000000 | |
| 0x81c8803c: fps_inv_arb | 00000000 | 0x81c88040: |
| fps_slow_sts_status | 00000000 | |
| 0x81c88044: fps_tx_frm_cnt | 00000000 | 0x81c88048: |
| fps_rx_frm_cnt | 00000000 | |
| 0x81c88050: fps_tx_word_cnt_hi | 00000000 | 0x81c8804c: |
| fps_tx_word_cnt_lo | 00000000 | |
| 0x81c88058: fps_rx_word_cnt_hi | 00000000 | 0x81c88054: |
| fps_rx_word_cnt_lo | 00000000 | |

BAL registers

=====


```

0x81c8f000: bal_desired_buf      00000000    0x81c8f004:
bal_alloc_buf      00000000
0x81c8f008: bal_busy_buf      00000000    0x81c8f00c:
bal_usable_buf     00000000
0x81c8f010: bal_max_bor_buf   00000000
0x81c8f014: bal_busy_buf_thresh 00000002

```

TXQ registers

=====

```

0x81c8b004: txq_phys_port_ctl  00410000
0x81c8b050: txq_link_skew     00000000
0x81c8b068: txq_cr_lk_dttm_intr_sts [00] 00000000 00000000
0x81c8b070: txq_cr_lk_dttm_intr_en [00] 00000000 00000000
0x81c8b024: txq_disc_frm_trap_cnt 00000014

```

FDS registers

=====

```

0x81c8c000: fds_rxf_ctl      00000002    0x81c8c004:
fds_rxf_wait_thresh 00000909
0x81c8c018: fds_rxf_first_error 00000000    0x81c8c01c:
fds_rxf_first_error_info 00000000
0x81c8c020: fds_rxf_inout_pkt_cnt 00000000
0x81c8c008: fds_rxf_err_int_status 00000000    0x81c8c024:
fds_rxf_fifo_status 00888888
0x81c8d000: fds_txf_ctl      0000003a    0x81c8d004:
fds_txf_wait_ifg_thresh 00a00106
0x81c8d008: fds_txf_err_int_status 00000000    0x81c8d024:
fds_txf_fifo_status 00088888
0x81c8d02c: fds_txf_bbc_scs  00000000

```

Logical TXQ registers

=====

```

0x81c8b000: txq_log_port_ctl  00000002    0x81c8b008:
txq_port_status     00000000
0x81c8b00c: txq_todo_flags    [00] 00000000 00000000
0x81c8b014: txq_spd_match_desc [00] 00000000 00000000 00000000
00000000
0x81c8b024: txq_spd_match_desc [04] 00000014
0x81c8b028: txq_vc_weight     [00] 01010101 01010101 01010101
01010101
0x81c8b038: txq_vc_weight     [04] 01010101 01010101 01010101
01010101
0x81c8b048: txq_vc_weight     [08] 01010101 00010101
0x81c8b054: txq_cong_dttm_ctrl 00000106
0x81c8b058: txq_cong_dttm_intr_sts [00] 00000000 00000000
0x81c8b060: txq_cong_dttm_intr_en [00] 00000000 00000000
0x81c8b078: txq_bw_limit_en_reg [00] 00000000 00000000
0x81c8b080: txq_bw_gua_en_reg [00] 00000000 00000000
0x81c8b088: txq_vc_group      [00] 03030300 03030303 03030303
03030303
0x81c8b098: txq_vc_group      [04] 03030303 03030303 03030303
03030303
0x81c8b0a8: txq_vc_group      [08] 03030303 03030303 00000000
00000000

```

| | | | | |
|---------------------------------|------|----------|----------|----------|
| 0x81c8b0b0: txq_bw_thresh_group | [00] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c8b0c0: txq_bw_thresh_group | [04] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c8b0d0: txq_bw_thresh_group | [08] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c8b0e0: txq_bw_thresh_group | [12] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c8b0f0: txq_bw_thresh_group | [16] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c8b100: txq_bw_thresh_group | [20] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c8b110: txq_bw_thresh_group | [24] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c8b120: txq_bw_thresh_group | [28] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c8b130: txq_bw_thresh_group | [32] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c8b140: txq_bw_thresh_group | [36] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |

txq Congestion detection Statistics RAM

=====

| | | |
|--------------------|----------|--------------------|
| 0x81090aa0: vc[0] | 00000000 | 0x81090aa4: vc[1] |
| 00000000 | | |
| 0x81090aa8: vc[2] | 00000000 | 0x81090aac: vc[3] |
| 00000000 | | |
| 0x81090ab0: vc[4] | 00000000 | 0x81090ab4: vc[5] |
| 00000000 | | |
| 0x81090ab8: vc[6] | 00000000 | 0x81090abc: vc[7] |
| 00000000 | | |
| 0x81090ac0: vc[8] | 00000000 | 0x81090ac4: vc[9] |
| 00000000 | | |
| 0x81090ac8: vc[10] | 00000000 | 0x81090acc: vc[11] |
| 00000000 | | |
| 0x81090ad0: vc[12] | 00000000 | 0x81090ad4: vc[13] |
| 00000000 | | |
| 0x81090ad8: vc[14] | 00000000 | 0x81090adc: vc[15] |
| 00000000 | | |
| 0x81090ae0: vc[16] | 00000000 | 0x81090ae4: vc[17] |
| 00000000 | | |
| 0x81090ae8: vc[18] | 00000000 | 0x81090aec: vc[19] |
| 00000000 | | |
| 0x81090af0: vc[20] | 00000000 | 0x81090af4: vc[21] |
| 00000000 | | |
| 0x81090af8: vc[22] | 00000000 | 0x81090afc: vc[23] |
| 00000000 | | |
| 0x81090b00: vc[24] | 00000000 | 0x81090b04: vc[25] |
| 00000000 | | |
| 0x81090b08: vc[26] | 00000000 | 0x81090b0c: vc[27] |
| 00000000 | | |
| 0x81090b10: vc[28] | 00000000 | 0x81090b14: vc[29] |
| 00000000 | | |
| 0x81090b18: vc[30] | 00000000 | 0x81090b1c: vc[31] |

```

00000000
0x81090b20: vc[32]      00000000      0x81090b24: vc[33]
00000000
0x81090b28: vc[34]      00000000      0x81090b2c: vc[35]
00000000
0x81090b30: vc[36]      00000000      0x81090b34: vc[37]
00000000
0x81090b38: vc[38]      00000000      0x81090b3c: vc[39]
00000000

```

Logical STS registers

=====

```

0x81584d44: sts_ftb_type1_miss  00000000
0x81584d48: sts_ftb_type2_miss  00000000
0x81584d4c: sts_ftb_type6_miss  00000000
0x81584d50: sts_hard_zoning_miss 00000000
0x81584d54: sts_lun_zoning_miss  00000000
0x81584d5c: sts_unroutable       00000000
0x81581d74: sts_rte_cl2          00000000      0x81581d78:
sts_rte_cl3          00000000      0x81581d7c: sts_rte_link_ctl
00000000            0x81584d68: sts_tx_timeout      00000000

```

Logical STS filter registers

=====

```

0x81584cc0: stsflt_trig [00] 00000000 00000000 00000000
00000000
0x81584cd0: stsflt_trig [04] 00000000 00000000 00000000
00000000
0x81584ce0: stsflt_trig [08] 00000000 00000000 00000000
00000000
0x81584cf0: stsflt_trig [12] 00000000 00000000 00000000
00000000
0x81584d00: stsflt_trig [16] 00000000 00000000 00000000
00000000
0x81584d10: stsflt_trig [20] 00000000 00000000 00000000
00000000
0x81584d20: stsflt_trig [24] 00000000 00000000 00000000
00000000
0x81584d30: stsflt_trig [28] 00000000 00000000 00000000
00000000
0x81584d40: stsflt_trig [32]

```

Logical STS discard registers

=====

```

0x815828b4: disc_mcast_wka      00000000      0x815828b8:
disc_inv_did          00000000
0x815828bc: disc_cl1_cl4        00000000      0x815828c0:
disc_sid_chk_fail     00000000
0x815828c4: disc_inv_dom_egid_txpt 00000000      0x815828c8:
disc_vft_hop_cnt_1    00000000
0x815828cc: disc_classf          00000000      0x815828d0:
disc_fcp_cdb_inv       00000000
0x815828d4: disc_vfid_trap_enabled 00000000      0x815828d8:

```

| | | |
|------------------------------------|----------|-------------|
| disc_vfid_hdr_chk_fail | 00000000 | |
| 0x815828dc: disc_shim_cksum_fail | 00000000 | 0x815828e0: |
| disc_fed_edit_cmd_err | 00000000 | |
| 0x815828e4: disc_ftb_vm_mode | 00000000 | 0x815828e8: |
| disc_ftb_agnt2_miss | 00000000 | |
| 0x815828ec: disc_ecb_reserved | 00000000 | 0x815828f0: |
| disc_ecb_de_pad_err | 00000000 | |
| 0x815828f4: disc_ecb_de_tag_err | 00000000 | 0x815828f8: |
| disc_ecb_de_seq_err | 00000000 | |
| 0x815828fc: disc_ecb_err | 00000000 | 0x81582900: |
| disc_ftb_type4_match | 00000000 | |
| 0x81582904: disc_fcp_rsp_ftb_type4 | 00000000 | 0x81582908: |
| disc_ftb_type5_match | 00000000 | |
| 0x8158290c: disc_ftb_type3_match | 00000000 | 0x81582910: |
| disc_els_ftb_type3 | 00000000 | |
| 0x81582914: disc_ftb_type1_match | 00000000 | 0x81582918: |
| disc_els_rsp_ex_port | 00000000 | |
| 0x8158291c: disc_inv_drp_dps | 00000000 | 0x81582920: |
| disc_did_lookup_miss | 00000000 | |
| 0x81582924: disc_ftb_type2_match | 00000000 | 0x81582928: |
| disc_trpd_plogi_pdisc | 00000000 | |
| 0x8158292c: disc_type2_lookup_miss | 00000000 | 0x81582930: |
| disc_ftb_type6_match | 00000000 | |
| 0x81582934: disc_els_rep_ex_port | 00000000 | 0x81582938: |
| disc_els_sid_lkup_bit1 | 00000000 | |
| 0x8158293c: disc_els_sid_lkup_bit0 | 00000000 | 0x81582940: |
| disc_bls_frm_trap_bit1 | 00000000 | |
| 0x81582944: disc_ftb_token_err | 00000000 | 0x81582948: |
| disc_asic_internal_err | 00000000 | |
| 0x8158294c: disc_hard_zone_miss | 00000000 | 0x81582950: |
| disc_lun_zone_miss | 00000000 | |
| 0x81582954: discflt_frame_disc | 00000000 | 0x81582958: |
| discflt_parity_err | 00000000 | |
| 0x8158295c: disc_frame_marked_du | 00000000 | 0x81582960: |
| disc_frame_marked_to | 00000000 | |
| 0x81582964: disc_lkup_rte_prty_err | 00000000 | |

portstatsshow 43

| | | |
|---------------|---|--------------------------|
| stat_wtx | 0 | 4-byte words transmitted |
| stat_wrx | 0 | 4-byte words received |
| stat_ftx | 0 | Frames transmitted |
| stat_frx | 0 | Frames received |
| stat_c2_frx | 0 | Class 2 frames received |
| stat_c3_frx | 0 | Class 3 frames received |
| stat_lc_rx | 0 | Link control frames |
| received | | |
| stat_mc_rx | 0 | Multicast frames |
| received | | |
| stat_mc_to | 0 | Multicast timeouts |
| stat_mc_tx | 0 | Multicast frames |
| transmitted | | |
| tim_txcrd_z | 0 | Time TX Credit Zero |
| (2.5Us ticks) | | |

| | | | | | |
|------------------------------|-----------------------------|-------------------------|---|---|-----|
| tim_txcrd_z_vc | 0- 3: | 0 | 0 | 0 | 0 |
| tim_txcrd_z_vc | 4- 7: | 0 | 0 | 0 | 0 |
| tim_txcrd_z_vc | 8-11: | 0 | 0 | 0 | 0 |
| tim_txcrd_z_vc | 12-15: | 0 | 0 | 0 | 0 |
| lat_tot_pkt_vc | 0- 3: | 1 | 1 | 1 | 1 |
| lat_tot_pkt_vc | 4- 7: | 1 | 1 | 1 | 1 |
| lat_tot_pkt_vc | 8-11: | 1 | 1 | 1 | 1 |
| lat_tot_pkt_vc | 12-15: | 1 | 1 | 1 | 1 |
| lat_hi_time_vc | 0- 3: | 0 | 0 | 0 | 0 |
| lat_hi_time_vc | 4- 7: | 0 | 0 | 0 | 0 |
| lat_hi_time_vc | 8-11: | 0 | 0 | 0 | 0 |
| lat_hi_time_vc | 12-15: | 0 | 0 | 0 | 0 |
| lat_lo_time_vc | 0- 3: | 1 | 1 | 1 | 1 |
| lat_lo_time_vc | 4- 7: | 1 | 1 | 1 | 1 |
| lat_lo_time_vc | 8-11: | 1 | 1 | 1 | 1 |
| lat_lo_time_vc | 12-15: | 1 | 1 | 1 | 1 |
| max_latency_vc | 0- 3: | 1 | 1 | 1 | 1 |
| max_latency_vc | 4- 7: | 1 | 1 | 1 | 1 |
| max_latency_vc | 8-11: | 1 | 1 | 1 | 1 |
| max_latency_vc | 12-15: | 1 | 1 | 1 | 1 |
| latency_dma_ts | 09-09-2024 UTC Mon 08:47:24 | | | | TXQ |
| Latency DMA TimeStamp | | | | | |
| fec_cor_detected | 0 | Count of blocks that | | | |
| were corrected by FEC | | | | | |
| fec_uncor_detected | 0 | Count of blocks that | | | |
| were left uncorrected by FEC | | | | | |
| er_enc_in | 0 | Encoding errors inside | | | |
| of frames | | | | | |
| er_crc | 0 | Frames with CRC errors | | | |
| er_trunc | 0 | Frames shorter than | | | |
| minimum | | | | | |
| er_toolong | 0 | Frames longer than | | | |
| maximum | | | | | |
| er_bad_eof | 0 | Frames with bad end-of- | | | |
| frame | | | | | |
| er_enc_out | 0 | Encoding error outside | | | |
| of frames | | | | | |
| er_bad_os | 0 | Invalid ordered set | | | |
| er_pcs_blk | 0 | PCS block errors | | | |
| er_rx_c3_timeout | 0 | Class 3 receive frames | | | |
| discarded due to timeout | | | | | |
| er_tx_c3_timeout | 0 | Class 3 transmit frames | | | |
| discarded due to timeout | | | | | |
| er_unroutable | 0 | Frames that are | | | |
| unroutable | | | | | |
| er_unreachable | 0 | Frame with unreachable | | | |
| destination | | | | | |
| er_other_discard | 0 | Other discards | | | |
| er_type1_miss | 0 | frames with FTB type 1 | | | |
| miss | | | | | |
| er_type2_miss | 0 | frames with FTB type 2 | | | |
| miss | | | | | |
| er_type6_miss | 0 | frames with FTB type 6 | | | |
| miss | | | | | |

| | | |
|-----------------------|-----------------------------|--------------------------|
| er_zone_miss | 0 | frames with hard zoning |
| miss | | |
| er_lun_zone_miss | 0 | frames with LUN zoning |
| miss | | |
| er_crc_good_eof | 0 | Crc error with good eof |
| er_inv_arb | 0 | Invalid ARB |
| er_single_credit_loss | 0 | Single vcrdy/frame loss |
| on link | | |
| er_multi_credit_loss | 0 | Multiple vcrdy/frame |
| loss on link | | |
| other_credit_loss | 0 | Link timeout/complete |
| credit loss | | |
| phy_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | Timestamp of |
| phy_port stats clear | | |
| lgc_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | Timestamp of |
| lgc_port stats clear | | |
| fec_corrected_rate | 0 | FEC Corrected blocks per |
| second | | |

portstats64show 43

| | | |
|---------------|---|--|
| stat64_wtx | 0 | top_int : 4-byte words transmitted |
| | 0 | bottom_int : 4-byte words transmitted |
| stat64_wrx | 0 | top_int : 4-byte words received |
| | 0 | bottom_int : 4-byte words received |
| stat64_ftx | 0 | top_int : Frames transmitted |
| | 0 | bottom_int : Frames transmitted |
| stat64_frx | 0 | top_int : Frames received |
| | 0 | bottom_int : Frames received |
| stat64_c2_frx | 0 | top_int : Class 2 frames received |
| | 0 | bottom_int : Class 2 frames received |
| stat64_c3_frx | 0 | top_int : Class 3 frames received |
| | 0 | bottom_int : Class 3 frames received |
| stat64_lc_rx | 0 | top_int : Link control frames received |
| | 0 | bottom_int : Link control frames |
| received | | |
| stat64_mc_rx | 0 | top_int : Multicast frames received |
| | 0 | bottom_int : Multicast frames received |
| stat64_mc_to | 0 | top_int : Multicast timeouts |
| | 0 | bottom_int : Multicast timeouts |
| stat64_mc_tx | 0 | top_int : Multicast frames transmitted |
| | 0 | bottom_int : Multicast frames |
| transmitted | | |
| tim64_rdy_pri | 0 | top_int : Time R_RDY high priority |
| | 0 | bottom_int : Time R_RDY high priority |
| tim64_txcrd_z | 0 | top_int : Time BB_credit zero |
| | 0 | bottom_int : Time BB_credit zero |
| er64_enc_in | 0 | top_int : Encoding errors inside of |
| frames | | |
| | 0 | bottom_int : Encoding errors inside of |
| frames | | |
| er64_crc | 0 | top_int : Frames with CRC errors |
| | 0 | bottom_int : Frames with CRC errors |
| er64_trunc | 0 | top_int : Frames shorter than minimum |
| | 0 | bottom_int : Frames shorter than minimum |

| | | |
|---|---|---|
| er64_toolong | 0 | top_int : Frames longer than maximum |
| | 0 | bottom_int : Frames longer than maximum |
| er64_bad_eof | 0 | top_int : Frames with bad end-of-frame |
| | 0 | bottom_int : Frames with bad end-of- |
| frame | | |
| er64_enc_out | 0 | top_int : Encoding error outside of |
| frames | | |
| | 0 | bottom_int : Encoding error outside of |
| frames | | |
| er64_disc_c3 | 0 | top_int : Class 3 frames discarded |
| | 0 | bottom_int : Class 3 frames discarded |
| er64_pcs_blk | 0 | top_int : PCS block errors |
| | 0 | bottom_int : PCS block errors |
| stat64_rateTxFrame | 0 | Tx frame rate (fr/sec) |
| stat64_rateRxFrame | 0 | Rx frame rate (fr/sec) |
| stat64_rateTxPeakFrame | 0 | Tx peak frame rate (fr/sec) |
| stat64_rateRxPeakFrame | 0 | Rx peak frame rate (fr/sec) |
| stat64_rateTxWord | 0 | Tx Word rate (words/sec) |
| stat64_rateRxWord | 0 | Rx Word rate (words/sec) |
| stat64_rateTxPeakWord | 0 | Tx peak Word rate (words/sec) |
| stat64_rateRxPeakWord | 0 | Rx peak Word rate (words/sec) |
| stat64_PRJTFrames | 0 | top_int : Number of PRJT frames |
| returned to this port | | |
| | 0 | bottom_int : Number of PRJT |
| frames returned to this port | | |
| stat64_PBSYFrames | 0 | top_int : Number of PBSY frames |
| returned to this port | | |
| | 0 | bottom_int : Number of PBSY |
| frames returned to this port | | |
| stat64_inputBuffersFull | 0 | top_int : Number of occurrences |
| when all input buffers full | | |
| | 0 | bottom_int : Number of |
| occurrences when all input buffers full | | |
| stat64_rxClass1Frames | 0 | top_int : Number of class 1 |
| frames received | | |
| | 0 | bottom_int : Number of class 1 |
| frames received | | |
| stat64_aveTxFrameSize | 0 | Average Tx Frame size |
| stat64_aveRxFrameSize | 0 | Average Rx Frame size |
| Lr_in | 0 | top_int |
| | 0 | bottom_int |
| Ols_in | 0 | top_int |
| | 0 | bottom_int |
| Lr_out | 0 | top_int |
| | 0 | bottom_int |
| Ols_out | 0 | top_int |
| | 0 | bottom_int |
| Link_failure | 0 | top_int |
| | 0 | bottom_int |
| Invalid_CRC | 0 | top_int |
| | 0 | bottom_int |
| Invalid_word | 0 | top_int |
| | 0 | bottom_int |
| Protocol_err | 0 | top_int |

```

Loss_of_sig      0          bottom_int
                  0          top_int
Loss_of_sync     0          bottom_int
                  0          top_int
er_bad_os        0          bottom_int
                  0          top_int : Invalid ordered set
                  0          bottom_int: Invalid ordered set

```

```

portrouteshow 43
port address ID: 0x012b00
external unicast routing table:
  0: Embedded
 255: Embedded
internal unicast routing table:
  0: Embedded

```

```
portcamshow 43
```

```

-----
Port  SID used  DID used  SID entries  DID entries
43    0         0         000000      000000
-----

```

```
ptbufshow, ptcreditshow, ptdatashow, ptstatsshow 43
```

```

S:
S:VF Enable:          1
S:
S:C4 Global Variable:
S:-----

```

```

S:trace_stop:        0
S:
S:C4 Phy Data Pointers: c4_phyp = 0xb6ad6180
S:-----

```

```

S:tnodep              0xbb83ea80      pt
    0x43028011
S:proto_phyp          0xb8809360      phy_cfg
0xb6ad8000
S:c4_chp              0x97e28000      c4_lgcp
0x97f8c000
S:c4_phy_regp         0x81c88000      proc_dir
0xb8519500
S:-----

```

```

S:magic_id            0xc4345678      num_port_timer      12
S:prev_if_id         0x43020011      S:ftx                0
    tov              0
S:initialized         1          port_idx             17
S:ui_idx              43          slot_no
    0
S:blade_idx           17          sw_usr_ports         400
S:unused              0          intr_debounced
    0

```


| | | | |
|------------------------------|------------|-----------------------|-----|
| S:aec_status | 0x0 | reason_code | |
| 0 | | | |
| S:debug | 0x00000004 | debug_trc_line | 0 |
| S:rxbuf_list_head | 0xffffffff | rxbuf_list_tail | |
| 0xffffffff | | | |
| S:isAePort | 0 | port_misc_data | |
| 0 | | | |
| S:num_fault1_rx_disc | 0 | num_fault2_rx_disc | 0 |
| S:p_lli_cause0 | 0 | p_sig_regained | 0 |
| S:p_sync_regained | 0 | enc_out | |
| 0x0 | | | |
| S:cached_fps_status | 0 | cached_sts_status | 0 |
| S:cached_er_crc_good_eof | 0 | | |
| S:cached_er_bad_os | 0 | cached_er_too_long | 0 |
| S:cached_er_trunc | 0 | | |
| cached_tot_er_crc_good_eof | 0 | | |
| S:num_pt_excess_intr | 0 | num_no_fid | 0 |
| S:num_fault1_cnt | 0 | num_fault2_cnt | |
| 0 | | | |
| S:num_fault_lip | 0 | num_fault_lli | 0 |
| S:num_fault_rx_fifo | 0 | num_fault_hss | 0 |
| S:num_fault_bwait | 0 | lli_intr_prim | |
| 0 | | | |
| S:num_sw_link_to | 0 | | |
| be_link_err_mon_count | 0 | | |
| S:ecb_enc_enabled | 0 | ecb_comp_enabled | |
| 0 | | | |
| S:ecb_rsv_enc | 0 | ecb_rsv_comp | 0 |
| S:ecb_enc_bm | 0x0 | ecb_key_index | |
| 0xffffffff | | | |
| S:fab_idx | 0 | | |
| S:num_be_lto | 0 | lto_count_reset_intvl | |
| 0 | | | |
| S:lr_count_reset_intvl | 0 | num_be_lr | |
| 0 | | | |
| S:num_fault_qsfm | 0 | check_lto | |
| 0 | | | |
| S:credit_loaded | 0 | num_credit_overrun | |
| 0 | | | |
| S:fec_enabled | 0x0 | fec_los_to_flag | 0x0 |
| S:phy_stats_clear_ts | 1725611419 | pcs_err_online | |
| 0 | | | |
| S:pcs_err_light_det | 0 | pcs_err_ignore | |
| 0 | | | |
| S:pcs_blk_err | 0 | pcs_hiber | 0 |
| S:phy_port_status | 0 | ecb_enc_lr_count | |
| 0 | | | |
| S:dport_mode | 0 | avoid_lto_det | 0 |
| S:sn_debounced | 0x0 | sn_started_kr_reqd | 0 |
| S:major_timer_started | 0x0 | ready_bm | 0x0 |
| S:parln_1_bm | 0x0 | parln_0_bm | 0x0 |
| S:be_los_of_sync_event_intvl | | 0 | |
| be_los_of_sync_event | 0 | | |
| S:errataPtenable_cntr | 0 | errataPoll_cntr | |

```

      0
S:jda_rx_sig_loss_det          0          jda_rx_sig_loss_cnt
      0
S:encrypt_blk_error          0
S:
S:      c4_trunk
S:=====
S:mark_ts          0x0          deskew          0x0
S:master_phy      0x0
S:
S:adelay[00]: 0x00000000 0x00000000 0x00000000 0x00000000
S:adelay[04]: 0x00000000 0x00000000 0x00000000 0x00000000
S:
S:      c4_buf
S:=====
S:tx_csc          0          rx_csc
      0
S:ld_vc_credits    0          tx_flag          0x0
S:alloc_buffers    0          req_buffers    0
S:est_buffers      20         ld_use_est    0
S:bb_sc_n          0          rx_bb_sc_n
      0
S:data_cr          5          nondata_cr
      6
S:cr_enable        0
S:ld_nondata_cr    6          tnodep
0xbb83eb60
S:tx_credits[0] 0 0 0 0 0 0 0 0
S:tx_credits[8] 0 0 0 0 0 0 0 0
S:tx_credits[16] 0 0 0 0 0 0 0 0 0 0
S:tx_credits[24] 0 0 0 0 0 0 0 0 0 0
S:tx_credits[32] 0 0 0 0 0 0 0 0 0 0
S:rx_credits[0] 0 0 0 0 0 0 0 0
S:rx_credits[8] 0 0 0 0 0 0 0 0
S:rx_credits[16] 0 0 0 0 0 0 0 0 0 0
S:rx_credits[24] 0 0 0 0 0 0 0 0 0 0
S:rx_credits[32] 0 0 0 0 0 0 0 0 0 0
S:tx_mbc[0] 0 0 0 0 0 0 0 0
S:tx_mbc[8] 0 0 0 0 0 0 0 0
S:tx_mbc[16] 0 0 0 0 0 0 0 0
S:tx_mbc[24] 0 0 0 0 0 0 0 0
S:tx_mbc[32] 0 0 0 0 0 0 0 0
S:rx_mbc[0] 0 0 0 0 0 0 0 0
S:rx_mbc[8] 0 0 0 0 0 0 0 0
S:rx_mbc[16] 0 0 0 0 0 0 0 0
S:rx_mbc[24] 0 0 0 0 0 0 0 0
S:rx_mbc[32] 0 0 0 0 0 0 0 0
S:
S:C4 Chip Variables: c4_phy->c4_chp = 0x97e28000
S:-----
-----
S:version = 2.1
S:magic_id          0xc4234567          init_state          0x8
S:reset_reg_mem    0x1

```

| | | | |
|---------------------------|------------|-------------------------|-----------------------|
| S:ch_int0_en_bm | 0x0 | intr0_cause | 0x0 |
| S:ch_int1_en_bm | 0x0 | intr1_cause | 0x0 |
| S:ch_int2_en_bm | 0x0 | intr2_cause | 0x0 |
| S:ch | 0x43010080 | ch_cfg | |
| 0xb7013ba0 | | | |
| S:raslog_hndl.hndl | 0x0 | obj_halted | 0x0 |
| S:c4_chip_regp | 0x80000000 | c4_fpg_regp | |
| 0x81800000 | | | |
| S:num_chip_timer | 0x5 | | |
| S:hi_task_bm | 0x0 | lo_task_bm | 0x0 |
| S:c4_deferq.q_head | 0x0 | c4_deferq.q_tail | 0x0 |
| S:c4_tmrq.q_head | 0x0 | c4_tmrq.q_tail | 0x0 |
| slot_no | 0 | | |
| S:chip_inst | 0 | chip_idx | 0 |
| S:pll_initialized | 1 | | |
| pll_serdes_initialized | 1 | | |
| S:init_tries | 0 | init_ptEnableBM | |
| 0xba01b488 | | | |
| S:tick_polling | 0xb980c9c0 | sec_polling | |
| 0xb980c960 | | | |
| S:bb_fid | 129 | | |
| S:ecb_key_bm[0] | 0x0 | ecb_key_bm[1] | 0x0 |
| S:ecb_key_bm[2] | 0x0 | ecb_key_bm[3] | 0x0 |
| S:is_chip_enc_enabled | | 0 | |
| is_chip_comp_enabled | 0x0 | | |
| S:ftb_rsrcp->ftb_flags | 0x0 | act_rsrcp->act_flag | 0x1 |
| S:lue_rsrcp->lue_flags[0] | 0x0 | lue_rsrcp->lue_flags[1] | 0x0 |
| >lue_flags[1] | 0x0 | | |
| S:c4_phyp[00]: | 0xb6ab0000 | 0xb6ab2080 | 0xb6ab4100 0xb6ab6180 |
| S:c4_phyp[04]: | 0xb6ab9040 | 0xb6abb0c0 | 0xb6abd140 0xb6ac0000 |
| S:c4_phyp[08]: | 0xb6ac2080 | 0xb6ac4100 | 0xb6ac6180 0xb6ac9040 |
| S:c4_phyp[12]: | 0xb6acb0c0 | 0xb6acd140 | 0xb6ad0000 0xb6ad2080 |
| S:c4_phyp[16]: | 0xb6ad4100 | 0xb6ad6180 | 0xb6ad9040 0xb6adb0c0 |
| S:c4_phyp[20]: | 0xb6add140 | 0xb6ae0000 | 0xb6ae2080 0xb6ae4100 |
| S:c4_phyp[24]: | 0xb6ae6180 | 0xb6ae9040 | 0xb6aeb0c0 0xb6aed140 |
| S:c4_phyp[28]: | 0xb6af0000 | 0xb6af2080 | 0xb6af4100 0xb6af6180 |
| S:c4_phyp[32]: | 0xb6af9040 | 0xb6afb0c0 | 0xb6afd140 0xb6b00000 |
| S:c4_phyp[36]: | 0xb6b02080 | 0xb6b04100 | 0xb6b06180 0xb6b09040 |
| S:c4_phyp[40]: | 0xb6b0b0c0 | 0xb6b0d140 | 0xb6b10000 0xb6b12080 |
| S:c4_phyp[44]: | 0xb6b14100 | 0xb6b16180 | 0xb6b19040 0xb6b1b0c0 |
| S:c4_phyp[48]: | 0xb6b1d140 | 0xb6b20000 | 0xb6b22080 0xb6b24100 |
| S:c4_phyp[52]: | 0xb6b26180 | 0xb6b29040 | 0xb6b2b0c0 0xb6b2d140 |
| S:c4_phyp[56]: | 0xb6b30000 | 0xb6b32080 | 0xb6b34100 0xb6b36180 |
| S:c4_phyp[60]: | 0xb6b39040 | 0xb6b3b0c0 | 0xb6b3d140 0xb6b40000 |
| S:c4_lgcp[00]: | 0x97f48000 | 0x97f4c000 | 0x97f50000 0x97f54000 |
| S:c4_lgcp[04]: | 0x97f58000 | 0x97f5c000 | 0x97f60000 0x97f64000 |
| S:c4_lgcp[08]: | 0x97f68000 | 0x97f6c000 | 0x97f70000 0x97f74000 |
| S:c4_lgcp[12]: | 0x97f78000 | 0x97f7c000 | 0x97f80000 0x97f84000 |
| S:c4_lgcp[16]: | 0x97f88000 | 0x97f8c000 | 0x97f90000 0x97f94000 |
| S:c4_lgcp[20]: | 0x97f98000 | 0x97f9c000 | 0x97fa0000 0x97fa4000 |
| S:c4_lgcp[24]: | 0x97fa8000 | 0x97fac000 | 0x97fb0000 0x97fb4000 |
| S:c4_lgcp[28]: | 0x97fb8000 | 0x97fbc000 | 0x97fc0000 0x97fc4000 |
| S:c4_lgcp[32]: | 0x97fc8000 | 0x97fcc000 | 0x97fd0000 0x97fd4000 |
| S:c4_lgcp[36]: | 0x97fd8000 | 0x97fdc000 | 0x97fe0000 0x97fe4000 |

```

S:c4_lgcp[40]: 0x97fe8000 0x97fec000 0x97ff0000 0x97ff4000
S:c4_lgcp[44]: 0x97ff8000 0x97ffc000 0x8e000000 0x8e004000
S:c4_lgcp[48]: 0x8e008000 0x8e00c000 0x8e010000 0x8e014000
S:c4_lgcp[52]: 0x8e018000 0x8e01c000 0x8e020000 0x8e024000
S:c4_lgcp[56]: 0x8e028000 0x8e02c000 0x8e030000 0x8e034000
S:c4_lgcp[60]: 0x8e038000 0x8e03c000 0x8e040000 0x8e044000
S:chip_timers[00]: 0xb980c720 0xb980c780 0xb980c7e0 0xb980c840
S:chip_timers[04]: 0xb980c8a0 0xb980c900
S:disc_trap_enable_required      0x0          rxlp_disc_log_stop
      0x0
S:curr_rxlp_frm_cnt      0x0          curr_rxlp_disc_frm_cnt  0x0
S:sw_disc_frm_cnt      0x0          last_disc_frm_cnt      0x0
S:txq_nopop_pr_cnt      0x0          pollErrataDfe_ptBM
0xba01b4b0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][0]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][1]  0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][2]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][0]  0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][1]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][2]  0x0
S:
S:C4 Logical Port Variables
S:-----
-----
S:c4_lgc_regp      0x81c88000
S:c4_phyp:
S:      0xb6ad6180      0x0          0x0          0x0

S:      0x0          0x0          0x0          0x0

S:master_phyp      0xb6ad6180      if_id
0x43020011
S:min_phyp      0x0          max_phyp      0x0
S:num_phy_ports      1          lgc_num      17
S:num_iu_to      0          sw_txq_bm
0
S:port_fid      128          unused      0
S:port_group      2          lgc_stats_clear_ts
1725611419
S:domain_tbl_sel      0          area_tbl_sel
0
S:egid_tbl_sel      0
S:serv_lo_bm      0x0
S:
S:Proto Phy Variables:
S:-----
-----
S:magic_id      0xc4123456      asic_phyp
0xb6ad6180
S:port_id      0x43028011      phy_cfg
0xb6ad8000
S:upsm_hdl      0xb8015000      physm_hdl
0xb8014d20
S:ov_sns_hdl      0xb8014be0      sw_sns_hdl

```

```

0xb8014c80
S:ov_lksm_hdl          0xb8014dc0      sw_lksm_hdl
0xb8014e60
S:trksm_hdl           0xb8014f00      lr_flag          0x0
S:lr_active           0x0             qsfm_txxr_rate_sel
0x0
S:
S:UPSM      UP00: UPST_PORT_DISABLED    --> UP01:
UPST_START_PORT_INIT
S:SNSM(OV)  SN00: OV_SNST_STOPPED          --> SN00: OV_SNST_STOPPED
S:SNSM(SW)  SW00: SW_SNST_STAGE_WS      --> SW00: SW_SNST_STAGE_WS
S:PHYSM     UNKNOWN                    --> PP03: PHYST_NO_SIGNAL
S:LKSM(OV)  LK00: OV_LKST_INACTIVE       --> LK00: OV_LKST_INACTIVE
S:LKSM(SW)  SW13: INACTIVE              --> SW13: INACTIVE
S:TRKSM     TRK0: TRKST_INIT            --> TRK0: TRKST_INIT
S:
S:physm variables:
S:-----
-----
S:proto_phyp          0xb8809360      physm_hdl
0xb8014d20
S:force_offline      0             copper          0
S:fault_reason       0: UNKNOWN
S:phy_media_present  1
S:
S:sns variables:
S:-----
-----
S:speed              0xff          proto_phyp
0xb8809360
S:hw_sn_tries_left   0x0           sw_sn_tries_left  0x0
S:curr_txsp_count    0x0           curr_tx_indx
S:tx_max             0x0
0x0
S:curr_tx            0x0           curr_rxsp_count
0x0
S:rx_max             0x0           curr_rx_indx
0x0
S:curr_rx            0x0           rx_mem
0x0
S:rxsp_rec_count     0x0
S:nc_start           0x0           tx_start          0x0
S:sync_start         0x0           sync_present      0x0
S:diag_auto          0x0           diag_speed        0xff
S:striped_wd_tov     3000          hw_wd_tov
3000
S:step               0x0           qsfm28_speed_mode
0x0
S:qsfm_mode0_hw_sn_tries_left  0x0
S:qsfm_mode1_hw_sn_tries_left  0x0
S:
S:lksm variables:
S:-----
-----

```

```

S:proto_phyph          0xb8809360      ov_lksm_hdl
0xb8014dc0
sw_lksm_hdl           0xb8014e60
num_lf1               0
S:hw_link_tries_left  0                sw_link_tries_left    0
S:buf_ptype           0x0              stored_entry_state     0x6
S:handshake_owner     0x0              0x0                    mark_unsent
0x0
S:busybuf_stuck       0x0              lr_wait                0x0
S:
S:trksm variables:
S:-----

```

```

S:Not a trunk port
S:
S:upsm variables:
S:-----

```

```

S:proto_phyph          0xb8809360      upsm_hdl
0xb8015000
S:bb_credits           0                port_beacon            0
S:port_diag_flag      0                0                      force_offline
0
S:port_fault_rsn      0: PORT_NO_FAULT
S:retry_init_rsn      0: UNKNOWN
S:linit_reason         0                linit_result           0
S:ie_fctl_mode         0                fec_in_sync_tries_left 0
S:retry_sn_fail_init  0
retry_link_fail_init  0
S:excess_lr_count     0
S:
S:c4_ch_cfg
S:-----

```

```

S:c4_desc_ring_size   256      292      256      256      292
292      2      292      292
S:thresh_def          0         16        1         0
S:intr_tries          500              cmem_pattern
0xdeadbeef
S:cmem_pattern_upwd   2                cmem_init_time        16
S:cmem_init_tries     5
S:ctrl_par_thresh     2                data_par_thresh
4
S:cam_par_thresh      4                buf_loss_thresh
12
S:crit_par_thresh     2                non_crit_par_thresh
6
S:pci_abort_thresh    10              pci_err_thresh         5
S:excess_chintr_thresh 8                sw_err_thresh          20
S:err_sample_period   300             intr_sleep
20000
S:frame_timeout       2500             proxy_dev              16384
S:vf_route            81920            qos                    2048
S:stats 2048          f_redirect       2048

```

```

S:rsp_trap          2048          lun_zoning          20480
S:area_mode        0          ftb_max_loop[0]    0
S:ftb_max_loop[1]  6          ftb_max_loop[2]    9
S:ftb_max_loop[3]  10         ftb_max_loop[4]    10
S:ftb_max_loop[5]  5          ftb_max_loop[6]    6
S:ftb_seg_size[0]  0          ftb_seg_size[1]
16384
S:ftb_seg_size[2]  65536       ftb_seg_size[3]
16384
S:ftb_seg_size[4]  16384       ftb_seg_size[5]
65536
S:ftb_seg_size[6]  16384       ftb_seg_base[0]    0
S:ftb_seg_base[1]  0          ftb_seg_base[2]
65536
S:ftb_seg_base[3]  16384       ftb_seg_base[4]
32768
S:ftb_seg_base[5]  131072      ftb_seg_base[6]
49152
asic_err_monitor_period1  300
asic_err_monitor_period2  86400
zone_chk_to_poll_period  25
zone_chk_class2_reject_tov  220
S:
S:c4_phy_cfg
S:-----
-----
S:version = 2.1
S:pt                0x43028011      fab_ptr
0x9a800000
S:fabattr           0x9a8000d4      fab_iop
0x9a800050
S:cfgbm            0xbb83e8c4      port_ctrl
0xb6ad8018
S:pcap.pcap_bm     0x8d215547      pcap.pcap2_bm
0x588289
S:pcap.pcap3_bm    0x1bebe0c
ui_idx             43          S:slot_no
0
is_icl             0          S:sw_usr_ports     400
S:neg_speed        0 0 0 0 0 0
S:my_domain        0x1          port_mode           0x0
S:hw_sn_maxtries   100         sw_sn_maxtries
0
S:hw_link_maxtries 10          sw_link_maxtries   5
S:rx_cyc_tov       28          rttov              300
S:bufrdy_tov       300         busybuf_tov        286
S:mark_tov         300         lksm_tov           3000
S:buf_dealloc_wait 4          hw_wd_tov          3000
S:hw_lk_train_tov  540        hw_lk_test_tov
150
S:syswait_tx_12_lips 1          lip_rx_tov         55
S:al_time_tov      15         lp_tov             2000
S:intr_tries_port  500        intr_mod_debounce
250

```

```

S:intr_lsrflt_debounce 500          intr_efifo_debounce 100
S:port_no_fid          3            excess_ptintr_thresh 8
S:port_fault1_thresh  100          port_fault1_spur_thresh 250
S:port_fault1_disc_thresh      500
port_fault1_disc_spur_thresh 1000
S:port_fault2_thresh  5            losync_tov          100
S:port_sw_link_to     15            en_8g_scramble
  1
frc_hw_sn_mode        0x1
S:enc_poll_thresh     0            fec_enable
  0
S:fec_in_sync_to      50            fec_in_sync_try_max
  4
S:port_be_lto_threshold      100    port_be_lr_threshold
  2
S:be_cr_in_sync_to     5
port_credit_overrun_thresh      10
S:jda_sfp_losig_tov    400
jda_sfp_losig_try_max    30
S:striped_wd_tov      3000
no_sync_debounce        1200
S:
S:      fab_iop
S:=====
S:fab_iop->interop_mode 0x0          fab_iop->lab_mode      0x0
S:fab_iop->fl_bbc        0x0          fab_iop->fl_fan
  0x0
S:fab_iop->fl_cls        0x4          fab_iop->fl_rscn
  0x0
S:fab_iop->domain_id_offset 0x60    fab_iop-
>mcdt_fabric_mode      0x0
S:fab_iop->mcdt_default_zone 0x0          fab_iop-
>mcdt_safe_zone        0x0
S:
S:      port_ctrl
S:=====
S:port_ctrl.port_type  1            port_ctrl.port_grp    2
S:port_ctrl.port_number 43          port_ctrl.vc_mode      1
S:
S:      port_ctrl.lcap
S:=====
S:has_serdes           0            has_media              1
S:topology             1            skip_nego              0
S:skip_pnego           0            skip_init_event        0
S:en_shim              0            speed_neg
  1
S:loop_back            0            num_speeds             5
S:fec_enable           0
S:
S:      port_ctrl.speed_list array
S:=====
S:speed_list[0].auto_neg 1      speed_list[0].lnk_speed 0x0000000a
S:speed_list[1].auto_neg 1      speed_list[1].lnk_speed 0x00000008
S:speed_list[2].auto_neg 0      speed_list[2].lnk_speed 0x00000006

```


S:speed_list[3].auto_neg 1 speed_list[3].lnk_speed 0x00000005
S:speed_list[4].auto_neg 0 speed_list[4].lnk_speed 0x00000003
S:speed_list[5].auto_neg 0 speed_list[5].lnk_speed 0x00000000

S:

S: port_ctrl.cm

S:=====

S:port_ctrl.cm.num_vcs 8
S:port_ctrl.cm.min_bufs 8
S:port_ctrl.cm.cr_shar_bufs 0
S:port_ctrl.vc_alloc
S:port_ctrl.vc_alloc 2 0 1 1 1 1 1 1
S:port_ctrl.vc_alloc 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.norm_vc_alloc
S:port_ctrl.norm_vc_alloc 4 0 5 5 5 5 1 1
S:port_ctrl.norm_vc_alloc 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.cm.skip_bb_credit 0
S:port_ctrl.cm.use_shim_based_sublist 0

S:

S: port_ctrl.serdes_set

S:=====

S:serdes_type 0x8
S:serdes_data_t.ibm_hss_serdes.tx_drive_power 0x1
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b_sign 0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b 0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_a 0x0
S:serdes_data_t.ibm_hss_serdes.rxeq 0x0

S:

S: cfgbm

S:=====

S:old_distance 0x0 gport_lockdown 0x0
S:tport 0x1 speed 0x0
S:disable_eport 0x0 fcacc 0x0
S:lport_lockdown 0x0 priv_lport_lockdown
0x0
S:vcxlt_linit 0x0 delay_flogi 0x0
S:isl_interop 0x0 distance 0x0
S:BufStarvFlag 0x0 credit_sharing 0x0
S:lport_halfduplex 0x0 lport_fairness 0x0
S:soft_neg 0x0 asn_frc_hwretry 0x0
S:cr_recov 0x0 fport_buffers 0x0
S:export 0x0 export_mode
0x0
S:csctl_en 0x0 mirror_port 0x0
S:fault_delay 0x0 non_dfe 0x0
S:fec_configured*(0=ENAB) 0 fec_tts
0

S:port_persistently_disabled (permanently) 0 (0)

S:

S: cfg property

S:=====

S:priv_pcfg_bm 0x00000000 lgcl_pcfg_bm
0xbb83e904

```

S: fport_buffer          0x00000000
S:
S:
S: C4 Discard Cntrs: rxlp_stats = 0xb6ad6530
S:-----
-----
S: disc_mcast_wka        0x0          disc_inv_did            0x0
S: disc_cl1_cl4          0x0          disc_sid_chk_fail      0x0
S: disc_inv_dom_egid_txpt 0x0          disc_vft_hop_cnt_1
  0x0
S: disc_classf           0x0          disc_fcp_cdb_inv       0x0
S: disc_vfid_trap_enabled 0x0
disc_vfid_hdr_chk_fail 0x0
S: disc_shim_cksum_fail  0x0          disc_fed_edit_cmd_err  0x0
S: disc_shim_cksum_fail  0x0          disc_fed_edit_cmd_err  0x0
S: disc_ftb_vm_mode      0x0          disc_ftb_agnt2_miss    0x0
S: disc_ecb_de_pad_err   0x0          disc_ecb_de_tag_err    0x0
S: disc_ecb_de_seq_err   0x0          disc_ecb_err            0x0
S: disc_ftb_type4_match  0x0          disc_fcp_rsp_ftb_type4 0x0
S: disc_fcp_rsp_ftb_type4 0x0          disc_ftb_type5_match
  0x0
S: disc_ftb_type3_match  0x0          disc_els_ftb_type3     0x0
S: disc_ftb_type1_match  0x0          disc_els_rsp_ex_port   0x0
S: disc_inv_drp_dps      0x0          disc_did_lookup_miss   0x0
S: disc_ftb_type2_match  0x0          disc_trpd_plogi_pdisc  0x0
S: disc_type2_lookup_miss 0x0          disc_ftb_type6_match
  0x0
S: disc_els_rep_ex_port  0x0          disc_els_sid_lkup_bit1 0x0
S: disc_els_sid_lkup_bit0 0x0
disc_bls_frm_trap_bit1 0x0
S: disc_ftb_token_err    0x0          disc_asic_internal_err 0x0
S: disc_hard_zone_miss   0x0          disc_lun_zone_miss     0x0
S: discflt_frame_disc    0x0          discflt_parity_err     0x0
S: disc_frame_marked_du  0x0          disc_frame_marked_to   0x0
E: Connection type: FE
E: Port type: F_port
E: Trunk port: No
E: Configured Speed: AUTO_SPEED_NEGO
E: Max Capable Speed: 32G
E: Current SNSM Speed: UNDEFINED
E: Hardware TX Speed: 32G (0x00000004)
E: Hardware RX Speed: 32G (0x00000040)
E:
E: Interrupts: 0          Link_failure: 0
Loss_of_sync: 0          Loss_of_sig: 0
E: Lli: 0                Invalid_word: 0
E: trapped_frm: 0        fwd_status_ok: 0
E: fwd_timeout: 0        fwd_tx_unavail: 0
E: fwd_unroutable: 0     fwd_zone_out: 0
E: fwd_other_err: 0     frm_err_discard: 0
E: Fltr listA: 0         Fltr listB: 0
E: Zone trap fwd: 0     Zone trap disc: 0
E: shim_csum: 0          RTE_perr: 0
E: Invalid_crc: 0        Delim_err: 0

```

E:Protocol_err: 0
E:Lr_in: 0 Lr_out: 0
E:Ols_in: 0 Ols_out: 0

filterportshow 43

FILTER DATA

Shadow settings:

Filter Enable: 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass: 0x00000000

Real settings:

Enable RAM: 0x00000000, 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000

Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass RAM: 0x00000000

Shadowed filters:

Filter 0: Not Installed (MIRROR1)(LISTA)
c4_fldenable[0] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[0] = 0x00000000,c4_fltr_config[0] = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
c4_fldenable[1] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[1] = 0x00000000,c4_fltr_config[1] = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
c4_fldenable[2] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[2] = 0x00000000,c4_fltr_config[2] = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
c4_fldenable[3] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[3] = 0x00000000,c4_fltr_config[3] = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
c4_fldenable[4] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[4] = 0x00000000,c4_fltr_config[4] = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
c4_fldenable[5] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[5] = 0x00000000,c4_fltr_config[5] = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
c4_fldenable[6] = 0x00000000 0x00000000 0x00000000

```
0x00000000
    c4_fldnegate[6] = 0x00000000,c4_fltr_config[6] = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
    c4_fldenable[7] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[7] = 0x00000000,c4_fltr_config[7] = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
    c4_fldenable[8] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[8] = 0x00000000,c4_fltr_config[8] = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
    c4_fldenable[9] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[9] = 0x00000000,c4_fltr_config[9] = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
    c4_fldenable[10] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[10] = 0x00000000,c4_fltr_config[10] =
0x00000000
Filter 11: Not Installed (SIM)(LISTA)
    c4_fldenable[11] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[11] = 0x00000000,c4_fltr_config[11] =
0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
    c4_fldenable[12] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[12] = 0x00000000,c4_fltr_config[12] =
0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
    c4_fldenable[13] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[13] = 0x00000000,c4_fltr_config[13] =
0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
    c4_fldenable[14] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[14] = 0x00000000,c4_fltr_config[14] =
0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
    c4_fldenable[15] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[15] = 0x00000000,c4_fltr_config[15] =
0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
    c4_fldenable[16] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[16] = 0x00000000,c4_fltr_config[16] =
0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
    c4_fldenable[17] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[17] = 0x00000000,c4_fltr_config[17] =
0x00000000
```

Filter 18: Not Installed (PERF3)(LISTA)
c4_fldenable[18] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[18] = 0x00000000,c4_fltr_config[18] =
0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
c4_fldenable[19] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[19] = 0x00000000,c4_fltr_config[19] =
0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
c4_fldenable[20] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[20] = 0x00000000,c4_fltr_config[20] =
0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
c4_fldenable[21] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[21] = 0x00000000,c4_fltr_config[21] =
0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
c4_fldenable[22] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[22] = 0x00000000,c4_fltr_config[22] =
0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
c4_fldenable[23] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[23] = 0x00000000,c4_fltr_config[23] =
0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
c4_fldenable[24] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[24] = 0x00000000,c4_fltr_config[24] =
0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
c4_fldenable[25] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[25] = 0x00000000,c4_fltr_config[25] =
0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
c4_fldenable[26] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[26] = 0x00000000,c4_fltr_config[26] =
0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
c4_fldenable[27] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[27] = 0x00000000,c4_fltr_config[27] =
0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
c4_fldenable[28] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[28] = 0x00000000,c4_fltr_config[28] =

```
0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
    c4_fldenable[29] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[29] = 0x00000000,c4_fltr_config[29] =
0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    c4_fldenable[30] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[30] = 0x00000000,c4_fltr_config[30] =
0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    c4_fldenable[31] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[31] = 0x00000000,c4_fltr_config[31] =
0x00000000
```

Real filters:

```
Filter 0: Not Installed (MIRROR1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
```

0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 11: Not Installed (SIM)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000


```

Filter 22: Not Installed (PERF7)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000

```

```

Filter dirty indicator: 0x00000000
Performance filters: 0
Port Mirror filters: 0 (0x0)

```

FIELD DATA

Shadowed fields:

```

fldoffset[0] = 0x00, fldmask[0] = 0x00, fldvalue_dyna[0]: 0x00 0x00
0x00 0x00
fldcontrol[0].inuse = 0x0  fldcontrol[0].refcnt = 0x00 0x00 0x00

```

```
0x00
fldoffset[1] = 0x00, fldmask[1] = 0x00, fldvalue_dyna[1]:0x00 0x00
0x00 0x00
fldcontrol[1].inuse = 0x0  fldcontrol[1].refcnt = 0x00 0x00 0x00
0x00
fldoffset[2] = 0x00, fldmask[2] = 0x00, fldvalue_dyna[2]:0x00 0x00
0x00 0x00
fldcontrol[2].inuse = 0x0  fldcontrol[2].refcnt = 0x00 0x00 0x00
0x00
fldoffset[3] = 0x00, fldmask[3] = 0x00, fldvalue_dyna[3]:0x00 0x00
0x00 0x00
fldcontrol[3].inuse = 0x0  fldcontrol[3].refcnt = 0x00 0x00 0x00
0x00
fldoffset[4] = 0x00, fldmask[4] = 0x00, fldvalue_dyna[4]:0x00 0x00
0x00 0x00
fldcontrol[4].inuse = 0x0  fldcontrol[4].refcnt = 0x00 0x00 0x00
0x00
fldoffset[5] = 0x00, fldmask[5] = 0x00, fldvalue_dyna[5]:0x00 0x00
0x00 0x00
fldcontrol[5].inuse = 0x0  fldcontrol[5].refcnt = 0x00 0x00 0x00
0x00
fldoffset[6] = 0x00, fldmask[6] = 0x00, fldvalue_dyna[6]:0x00 0x00
0x00 0x00
fldcontrol[6].inuse = 0x0  fldcontrol[6].refcnt = 0x00 0x00 0x00
0x00
fldoffset[7] = 0x00, fldmask[7] = 0x00, fldvalue_dyna[7]:0x00 0x00
0x00 0x00
fldcontrol[7].inuse = 0x0  fldcontrol[7].refcnt = 0x00 0x00 0x00
0x00
fldoffset[8] = 0x00, fldmask[8] = 0x00, fldvalue_dyna[8]:0x00 0x00
0x00 0x00
fldcontrol[8].inuse = 0x0  fldcontrol[8].refcnt = 0x00 0x00 0x00
0x00
fldoffset[9] = 0x00, fldmask[9] = 0x00, fldvalue_dyna[9]:0x00 0x00
0x00 0x00
fldcontrol[9].inuse = 0x0  fldcontrol[9].refcnt = 0x00 0x00 0x00
0x00
fldoffset[10] = 0x00, fldmask[10] = 0x00, fldvalue_dyna[10]:0x00 0x00
0x00 0x00
fldcontrol[10].inuse = 0x0  fldcontrol[10].refcnt = 0x00 0x00 0x00
0x00
fldoffset[11] = 0x00, fldmask[11] = 0x00, fldvalue_dyna[11]:0x00 0x00
0x00 0x00
fldcontrol[11].inuse = 0x0  fldcontrol[11].refcnt = 0x00 0x00 0x00
0x00
fldoffset[12] = 0x00, fldmask[12] = 0x00, fldvalue_dyna[12]:0x00 0x00
0x00 0x00
fldcontrol[12].inuse = 0x0  fldcontrol[12].refcnt = 0x00 0x00 0x00
0x00
fldoffset[13] = 0x00, fldmask[13] = 0x00, fldvalue_dyna[13]:0x00 0x00
0x00 0x00
fldcontrol[13].inuse = 0x0  fldcontrol[13].refcnt = 0x00 0x00 0x00
0x00
fldoffset[14] = 0x00, fldmask[14] = 0x00, fldvalue_dyna[14]:0x00 0x00
```

```
0x00 0x00
fldcontrol[14].inuse = 0x0 fldcontrol[14].refcnt = 0x00 0x00 0x00
0x00
fldoffset[15] = 0x00,fldmask[15] = 0x00,fldvalue_dyna[15]:0x00 0x00
0x00 0x00
fldcontrol[15].inuse = 0x0 fldcontrol[15].refcnt = 0x00 0x00 0x00
0x00
fldoffset[16] = 0x00,fldmask[16] = 0x00,fldvalue_dyna[16]:0x00 0x00
0x00 0x00
fldcontrol[16].inuse = 0x0 fldcontrol[16].refcnt = 0x00 0x00 0x00
0x00
fldoffset[17] = 0x00,fldmask[17] = 0x00,fldvalue_dyna[17]:0x00 0x00
0x00 0x00
fldcontrol[17].inuse = 0x0 fldcontrol[17].refcnt = 0x00 0x00 0x00
0x00
fldoffset[18] = 0x00,fldmask[18] = 0x00,fldvalue_dyna[18]:0x00 0x00
0x00 0x00
fldcontrol[18].inuse = 0x0 fldcontrol[18].refcnt = 0x00 0x00 0x00
0x00
fldoffset[19] = 0x00,fldmask[19] = 0x00,fldvalue_dyna[19]:0x00 0x00
0x00 0x00
fldcontrol[19].inuse = 0x0 fldcontrol[19].refcnt = 0x00 0x00 0x00
0x00
```

Real fields:

```
fldoffset RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000
```

```
fldmask RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000
```

fld value4 RAM:

```
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
```

```
Field dirty indicator: 0x00000000
```

```
FDB reference count fdb: 0 [0 0 0 0 ]
```

FDB reference count fdb: 1 [0 0 0 0]
FDB reference count fdb: 2 [0 0 0 0]
FDB reference count fdb: 3 [0 0 0 0]
FDB reference count fdb: 4 [0 0 0 0]
FDB reference count fdb: 5 [0 0 0 0]
FDB reference count fdb: 6 [0 0 0 0]
FDB reference count fdb: 7 [0 0 0 0]
FDB reference count fdb: 8 [0 0 0 0]
FDB reference count fdb: 9 [0 0 0 0]
FDB reference count fdb: 10 [0 0 0 0]
FDB reference count fdb: 11 [0 0 0 0]
FDB reference count fdb: 12 [0 0 0 0]
FDB reference count fdb: 13 [0 0 0 0]
FDB reference count fdb: 14 [0 0 0 0]
FDB reference count fdb: 15 [0 0 0 0]
FDB reference count fdb: 16 [0 0 0 0]
FDB reference count fdb: 17 [0 0 0 0]
FDB reference count fdb: 18 [0 0 0 0]
FDB reference count fdb: 19 [0 0 0 0]

Filter counters:

Filter counter 0: 0 (MIRROR1)
Filter counter 1: 0 (MIRROR2)
Filter counter 2: 0 (MIRROR3)
Filter counter 3: 0 (MIRROR4)
Filter counter 4: 0 (AEPORT_NON_MIRR_DROP)
Filter counter 5: 0 (ZONING TRAP)
Filter counter 6: 0 (FCR_EXPORT_DC)
Filter counter 7: 0 (TIN TRAP)
Filter counter 8: 0 (FICON CUP)
Filter counter 9: 0 (FICON CUP DST)
Filter counter 10: 0 (WELL KNOWN ADDR)
Filter counter 11: 0 (SIM)
Filter counter 12: 0 (UNUSED)
Filter counter 13: 0 (UNUSED)
Filter counter 14: 0 (UNUSED)
Filter counter 15: 0 (UNUSED)
Filter counter 16: 0 (PERF1)
Filter counter 17: 0 (PERF2)
Filter counter 18: 0 (PERF3)
Filter counter 19: 0 (PERF4)
Filter counter 20: 0 (PERF5)
Filter counter 21: 0 (PERF6)
Filter counter 22: 0 (PERF7)
Filter counter 23: 0 (PERF8)
Filter counter 24: 0 (PERF9)
Filter counter 25: 0 (PERF10)
Filter counter 26: 0 (PERF11)
Filter counter 27: 0 (PERF12)
Filter counter 28: 0 (OPM1)
Filter counter 29: 0 (OPM2)
Filter counter 30: 0 (IPM1)
Filter counter 31: 0 (IPM2)

ACL DATA

Logical port 17: Hard Zoning disabled, Soft Zoning disabled
Zone type: WWN Zoning
Frames with hard zone miss: 0

*** Please use filterportshow on user port 56 to display ACL hash tables and Mirroring resources of thischip.
***We show this data only for the first physical port which is an external port.

portFcPortCmdShow --slot 0 44 3
doing portFcPortCmdShow: arg1 = 3, arg2 = -2

portshow 44
portDisableReason: None
portCFlags: 0x1
portFlags: 0x1 PRESENT U_PORT
LocalSwcFlags: 0x0
portType: 26.0
POD Port: Port is licensed
portState: 2 Offline
Protocol: FC
portPhys: 4 No_Light portScn: 2 Offline
port generation number: 0
state transition count: 1

portId: 012c00
portIfId: 43020017
portWwn: 20:2c:d8:1f:cc:2c:99:90
portWwn of device(s) connected:
16b Area list:
Distance: normal
portSpeed: N32Gbps

FEC: Inactive
Credit Recovery: Inactive
LE domain: 0
Peer beacon: Off
FC Fastwrite: OFF

| | | | | |
|-------------|---|---------------|---|-------|
| Interrupts: | 0 | Link_failure: | 0 | Frjt: |
| 0 | | | | |
| Unknown: | 0 | Loss_of_sync: | 0 | Fbsy: |
| 0 | | | | |
| Lli: | 0 | Loss_of_sig: | 0 | |
| Proc_rqrd: | 0 | Protocol_err: | 0 | |
| Timed_out: | 0 | Invalid_word: | 0 | |
| Tx_unavail: | 0 | Invalid_crc: | 0 | |
| Delim_err: | 0 | Address_err: | 0 | |
| Lr_in: | 0 | Ols_in: | 0 | |
| Lr_out: | 0 | Ols_out: | 0 | |

portloginshow 44

```
Type PID World Wide Name credit df_sz cos
=====
```

```
portloginshow 44 -history
```

```
Type PID World Wide Name logout time
=====
```

```
portregshow 44
```

```
LED registers
```

```
=====
0x81cba000: c4_led_status 00000000 0x81cba004:
c4_led_ctl 00000000
```

```
FPL registers
```

```
=====
0x81cb8200: fpl_port_config 23298002
0x81cb820c: fpl_port_id_ctl 00000000 0x81cb8210:
fpl_port_id_addr 00012c00
0x81cb8214: fpl_port_speed 00000004 0x81cb821c:
fpl_lli_ctl 00000100
0x81cb8228: fpl_lli_os_ctl bc94ffff 0x81cb822c:
fpl_lli_send_word bc95b5b5
0x81cb8230: fpl_lli_mark_rx 00000000 0x81cb8234:
fpl_lli_rnd_trip_time 00000000
0x81cb8238: fpl_lli_ns_status 00130007 0x81cb823c:
fpl_lli_intr_status 00030007
0x81cb8244: fpl_lli_def 00100000 0x81cb8254:
fpl_lli_intr_enable_clr 001c0000
0x81cb8258: fpl_err_intr_status 00000000 0x81cb8260:
fpl_err_intr_enable_clr 00000000
0x81cb8268: fpl_err_first_error 00000000 0x81cb826c:
fpl_speed_neg_ctl 00000000
0x81cb8270: fpl_speed_neg_stat 00000000 0x81cb8274:
fpl_softasn_ctl 0000000f
0x81cb8278: fpl_link_init_ctl 00000000 0x81cb827c:
fpl_link_init_stat 00000000
0x81cb8280: fpl_aec_ctl 001c1060 0x81cb8284:
fpl_aec_ctl2 04009f60
0x81cb8288: fpl_pcs_ctl 00000170 0x81cb828c:
fpl_fec_ctl 00000424
0x81cb8290: fpl_fec_cor 00000000 0x81cb8294:
fpl_fec_uncor 00000000
0x81cb8298: fpl_hss_link_ctl 0031f040 0x81cb829c:
fpl_afifo_link_ctl 00000a86
0x81cb82a0: fpl_echo_lb_ctl 0000028c 0x81cb82a4:
fpl_scratch 00000121
0x81cb82a8: fpl_debug 00060005 0x81cb82ac:
fpl_misc_debug 00000800
0x00000000: SW_shadow_reg 00000000 0x00000000:
SW_c4_phyp->cfgptr 00030003
```

per-fpg (per octet) registers

=====

| | | | |
|-------------|-------------------------|----------|-------------|
| 0x8181382c: | fpg_serdes_ctla0 | 81a37be7 | 0x81813830: |
| | fpg_serdes_ctla1 | 81a37be7 | |
| 0x81813834: | fpg_serdes_ctlb0 | 81a1c3c3 | 0x81813838: |
| | fpg_serdes_ctlb1 | 81a1c3c3 | |
| 0x8181383c: | fpg_serdes_xgmii_1ms | 00067c28 | 0x81813840: |
| | fpg_serdes_regtimctl | 40e47946 | |
| 0x81813844: | fpg_serdes_asnrsttimctl | 00000102 | |

HSS PLL registers

=====

| | | | |
|-------------|----------------------------|----------|-------------|
| 0x81813400: | 00_hssplla_vco_coarse_cal0 | 00000000 | 0x81813404: |
| | 01_hssplla_vco_coarse_cal1 | 00000014 | |
| 0x81813408: | 02_hssplla_vco_coarse_cal2 | 00000000 | 0x8181340c: |
| | 03_hssplla_vco_coarse_cal3 | 00000000 | |
| 0x81813410: | 04_hssplla_vco_coarse_cal4 | 00000000 | 0x81813424: |
| | 09_hssplla_power_ctl | 00000000 | |
| 0x81813428: | 0A_hssplla_charge_pump_ctl | 00000004 | 0x81813438: |
| | 0E_hssplla_pll_misc_ctl | 00000000 | |
| 0x8181343c: | 0F_hssplla_pclk_ctl | 000000f8 | 0x81813440: |
| | 10_hssplla_eyem_intv_ctl | 00000000 | |
| 0x81813444: | 11_hssplla_eyem_intv_lim1 | 00000000 | 0x81813448: |
| | 12_hssplla_eyem_intv_lim2 | 00000000 | |
| 0x8181344c: | 13_hssplla_eyem_intv_lim3 | 00000000 | 0x81813450: |
| | 14_hssplla_eyem_intv_lim4 | 00000000 | |
| 0x818134f0: | 3C_hssplla_macro_tst_ctl4 | 00000000 | 0x818134f4: |
| | 3D_hssplla_macro_tst_ctl3 | 00000000 | |
| 0x818134f8: | 3E_hssplla_macro_tst_ctl2 | 00000000 | 0x818134fc: |
| | 3F_hssplla_macro_tst_ctl1 | 00000000 | |
| 0x81813500: | 00_hsspllb_vco_coarse_cal0 | 0000000a | 0x81813504: |
| | 01_hsspllb_vco_coarse_cal1 | 00000014 | |
| 0x81813508: | 02_hsspllb_vco_coarse_cal2 | 00000000 | 0x8181350c: |
| | 03_hsspllb_vco_coarse_cal3 | 00000000 | |
| 0x81813510: | 04_hsspllb_vco_coarse_cal4 | 00000000 | 0x81813524: |
| | 09_hsspllb_power_ctl | 00000000 | |
| 0x81813528: | 0A_hsspllb_charge_pump_ctl | 00000004 | 0x81813538: |
| | 0E_hsspllb_pll_misc_ctl | 00000000 | |
| 0x8181353c: | 0F_hsspllb_pclk_ctl | 000000f8 | 0x81813540: |
| | 10_hsspllb_eyem_intv_ctl | 00000000 | |
| 0x81813544: | 11_hsspllb_eyem_intv_lim1 | 00000000 | 0x81813548: |
| | 12_hsspllb_eyem_intv_lim2 | 00000000 | |
| 0x8181354c: | 13_hsspllb_eyem_intv_lim3 | 00000000 | 0x81813550: |
| | 14_hsspllb_eyem_intv_lim4 | 00000000 | |
| 0x818135f0: | 3C_hsspllb_macro_tst_ctl4 | 00000000 | 0x818135f4: |
| | 3D_hsspllb_macro_tst_ctl3 | 00000000 | |
| 0x818135f8: | 3E_hsspllb_macro_tst_ctl2 | 00000000 | 0x818135fc: |
| | 3F_hsspllb_macro_tst_ctl1 | 00000000 | |

HSS TX registers

=====

| | | | |
|-------------|------------------------|----------|-------------|
| 0x81812500: | 00_hsstx_cfg_mode_PHY | 00009f48 | 0x81812504: |
| | 01_hsstx_test_ctl | 00000000 | |
| 0x81812508: | 02_hsstx_coeff_ctl_INV | 00000000 | 0x8181250c: |

| | | | |
|---|----------|-------------|--|
| 03_hsstx_drv_mode_ctl | 00000000 | | |
| 0x81812510: 04_hsstx_drv_ovrd_ctl | 00000010 | 0x81812514: | |
| 05_hsstx_dclk_align_ovrd | 00000080 | | |
| 0x81812518: 06_hsstx_imp_cal_ovrd | 00000c0c | 0x8181251c: | |
| 07_hsstx_dclk_drift_tol | 00000004 | | |
| 0x81812520: 08_hsstx_tap0_coeff_TUNE | 00000000 | 0x81812524: | |
| 09_hsstx_tap1_coeff_TUNE | 00000003 | | |
| 0x81812528: 0A_hsstx_tap2_coeff_TUNE | 00000019 | 0x8181252c: | |
| 0B_hsstx_tap3_coeff_TUNE | 00000003 | | |
| 0x81812534: 0D_hsstx_pol_INV | 00000004 | 0x81812538: | |
| 0E_hsstx_ae_cmd | 00000000 | | |
| 0x8181253c: 0F_hsstx_ae_stat | 00000000 | 0x81812540: | |
| 10_hsstx_ae_tap0_TUNE | 00000000 | | |
| 0x81812544: 11_hsstx_ae_tap1_TUNE | 00000000 | 0x81812548: | |
| 12_hsstx_ae_tap2_TUNE | 00000028 | | |
| 0x8181254c: 13_hsstx_ae_tap3_TUNE | 00000000 | 0x81812554: | |
| 15_hsstx_app_tune | 0000120e | | |
| 0x81812558: 16_hsstx_analog_diag | 00000000 | 0x81812560: | |
| 18_hsstx_4x_seg_app | 0000aa00 | | |
| 0x81812564: 19_hsstx_2x_seg_app | 000000aa | 0x81812568: | |
| 1A_hsstx_1x_seg_app | 0000f5e4 | | |
| 0x8181256c: 1B_hsstx_seg_4x_term_app | 0000000f | 0x81812570: | |
| 1C_hsstx_seg_2x1x_term_app | 00000001 | | |
| 0x81812574: 1D_hsstx_tap_sign_app | 00000004 | 0x81812578: | |
| 1E_hsstx_ext_addr_data | 00000001 | | |
| 0x8181257c: 1F_hsstx_ext_addr_addr | 00000000 | 0x81812580: | |
| 20_hsstx_pat_buf_bytes_1_0 | 00000000 | | |
| 0x81812584: 21_hsstx_pat_buf_bytes_3_2 | 00000000 | 0x81812588: | |
| 22_hsstx_pat_buf_bytes_5_4 | 00000000 | | |
| 0x8181258c: 23_hsstx_pat_buf_bytes_7_6 | 00000000 | 0x8181259c: | |
| 27_hsstx_8023az_ctl | 00000000 | | |
| 0x818125a0: 28_hsstx_dcc_ctl | 000060c0 | 0x818125a4: | |
| 29_hsstx_dcc_ovrd | 00001000 | | |
| 0x818125a8: 2A_hsstx_dcc_app | 00000105 | 0x818125ac: | |
| 2B_hsstx_dcc_timeout | 0000ffff | | |
| 0x818125c0: 30_hsstx_tap_sign_ovrd | 00000000 | 0x818125c8: | |
| 32_hsstx_seg_4x_ovrd | 00000000 | | |
| 0x818125cc: 33_hsstx_seg_2x_ovrd | 00000000 | 0x818125d0: | |
| 34_hsstx_seg_1x_ovrd | 00000000 | | |
| 0x818125d8: 36_hsstx_tap_seg_4x_term_ovrd | 00000000 | 0x818125dc: | |
| 37_hsstx_tap_seg_2x_term_ovrd | 00000000 | | |
| 0x818125e0: 38_hsstx_tap_seg_1x_term_ovrd | 00000000 | 0x818125ec: | |
| 3B_hsstx_mac_test_ctl5 | 00000000 | | |
| 0x818125f0: 3C_hsstx_mac_test_ctl4 | 00000000 | 0x818125f4: | |
| 3D_hsstx_mac_test_ctl3 | 00000000 | | |
| 0x818125f8: 3E_hsstx_mac_test_ctl2 | 00000000 | 0x818125fc: | |
| 3F_hsstx_mac_test_ctl1 | 000000c6 | | |

HSS RX registers

=====

| | | | |
|-----------------------------------|----------|-------------|--|
| 0x81812700: 00_hssrx_cfg_mode_PHY | 00009e78 | 0x81812704: | |
| 01_hssrx_test_ctl | 00000000 | | |
| 0x81812708: 02_hssrx_phs_rot_ctl | 0000cb80 | 0x8181270c: | |
| 03_hssrx_phs_rot_ofs_ctl | 00000610 | | |

| | | |
|---|----------|-------------|
| 0x81812710: 04_hssrx_phs_rot_posn1 | 00003132 | 0x81812714: |
| 05_hssrx_phs_rot_posn2 | 00000023 | |
| 0x81812718: 06_hssrx_phs_rot_sta_ofs1 | 0000001e | 0x8181271c: |
| 07_hssrx_phs_rot_sta_ofs2 | 0000001f | |
| 0x81812720: 08_hssrx_dfe_ctl_PHY | 00002002 | 0x81812724: |
| 09_hssrx_dfe_smpl_snap1 | 00000000 | |
| 0x81812728: 0A_hssrx_dfe_smpl_snap2 | 00008000 | 0x8181272c: |
| 0B_hssrx_vga_ctl1 | 00004015 | |
| 0x81812730: 0C_hssrx_vga_ctl2 | 00007aa0 | 0x81812734: |
| 0D_hssrx_vga_ctl3 | 000009e4 | |
| 0x81812738: 0E_hssrx_pwr_mgmnt_ctl | 0000001f | 0x8181273c: |
| 0F_hssrx_iqamp_ctl1 | 00000018 | |
| 0x81812740: 10_hssrx_iqamp_ctl2 | 00000002 | 0x81812744: |
| 11_hssrx_dacap_dacan_sel | 00000003 | |
| 0x81812748: 12_hssrx_dacap_dacan | 0000ffff | 0x8181274c: |
| 13_hssrx_daca_min | 00000000 | |
| 0x81812750: 14_hssrx_adac_ctl | 00000000 | 0x81812754: |
| 15_hssrx_ac_cp_ctl | 000031c3 | |
| 0x81812758: 16_hssrx_ac_cp_val | 00000051 | 0x8181275c: |
| 17_hssrx_dfe_h1h2h3_lcl_off_ch | 00000014 | |
| 0x81812760: 18_hssrx_dfe_h1h2h3_lcl_off_val | 00000000 | 0x81812764: |
| 19_hssrx_peaked_intg | 000000ff | |
| 0x81812768: 1A_hssrx_cdr_analog_sw | 0000ce00 | 0x8181276c: |
| 1B_hssrx_peaking_amp_init_c_PHY | 00000000 | |
| 0x81812770: 1C_hssrx_dac_dpc | 00000040 | 0x81812774: |
| 1D_hssrx_ddc | 00000000 | |
| 0x81812778: 1E_hssrx_int_stat_PHY | 00001c0f | 0x8181277c: |
| 1F_hssrx_dfe_func_ctl1_PHY | 0000ffff | |
| 0x81812780: 20_hssrx_dfe_func_ctl2_INV | 00007ebf | 0x81812784: |
| 21_hssrx_ofs_ch_dcc_qcc_idx | 00002000 | |
| 0x81812788: 22_hssrx_dfe_ofs_val | 0000087d | 0x8181278c: |
| 23_hssrx_h_coeff_bist | 00000401 | |
| 0x81812790: 24_hssrx_ac_cap_bist | 000000c4 | 0x81812794: |
| 25_hssrx_max_gain_path_idx_res | 00007800 | |
| 0x81812798: 26_hssrx_loff_ctl | 00000040 | 0x8181279c: |
| 27_hssrx_sigdet_ctl | 00002c80 | |
| 0x818127a0: 28_hssrx_ana_ctl_sw | 00000000 | 0x818127a4: |
| 29_hssrx_intg_dac_ofs | 0000dedd | |
| 0x818127a8: 2A_hssrx_eye_ctl | 00000000 | 0x818127ac: |
| 2B_hssrx_eye_met | 00000004 | |
| 0x818127b0: 2C_hssrx_eye_met_err_cnt | 00000000 | 0x818127b4: |
| 2D_hssrx_eye_met_pdf_eyec | 00000000 | |
| 0x818127b8: 2E_hssrx_eye_met_pat_len | 0000007f | 0x818127bc: |
| 2F_hssrx_dfe_func_ctl3 | 0000dfff | |
| 0x818127c0: 30_hssrx_dfe_tap_ctl_idx_ptr | 00000008 | 0x818127c4: |
| 31_hssrx_dfe_tap | 00003030 | |
| 0x818127c8: 32_hssrx_lte_ctl_TUNE | 00000600 | 0x818127e4: |
| 39_hssrx_int_stat2 | 0000c1ff | |
| 0x818127e8: 3A_hssrx_ac_cpl_cur_src_adj | 00000041 | 0x818127ec: |
| 3B_hssrx_dcd_ctl | 00007c47 | |
| 0x818127f0: 3C_hssrx_dcc_ctl | 00000d42 | 0x818127f4: |
| 3D_hssrx_qcc_ctl | 00006948 | |
| 0x818127f8: 3E_hssrx_mac_test_ctl2 | 00000000 | 0x818127fc: |
| 3F_hssrx_mac_test_ctl1 | 00000000 | |

```

0x81812748: 12_hssrx_dacap_dacan[02]          00fe ffff
0x81812760: 18_hssrx_dfe_h1h2h3_lcl_off_va[00]    0000 0000 0000
0000 0000 0000 0000 0000
0x81812760: 18_hssrx_dfe_h1h2h3_lcl_off_va[08]    0000 0000 0000
0000 0000 0000 0000 0000
0x81812760: 18_hssrx_dfe_h1h2h3_lcl_off_va[16]    0000 0000 0000
0000 0000
0x81812788: 22_hssrx_dfe_ofs_val[00][00]          087d 7f00 7a7d
0000 7e7d 0000
0x81812788: 22_hssrx_dfe_ofs_val[03][00]          7b7b 0000 7d7f
0000 0b01 7f00
0x81812788: 22_hssrx_dfe_ofs_val[06][00]          0307 7f7f 0703
7f7f 7b01 0000
0x81812788: 22_hssrx_dfe_ofs_val[09][00]          7a7c 0000 037b
0000 007d 0000
0x81812788: 22_hssrx_dfe_ofs_val[12][00]          7f7b 0000 7b7f
0000 0105 007f
0x81812788: 22_hssrx_dfe_ofs_val[15][00]          7f7d 0000 0904
7f00 037f 7f00
0x81812788: 22_hssrx_dfe_ofs_val[18][00]          017f 0000 7e7e
0000 0007 007f
0x81812788: 22_hssrx_dfe_ofs_val[21][00]          0007 007f 0007
007f 0007 007f
0x81812788: 22_hssrx_dfe_ofs_val[24][00]          7a7a 0001 017d
7f00 7c7b 0000
0x81812794: 25_hssrx_max_gain_path_idx_res[00]    005d 0853 100b
188f 20cf 28a5 308d 3800
0x81812794: 25_hssrx_max_gain_path_idx_res[08]    40af 488a 507b
5800 6040 6800 70fd 7800
0x818127c4: 31_hssrx_dfe_tap[00]                  fffe 8080 0000
0000 0030 0030 3030 3030
0x818127c4: 31_hssrx_dfe_tap[08]                  3030 3030 3030
0000
0x818127e8: 3A_hssrx_ac_cpl_cur_src_adj[00]       0041 0041 0041
0041
0x818127ec: 3B_hssrx_dcd_ctl[00]                  7c47 5c00 7c86
5c00 7c83
0x818127f0: 3C_hssrx_dcc_ctl[00]                  0d42 0d82 0d81
0d81
0x818127f4: 3D_hssrx_qcc_ctl[00]                  6987 6948

```

xfipcs, fec, aec, & aet registers

=====

```

0x81cb8400: xfipcs_reg [00] 00002040 00000080 00000000
00000000 00000001 00000008 00000000 00000000
0x81cb8420: xfipcs_reg [08] 00008401 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81cb8440: xfipcs_reg [16] 00000000 00000000 00000000
00000000 00000040 00000000 00000000 00000000
0x81cb8460: xfipcs_reg [24] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81cb8480: xfipcs_reg [32] 00000004 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81cb8620: fec_32g_128g_reg [08] 00000000 00008003 00000000

```

```

00000000 00000000 00000000 00000000
0x81cb8648: fec_32g_128g_reg [18] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81cb8a00: aec_reg [00] 00000000 00000000 00000000
00000000 00000040 00000000 00000000 00002490
0x81cb8c00: aet_reg [00] 000000b0 00007000 000008c4
00000000 00000000

```

bbc registers

=====

```

0x81cb9800: bbc_trc 0 0 0 0 0 0 0
0
0x81cb9840: bbc_trc 0 0 0 0 0 0 0
0
0x81cb9880: bbc_trc 0 0 0 0 0 0 0
0
0x81cb98c0: bbc_trc 0 0 0 0 0 0 0
0
0x81cb9900: bbc_trc 0 0 0 0 0 0 0
0
0x81cb9804: bbc_mbc 0 0 0 0 0 0 0
0
0x81cb9844: bbc_mbc 0 0 0 0 0 0 0
0
0x81cb9884: bbc_mbc 0 0 0 0 0 0 0
0
0x81cb98c4: bbc_mbc 0 0 0 0 0 0 0
0
0x81cb9904: bbc_mbc 0 0 0 0 0 0 0
0
0x81cb9a00: bbc_rcc 0 0 0 0 0 0 0
0
0x81cb9a20: bbc_rcc 0 0 0 0 0 0 0
0
0x81cb9a40: bbc_rcc 0 0 0 0 0 0 0
0
0x81cb9a60: bbc_rcc 0 0 0 0 0 0 0
0
0x81cb9a80: bbc_rcc 0 0 0 0 0 0 0
0
0x81cb9c00: bbc_rqc 0 0 0 0 0 0 0
0
0x81cb9c20: bbc_rqc 0 0 0 0 0 0 0
0
0x81cb9c40: bbc_rqc 0 0 0 0 0 0 0
0
0x81cb9c60: bbc_rqc 0 0 0 0 0 0 0
0
0x81cb9c80: bbc_rqc 0 0 0 0 0 0 0
0
0x81cb9d00: bbc_fbpc 00000000 0x81cb9d04: bbc_csc
00000000
0x81cb9d08: bbc_rcc_inc 00000000 0x81cb9d0c:
bbc_rqc_inc 00000000

```

| | | |
|-------------------------------------|----------|----------------------|
| 0x81cb9d10: bbc_fbpc_inc | 00000000 | 0x81cb9d14: |
| bbc_tmc_inc | 00000000 | |
| 0x81cb9d18: bbc_threshold | 00080100 | 0x81cb9d1c: |
| bbc_counter_clr | 00000000 | |
| 0x81cb9d20: bbc_debug_en | 00000000 | 0x81cb9d24: bbc_ctrl |
| 00200120 | | |
| 0x81cb9d28: bbc_rqc_rcc_thresh | 00000055 | 0x81cb9d34: |
| bbc_bb_sc_n | 00000000 | |
| 0x81cb9d38: bbc_crd_reco_debug | 00000000 | 0x81cb9d3c: |
| bbc_crd_reco_debug_data | 00000000 | |
| 0x81cb9d40: bbc_multi_frm_loss_cnt | 00000000 | 0x81cb9d44: |
| bbc_multi_rdy_loss_cnt | 00000000 | |
| 0x81cb9d48: bbc_1frm_loss_recov_cnt | 00000000 | 0x81cb9d4c: |
| bbc_1rdy_loss_recov_cnt | 00000000 | |
| 0x81cb9d58: bbc_int_status | 00000000 | 0x81cb9d5c: |
| bbc_int_set | 00000000 | |
| 0x81cb9d60: bbc_int_first | 00000000 | 0x81cb9d64: |
| bbc_frm_rdy_rx_err_addr | 00000000 | |
| 0x81cb9d68: bbc_frm_rdy_tx_err_addr | 00000000 | 0x81cb9d6c: |
| bbc_trc_mbc_err_addr | 00000000 | |
| 0x81cb9d70: bbc_frm_rdy_rx_dbl_ecc | 00000000 | 0x81cb9d74: |
| bbc_frm_rdy_tx_dbl_ecc | 00000000 | |
| 0x81cb9d78: bbc_trc_mbc_dbl_ecc | 00000000 | |
| 0x81cb9d7c: bbc_fsm_status | 00001011 | 0x81cb9d80: |
| bbc_force_err | 00000000 | |
| 0x81cb9d84: bbc_crdt_avail0 | 00000000 | 0x81cb9d88: |
| bbc_crdt_avail1 | 00000000 | |
| 0x81cb9d8c: bbc_scratch | 00000000 | |

FPS registers

=====

| | | |
|--------------------------------|----------|-------------|
| 0x81cb8004: fps_er_enc_in | 00000000 | 0x81cb8008: |
| fps_er_crc | 00000000 | |
| 0x81cb800c: fps_er_trunc | 00000000 | 0x81cb8010: |
| fps_er_toolong | 00000000 | |
| 0x81cb8014: fps_er_bad_eof | 00000000 | 0x81cb8018: |
| fps_er_enc_out | 00000000 | |
| 0x81cb801c: fps_er_bad_os | 00000000 | 0x81cb8020: |
| fps_er_flush | 00000000 | |
| 0x81cb8024: fps_er_ifg | 00000000 | 0x81cb8038: |
| fps_er_crc_good_eof | 00000000 | |
| 0x81cb803c: fps_inv_arb | 00000000 | 0x81cb8040: |
| fps_slow_sts_status | 00000000 | |
| 0x81cb8044: fps_tx_frm_cnt | 00000000 | 0x81cb8048: |
| fps_rx_frm_cnt | 00000000 | |
| 0x81cb8050: fps_tx_word_cnt_hi | 00000000 | 0x81cb804c: |
| fps_tx_word_cnt_lo | 00000000 | |
| 0x81cb8058: fps_rx_word_cnt_hi | 00000000 | 0x81cb8054: |
| fps_rx_word_cnt_lo | 00000000 | |

BAL registers

=====

| | | |
|-----------------------------|----------|-------------|
| 0x81cbf000: bal_desired_buf | 00000000 | 0x81cbf004: |
| bal_alloc_buf | 00000000 | |

```

0x81cbf008: bal_busy_buf          00000000    0x81cbf00c:
bal_usable_buf          00000000
0x81cbf010: bal_max_bor_buf          00000000
0x81cbf014: bal_busy_buf_thresh      00000002

```

TXQ registers

=====

```

0x81cbb004: txq_phys_port_ctl      00470000
0x81cbb050: txq_link_skew          00000000
0x81cbb068: txq_cr_lk_dttm_intr_sts [00] 00000000 00000000
0x81cbb070: txq_cr_lk_dttm_intr_en [00] 00000000 00000000
0x81cbb024: txq_disc_frm_trap_cnt  00000014

```

FDS registers

=====

```

0x81cbc000: fds_rxf_ctl            00000002    0x81cbc004:
fds_rxf_wait_thresh    00000909
0x81cbc018: fds_rxf_first_error    00000000    0x81cbc01c:
fds_rxf_first_error_info 00000000
0x81cbc020: fds_rxf_inout_pkt_cnt  00000000
0x81cbc008: fds_rxf_err_int_status 00000000    0x81cbc024:
fds_rxf_fifo_status    00888888
0x81cbd000: fds_txf_ctl            0000003a    0x81cbd004:
fds_txf_wait_ifg_thresh 00a00106
0x81cbd008: fds_txf_err_int_status 00000000    0x81cbd024:
fds_txf_fifo_status    00088888
0x81cbd02c: fds_txf_bbc_scs        00000000

```

Logical TXQ registers

=====

```

0x81cbb000: txq_log_port_ctl      00000002    0x81cbb008:
txq_port_status        00000000
0x81cbb00c: txq_todo_flags        [00] 00000000 00000000
0x81cbb014: txq_spd_match_desc    [00] 00000000 00000000 00000000
00000000
0x81cbb024: txq_spd_match_desc    [04] 00000014
0x81cbb028: txq_vc_weight         [00] 01010101 01010101 01010101
01010101
0x81cbb038: txq_vc_weight         [04] 01010101 01010101 01010101
01010101
0x81cbb048: txq_vc_weight         [08] 01010101 00010101
0x81cbb054: txq_cong_dttm_ctrl    00000106
0x81cbb058: txq_cong_dttm_intr_sts [00] 00000000 00000000
0x81cbb060: txq_cong_dttm_intr_en [00] 00000000 00000000
0x81cbb078: txq_bw_limit_en_reg   [00] 00000000 00000000
0x81cbb080: txq_bw_gua_en_reg     [00] 00000000 00000000
0x81cbb088: txq_vc_group          [00] 03030300 03030303 03030303
03030303
0x81cbb098: txq_vc_group          [04] 03030303 03030303 03030303
03030303
0x81cbb0a8: txq_vc_group          [08] 03030303 03030303 00000000
00000000
0x81cbb0b0: txq_bw_thresh_group   [00] 00000000 00000000 00000000
00000000

```

| | | | | |
|---------------------------------|------|----------|----------|----------|
| 0x81cbb0c0: txq_bw_thresh_group | [04] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81cbb0d0: txq_bw_thresh_group | [08] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81cbb0e0: txq_bw_thresh_group | [12] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81cbb0f0: txq_bw_thresh_group | [16] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81cbb100: txq_bw_thresh_group | [20] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81cbb110: txq_bw_thresh_group | [24] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81cbb120: txq_bw_thresh_group | [28] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81cbb130: txq_bw_thresh_group | [32] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81cbb140: txq_bw_thresh_group | [36] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |

txq Congestion detection Statistics RAM

=====

| | | |
|--------------------|----------|--------------------|
| 0x81090e60: vc[0] | 00000000 | 0x81090e64: vc[1] |
| 00000000 | | |
| 0x81090e68: vc[2] | 00000000 | 0x81090e6c: vc[3] |
| 00000000 | | |
| 0x81090e70: vc[4] | 00000000 | 0x81090e74: vc[5] |
| 00000000 | | |
| 0x81090e78: vc[6] | 00000000 | 0x81090e7c: vc[7] |
| 00000000 | | |
| 0x81090e80: vc[8] | 00000000 | 0x81090e84: vc[9] |
| 00000000 | | |
| 0x81090e88: vc[10] | 00000000 | 0x81090e8c: vc[11] |
| 00000000 | | |
| 0x81090e90: vc[12] | 00000000 | 0x81090e94: vc[13] |
| 00000000 | | |
| 0x81090e98: vc[14] | 00000000 | 0x81090e9c: vc[15] |
| 00000000 | | |
| 0x81090ea0: vc[16] | 00000000 | 0x81090ea4: vc[17] |
| 00000000 | | |
| 0x81090ea8: vc[18] | 00000000 | 0x81090eac: vc[19] |
| 00000000 | | |
| 0x81090eb0: vc[20] | 00000000 | 0x81090eb4: vc[21] |
| 00000000 | | |
| 0x81090eb8: vc[22] | 00000000 | 0x81090ebc: vc[23] |
| 00000000 | | |
| 0x81090ec0: vc[24] | 00000000 | 0x81090ec4: vc[25] |
| 00000000 | | |
| 0x81090ec8: vc[26] | 00000000 | 0x81090ecc: vc[27] |
| 00000000 | | |
| 0x81090ed0: vc[28] | 00000000 | 0x81090ed4: vc[29] |
| 00000000 | | |
| 0x81090ed8: vc[30] | 00000000 | 0x81090edc: vc[31] |
| 00000000 | | |
| 0x81090ee0: vc[32] | 00000000 | 0x81090ee4: vc[33] |

```

00000000
0x81090ee8: vc[34]      00000000      0x81090eec: vc[35]
00000000
0x81090ef0: vc[36]      00000000      0x81090ef4: vc[37]
00000000
0x81090ef8: vc[38]      00000000      0x81090efc: vc[39]
00000000

```

Logical STS registers

=====

```

0x815851c4: sts_ftb_type1_miss  00000000
0x815851c8: sts_ftb_type2_miss  00000000
0x815851cc: sts_ftb_type6_miss  00000000
0x815851d0: sts_hard_zoning_miss 00000000
0x815851d4: sts_lun_zoning_miss  00000000
0x815851dc: sts_unroutable      00000000
0x815821f4: sts_rte_cl2         00000000      0x815821f8:
sts_rte_cl3           00000000      0x815821fc: sts_rte_link_ctl
00000000              0x815851e8: sts_tx_timeout  00000000

```

Logical STS filter registers

=====

```

0x81585140: stsflt_trig [00] 00000000 00000000 00000000
00000000
0x81585150: stsflt_trig [04] 00000000 00000000 00000000
00000000
0x81585160: stsflt_trig [08] 00000000 00000000 00000000
00000000
0x81585170: stsflt_trig [12] 00000000 00000000 00000000
00000000
0x81585180: stsflt_trig [16] 00000000 00000000 00000000
00000000
0x81585190: stsflt_trig [20] 00000000 00000000 00000000
00000000
0x815851a0: stsflt_trig [24] 00000000 00000000 00000000
00000000
0x815851b0: stsflt_trig [28] 00000000 00000000 00000000
00000000
0x815851c0: stsflt_trig [32]

```

Logical STS discard registers

=====

```

0x8158316c: disc_mcast_wka      00000000      0x81583170:
disc_inv_did          00000000
0x81583174: disc_cl1_cl4        00000000      0x81583178:
disc_sid_chk_fail     00000000
0x8158317c: disc_inv_dom_egid_txpt 00000000      0x81583180:
disc_vft_hop_cnt_1    00000000
0x81583184: disc_classf         00000000      0x81583188:
disc_fcp_cdb_inv      00000000
0x8158318c: disc_vfid_trap_enabled 00000000      0x81583190:
disc_vfid_hdr_chk_fail 00000000
0x81583194: disc_shim_cksum_fail 00000000      0x81583198:

```

```

disc_fed_edit_cmd_err 00000000
0x8158319c: disc_ftb_vm_mode 00000000 0x815831a0:
disc_ftb_agnt2_miss 00000000
0x815831a4: disc_ecb_reserved 00000000 0x815831a8:
disc_ecb_de_pad_err 00000000
0x815831ac: disc_ecb_de_tag_err 00000000 0x815831b0:
disc_ecb_de_seq_err 00000000
0x815831b4: disc_ecb_err 00000000 0x815831b8:
disc_ftb_type4_match 00000000
0x815831bc: disc_fcp_rsp_ftb_type4 00000000 0x815831c0:
disc_ftb_type5_match 00000000
0x815831c4: disc_ftb_type3_match 00000000 0x815831c8:
disc_els_ftb_type3 00000000
0x815831cc: disc_ftb_type1_match 00000000 0x815831d0:
disc_els_rsp_ex_port 00000000
0x815831d4: disc_inv_drp_dps 00000000 0x815831d8:
disc_did_lookup_miss 00000000
0x815831dc: disc_ftb_type2_match 00000000 0x815831e0:
disc_trpd_plogi_pdisc 00000000
0x815831e4: disc_type2_lookup_miss 00000000 0x815831e8:
disc_ftb_type6_match 00000000
0x815831ec: disc_els_rep_ex_port 00000000 0x815831f0:
disc_els_sid_lkup_bit1 00000000
0x815831f4: disc_els_sid_lkup_bit0 00000000 0x815831f8:
disc_bls_frm_trap_bit1 00000000
0x815831fc: disc_ftb_token_err 00000000 0x81583200:
disc_asic_internal_err 00000000
0x81583204: disc_hard_zone_miss 00000000 0x81583208:
disc_lun_zone_miss 00000000
0x8158320c: discflt_frame_disc 00000000 0x81583210:
discflt_parity_err 00000000
0x81583214: disc_frame_marked_du 00000000 0x81583218:
disc_frame_marked_to 00000000
0x8158321c: disc_lkup_rte_prty_err 00000000

```

portstatsshow 44

```

stat_wtx 0 4-byte words transmitted
stat_wrx 0 4-byte words received
stat_ftx 0 Frames transmitted
stat_frx 0 Frames received
stat_c2_frx 0 Class 2 frames received
stat_c3_frx 0 Class 3 frames received
stat_lc_rx 0 Link control frames
received
stat_mc_rx 0 Multicast frames
received
stat_mc_to 0 Multicast timeouts
stat_mc_tx 0 Multicast frames
transmitted
tim_txcrd_z 0 Time TX Credit Zero
(2.5Us ticks)
tim_txcrd_z_vc 0- 3: 0 0 0 0
tim_txcrd_z_vc 4- 7: 0 0 0 0

```


| | | | | | |
|----------------|--------|---|---|---|---|
| tim_txcrd_z_vc | 8-11: | 0 | 0 | 0 | 0 |
| tim_txcrd_z_vc | 12-15: | 0 | 0 | 0 | 0 |
| lat_tot_pkt_vc | 0- 3: | 1 | 1 | 1 | 1 |
| lat_tot_pkt_vc | 4- 7: | 1 | 1 | 1 | 1 |
| lat_tot_pkt_vc | 8-11: | 1 | 1 | 1 | 1 |
| lat_tot_pkt_vc | 12-15: | 1 | 1 | 1 | 1 |
| lat_hi_time_vc | 0- 3: | 0 | 0 | 0 | 0 |
| lat_hi_time_vc | 4- 7: | 0 | 0 | 0 | 0 |
| lat_hi_time_vc | 8-11: | 0 | 0 | 0 | 0 |
| lat_hi_time_vc | 12-15: | 0 | 0 | 0 | 0 |
| lat_lo_time_vc | 0- 3: | 1 | 1 | 1 | 1 |
| lat_lo_time_vc | 4- 7: | 1 | 1 | 1 | 1 |
| lat_lo_time_vc | 8-11: | 1 | 1 | 1 | 1 |
| lat_lo_time_vc | 12-15: | 1 | 1 | 1 | 1 |
| max_latency_vc | 0- 3: | 1 | 1 | 1 | 1 |
| max_latency_vc | 4- 7: | 1 | 1 | 1 | 1 |
| max_latency_vc | 8-11: | 1 | 1 | 1 | 1 |
| max_latency_vc | 12-15: | 1 | 1 | 1 | 1 |

latency_dma_ts 09-09-2024 UTC Mon 08:47:25 TXQ

Latency DMA TimeStamp

| | | |
|------------------------------|---|-------------------------|
| fec_cor_detected | 0 | Count of blocks that |
| were corrected by FEC | | |
| fec_uncor_detected | 0 | Count of blocks that |
| were left uncorrected by FEC | | |
| er_enc_in | 0 | Encoding errors inside |
| of frames | | |
| er_crc | 0 | Frames with CRC errors |
| er_trunc | 0 | Frames shorter than |
| minimum | | |
| er_toolong | 0 | Frames longer than |
| maximum | | |
| er_bad_eof | 0 | Frames with bad end-of- |
| frame | | |
| er_enc_out | 0 | Encoding error outside |
| of frames | | |
| er_bad_os | 0 | Invalid ordered set |
| er_pcs_blk | 0 | PCS block errors |
| er_rx_c3_timeout | 0 | Class 3 receive frames |
| discarded due to timeout | | |
| er_tx_c3_timeout | 0 | Class 3 transmit frames |
| discarded due to timeout | | |
| er_unroutable | 0 | Frames that are |
| unroutable | | |
| er_unreachable | 0 | Frame with unreachable |
| destination | | |
| er_other_discard | 0 | Other discards |
| er_type1_miss | 0 | frames with FTB type 1 |
| miss | | |
| er_type2_miss | 0 | frames with FTB type 2 |
| miss | | |
| er_type6_miss | 0 | frames with FTB type 6 |
| miss | | |
| er_zone_miss | 0 | frames with hard zoning |
| miss | | |

| | | |
|-----------------------|-----------------------------|--------------------------|
| er_lun_zone_miss | 0 | frames with LUN zoning |
| miss | | |
| er_crc_good_eof | 0 | Crc error with good eof |
| er_inv_arb | 0 | Invalid ARB |
| er_single_credit_loss | 0 | Single vcrdy/frame loss |
| on link | | |
| er_multi_credit_loss | 0 | Multiple vcrdy/frame |
| loss on link | | |
| other_credit_loss | 0 | Link timeout/complete |
| credit loss | | |
| phy_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | Timestamp of |
| phy_port stats clear | | |
| lgc_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | Timestamp of |
| lgc_port stats clear | | |
| fec_corrected_rate | 0 | FEC Corrected blocks per |
| second | | |

portstats64show 44

| | | |
|---------------|---|--|
| stat64_wtx | 0 | top_int : 4-byte words transmitted |
| | 0 | bottom_int : 4-byte words transmitted |
| stat64_wrx | 0 | top_int : 4-byte words received |
| | 0 | bottom_int : 4-byte words received |
| stat64_ftx | 0 | top_int : Frames transmitted |
| | 0 | bottom_int : Frames transmitted |
| stat64_frx | 0 | top_int : Frames received |
| | 0 | bottom_int : Frames received |
| stat64_c2_frx | 0 | top_int : Class 2 frames received |
| | 0 | bottom_int : Class 2 frames received |
| stat64_c3_frx | 0 | top_int : Class 3 frames received |
| | 0 | bottom_int : Class 3 frames received |
| stat64_lc_rx | 0 | top_int : Link control frames received |
| | 0 | bottom_int : Link control frames |
| received | | |
| stat64_mc_rx | 0 | top_int : Multicast frames received |
| | 0 | bottom_int : Multicast frames received |
| stat64_mc_to | 0 | top_int : Multicast timeouts |
| | 0 | bottom_int : Multicast timeouts |
| stat64_mc_tx | 0 | top_int : Multicast frames transmitted |
| | 0 | bottom_int : Multicast frames |
| transmitted | | |
| tim64_rdy_pri | 0 | top_int : Time R_RDY high priority |
| | 0 | bottom_int : Time R_RDY high priority |
| tim64_txcrd_z | 0 | top_int : Time BB_credit zero |
| | 0 | bottom_int : Time BB_credit zero |
| er64_enc_in | 0 | top_int : Encoding errors inside of |
| frames | | |
| | 0 | bottom_int : Encoding errors inside of |
| frames | | |
| er64_crc | 0 | top_int : Frames with CRC errors |
| | 0 | bottom_int : Frames with CRC errors |
| er64_trunc | 0 | top_int : Frames shorter than minimum |
| | 0 | bottom_int : Frames shorter than minimum |
| er64_toolong | 0 | top_int : Frames longer than maximum |
| | 0 | bottom_int : Frames longer than maximum |

| | | |
|---|---|--|
| er64_bad_eof | 0 | top_int : Frames with bad end-of-frame |
| | 0 | bottom_int : Frames with bad end-of- |
| frame | | |
| er64_enc_out | 0 | top_int : Encoding error outside of |
| frames | 0 | bottom_int : Encoding error outside of |
| frames | | |
| er64_disc_c3 | 0 | top_int : Class 3 frames discarded |
| | 0 | bottom_int : Class 3 frames discarded |
| er64_pcs_blk | 0 | top_int : PCS block errors |
| | 0 | bottom_int : PCS block errors |
| stat64_rateTxFrame | 0 | Tx frame rate (fr/sec) |
| stat64_rateRxFrame | 0 | Rx frame rate (fr/sec) |
| stat64_rateTxPeakFrame | 0 | Tx peak frame rate (fr/sec) |
| stat64_rateRxPeakFrame | 0 | Rx peak frame rate (fr/sec) |
| stat64_rateTxWord | 0 | Tx Word rate (words/sec) |
| stat64_rateRxWord | 0 | Rx Word rate (words/sec) |
| stat64_rateTxPeakWord | 0 | Tx peak Word rate (words/sec) |
| stat64_rateRxPeakWord | 0 | Rx peak Word rate (words/sec) |
| stat64_PRJTFrames | 0 | top_int : Number of PRJT frames |
| returned to this port | 0 | bottom_int : Number of PRJT |
| frames returned to this port | | |
| stat64_PBSYFrames | 0 | top_int : Number of PBSY frames |
| returned to this port | 0 | bottom_int : Number of PBSY |
| frames returned to this port | | |
| stat64_inputBuffersFull | 0 | top_int : Number of occurrences |
| when all input buffers full | 0 | bottom_int : Number of |
| occurrences when all input buffers full | | |
| stat64_rxClass1Frames | 0 | top_int : Number of class 1 |
| frames received | 0 | bottom_int : Number of class 1 |
| frames received | | |
| stat64_aveTxFrameSize | 0 | Average Tx Frame size |
| stat64_aveRxFrameSize | 0 | Average Rx Frame size |
| Lr_in | 0 | top_int |
| | 0 | bottom_int |
| Ols_in | 0 | top_int |
| | 0 | bottom_int |
| Lr_out | 0 | top_int |
| | 0 | bottom_int |
| Ols_out | 0 | top_int |
| | 0 | bottom_int |
| Link_failure | 0 | top_int |
| | 0 | bottom_int |
| Invalid_CRC | 0 | top_int |
| | 0 | bottom_int |
| Invalid_word | 0 | top_int |
| | 0 | bottom_int |
| Protocol_err | 0 | top_int |
| | 0 | bottom_int |
| Loss_of_sig | 0 | top_int |

```

Loss_of_sync      0          bottom_int
                  0          top_int
er_bad_os         0          bottom_int
                  0          top_int : Invalid ordered set
                  0          bottom_int: Invalid ordered set

```

```

portrouteshow 44
port address ID: 0x012c00
external unicast routing table:
  0: Embedded
 255: Embedded
internal unicast routing table:
  0: Embedded

```

```
portcamshow 44
```

```

-----
Port  SID used  DID used  SID entries  DID entries
44    0         0         000000      000000
-----

```

```
ptbufshow, ptcreditshow, ptdatashow, ptstatshow 44
```

```

S:
S:VF Enable:          1
S:
S:C4 Global Variable:
S:-----
S:trace_stop:        0
S:
S:C4 Phy Data Pointers: c4_phyp = 0xb6ae4100
S:-----
S:tnodep              0xbb845a80      pt
   0x43028017
S:proto_phyp          0xb880a7e0      phy_cfg
0xb6ae5140
S:c4_chp              0x97e28000      c4_lgcp
0x97fa4000
S:c4_phy_regp        0x81cb8000      proc_dir
0xb851bf00
S:-----
S:magic_id            0xc4345678      num_port_timer      12
S:prev_if_id         0x43020017      S:ftx                0
   tov              0
S:initialized        1          port_idx              23
S:ui_idx              44          slot_no
   0
S:blade_idx          23          sw_usr_ports          400
S:unused              0          intr_debounced
   0
S:aec_status         0x0          reason_code
   0

```

| | | | |
|------------------------------|------------|-----------------------|-----|
| S:debug | 0x00000004 | debug_trc_line | 0 |
| S:rxbuf_list_head | 0xffffffff | rxbuf_list_tail | |
| 0xffffffff | | | |
| S:isAePort | 0 | port_misc_data | |
| 0 | | | |
| S:num_fault1_rx_disc | 0 | num_fault2_rx_disc | 0 |
| S:p_lli_cause0 | 0 | p_sig_regained | 0 |
| S:p_sync_regained | 0 | enc_out | |
| 0x0 | | | |
| S:cached_fps_status | 0 | cached_sts_status | 0 |
| S:cached_er_crc_good_eof | 0 | | |
| S:cached_er_bad_os | 0 | cached_er_too_long | 0 |
| S:cached_er_trunc | 0 | | |
| cached_tot_er_crc_good_eof | 0 | | |
| S:num_pt_excess_intr | 0 | num_no_fid | 0 |
| S:num_fault1_cnt | 0 | num_fault2_cnt | |
| 0 | | | |
| S:num_fault_lip | 0 | num_fault_lli | 0 |
| S:num_fault_rx_fifo | 0 | num_fault_hss | 0 |
| S:num_fault_bwait | 0 | lli_intr_prim | |
| 0 | | | |
| S:num_sw_link_to | 0 | | |
| be_link_err_mon_count | 0 | | |
| S:ecb_enc_enabled | 0 | ecb_comp_enabled | |
| 0 | | | |
| S:ecb_rsv_enc | 0 | ecb_rsv_comp | 0 |
| S:ecb_enc_bm | 0x0 | ecb_key_index | |
| 0xffffffff | | | |
| S:fab_idx | 0 | | |
| S:num_be_lto | 0 | lto_count_reset_intvl | |
| 0 | | | |
| S:lr_count_reset_intvl | 0 | num_be_lr | |
| 0 | | | |
| S:num_fault_qsfm | 0 | check_lto | |
| 0 | | | |
| S:credit_loaded | 0 | num_credit_overrun | |
| 0 | | | |
| S:fec_enabled | 0x0 | fec_los_to_flag | 0x0 |
| S:phy_stats_clear_ts | 1725611419 | pcs_err_online | |
| 0 | | | |
| S:pcs_err_light_det | 0 | pcs_err_ignore | |
| 0 | | | |
| S:pcs_blk_err | 0 | pcs_hiber | 0 |
| S:phy_port_status | 0 | ecb_enc_lr_count | |
| 0 | | | |
| S:dport_mode | 0 | avoid_lto_det | 0 |
| S:sn_debounced | 0x0 | sn_started_kr_reqd | 0 |
| S:major_timer_started | 0x0 | ready_bm | 0x0 |
| S:parln_1_bm | 0x0 | parln_0_bm | 0x0 |
| S:be_los_of_sync_event_intvl | | 0 | |
| be_los_of_sync_event | 0 | | |
| S:errataPtenable_cntr | 0 | errataPoll_cntr | |
| 0 | | | |
| S:jda_rx_sig_loss_det | 0 | jda_rx_sig_loss_cnt | |

```

      0
S:encrypt_blk_error          0
S:
S:      c4_trunk
S:=====
S:mark_ts                    0x0          deskew          0x0
S:master_phyp                0x0
S:
S:adelay[00]: 0x00000000 0x00000000 0x00000000 0x00000000
S:adelay[04]: 0x00000000 0x00000000 0x00000000 0x00000000
S:
S:      c4_buf
S:=====
S:tx_csc                      0          rx_csc
      0
S:ld_vc_credits              0          tx_flag          0x0
S:alloc_buffers              0          req_buffers       0
S:est_buffers                 20         ld_use_est        0
S:bb_sc_n                     0          rx_bb_sc_n
      0
S:data_cr                     5          nondata_cr
      6
S:cr_enable                   0
S:ld_nondata_cr              6          tnodep
0xbb845b60
S:tx_credits[0] 0 0 0 0 0 0 0 0
S:tx_credits[8] 0 0 0 0 0 0 0 0
S:tx_credits[16] 0 0 0 0 0 0 0 0
S:tx_credits[24] 0 0 0 0 0 0 0 0
S:tx_credits[32] 0 0 0 0 0 0 0 0
S:rx_credits[0] 0 0 0 0 0 0 0 0
S:rx_credits[8] 0 0 0 0 0 0 0 0
S:rx_credits[16] 0 0 0 0 0 0 0 0
S:rx_credits[24] 0 0 0 0 0 0 0 0
S:rx_credits[32] 0 0 0 0 0 0 0 0
S:tx_mbc[0] 0 0 0 0 0 0 0 0
S:tx_mbc[8] 0 0 0 0 0 0 0 0
S:tx_mbc[16] 0 0 0 0 0 0 0 0
S:tx_mbc[24] 0 0 0 0 0 0 0 0
S:tx_mbc[32] 0 0 0 0 0 0 0 0
S:rx_mbc[0] 0 0 0 0 0 0 0 0
S:rx_mbc[8] 0 0 0 0 0 0 0 0
S:rx_mbc[16] 0 0 0 0 0 0 0 0
S:rx_mbc[24] 0 0 0 0 0 0 0 0
S:rx_mbc[32] 0 0 0 0 0 0 0 0
S:
S:C4 Chip Variables: c4_phyp->c4_chp = 0x97e28000
S:-----
-----
S:version = 2.1
S:magic_id                    0xc4234567   init_state        0x8
S:reset_reg_mem               0x1
S:ch_int0_en_bm               0x0          intr0_cause       0x0
S:ch_int1_en_bm               0x0          intr1_cause       0x0

```

| | | | |
|---------------------------|------------|---------------------|-----------------------|
| S:ch_int2_en_bm | 0x0 | intr2_cause | 0x0 |
| S:ch | 0x43010080 | ch_cfg | |
| 0xb7013ba0 | | | |
| S:raslog_hndl.hndl | 0x0 | obj_halted | 0x0 |
| S:c4_chip_regp | 0x80000000 | c4_fpg_regp | |
| 0x81800000 | | | |
| S:num_chip_timer | 0x5 | | |
| S:hi_task_bm | 0x0 | lo_task_bm | 0x0 |
| S:c4_deferq.q_head | 0x0 | c4_deferq.q_tail | 0x0 |
| S:c4_tmrq.q_head | 0x0 | c4_tmrq.q_tail | 0x0 |
| slot_no | 0 | | |
| S:chip_inst | 0 | chip_idx | 0 |
| S:pll_initialized | 1 | | |
| pll_serdes_initialized | 1 | | |
| S:init_tries | 0 | init_ptEnableBM | |
| 0xba01b488 | | | |
| S:tick_polling | 0xb980c9c0 | sec_polling | |
| 0xb980c960 | | | |
| S:bb_fid | 129 | | |
| S:ecb_key_bm[0] | 0x0 | ecb_key_bm[1] | 0x0 |
| S:ecb_key_bm[2] | 0x0 | ecb_key_bm[3] | 0x0 |
| S:is_chip_enc_enabled | | 0 | |
| is_chip_comp_enabled | 0x0 | | |
| S:ftb_rsrcp->ftb_flags | 0x0 | act_rsrcp->act_flag | 0x1 |
| S:lue_rsrcp->lue_flags[0] | 0x0 | lue_rsrcp- | |
| >lue_flags[1] | 0x0 | | |
| S:c4_phyp[00]: | 0xb6ab0000 | 0xb6ab2080 | 0xb6ab4100 0xb6ab6180 |
| S:c4_phyp[04]: | 0xb6ab9040 | 0xb6abb0c0 | 0xb6abd140 0xb6ac0000 |
| S:c4_phyp[08]: | 0xb6ac2080 | 0xb6ac4100 | 0xb6ac6180 0xb6ac9040 |
| S:c4_phyp[12]: | 0xb6ac60c0 | 0xb6acd140 | 0xb6ad0000 0xb6ad2080 |
| S:c4_phyp[16]: | 0xb6ad4100 | 0xb6ad6180 | 0xb6ad9040 0xb6adb0c0 |
| S:c4_phyp[20]: | 0xb6add140 | 0xb6ae0000 | 0xb6ae2080 0xb6ae4100 |
| S:c4_phyp[24]: | 0xb6ae6180 | 0xb6ae9040 | 0xb6aeb0c0 0xb6aed140 |
| S:c4_phyp[28]: | 0xb6af0000 | 0xb6af2080 | 0xb6af4100 0xb6af6180 |
| S:c4_phyp[32]: | 0xb6af9040 | 0xb6afb0c0 | 0xb6afd140 0xb6b00000 |
| S:c4_phyp[36]: | 0xb6b02080 | 0xb6b04100 | 0xb6b06180 0xb6b09040 |
| S:c4_phyp[40]: | 0xb6b0b0c0 | 0xb6b0d140 | 0xb6b10000 0xb6b12080 |
| S:c4_phyp[44]: | 0xb6b14100 | 0xb6b16180 | 0xb6b19040 0xb6b1b0c0 |
| S:c4_phyp[48]: | 0xb6b1d140 | 0xb6b20000 | 0xb6b22080 0xb6b24100 |
| S:c4_phyp[52]: | 0xb6b26180 | 0xb6b29040 | 0xb6b2b0c0 0xb6b2d140 |
| S:c4_phyp[56]: | 0xb6b30000 | 0xb6b32080 | 0xb6b34100 0xb6b36180 |
| S:c4_phyp[60]: | 0xb6b39040 | 0xb6b3b0c0 | 0xb6b3d140 0xb6b40000 |
| S:c4_lgcp[00]: | 0x97f48000 | 0x97f4c000 | 0x97f50000 0x97f54000 |
| S:c4_lgcp[04]: | 0x97f58000 | 0x97f5c000 | 0x97f60000 0x97f64000 |
| S:c4_lgcp[08]: | 0x97f68000 | 0x97f6c000 | 0x97f70000 0x97f74000 |
| S:c4_lgcp[12]: | 0x97f78000 | 0x97f7c000 | 0x97f80000 0x97f84000 |
| S:c4_lgcp[16]: | 0x97f88000 | 0x97f8c000 | 0x97f90000 0x97f94000 |
| S:c4_lgcp[20]: | 0x97f98000 | 0x97f9c000 | 0x97fa0000 0x97fa4000 |
| S:c4_lgcp[24]: | 0x97fa8000 | 0x97fac000 | 0x97fb0000 0x97fb4000 |
| S:c4_lgcp[28]: | 0x97fb8000 | 0x97fbc000 | 0x97fc0000 0x97fc4000 |
| S:c4_lgcp[32]: | 0x97fc8000 | 0x97fcc000 | 0x97fd0000 0x97fd4000 |
| S:c4_lgcp[36]: | 0x97fd8000 | 0x97fdc000 | 0x97fe0000 0x97fe4000 |
| S:c4_lgcp[40]: | 0x97fe8000 | 0x97fec000 | 0x97ff0000 0x97ff4000 |
| S:c4_lgcp[44]: | 0x97ff8000 | 0x97ffc000 | 0x8e000000 0x8e004000 |

```

S:c4_lgcp[48]: 0x8e008000 0x8e00c000 0x8e010000 0x8e014000
S:c4_lgcp[52]: 0x8e018000 0x8e01c000 0x8e020000 0x8e024000
S:c4_lgcp[56]: 0x8e028000 0x8e02c000 0x8e030000 0x8e034000
S:c4_lgcp[60]: 0x8e038000 0x8e03c000 0x8e040000 0x8e044000
S:chip_timers[00]: 0xb980c720 0xb980c780 0xb980c7e0 0xb980c840
S:chip_timers[04]: 0xb980c8a0 0xb980c900
S:disc_trap_enable_required      0x0                rxlp_disc_log_stop
      0x0
S:curr_rxlp_frm_cnt      0x0                curr_rxlp_disc_frm_cnt  0x0
S:sw_disc_frm_cnt      0x0                last_disc_frm_cnt      0x0
S:txq_nopop_pr_cnt      0x0                pollErrataDfe_ptBM
0xba01b4b0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][0]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][1] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][2]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][0] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][1]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][2] 0x0
S:
S:C4 Logical Port Variables
S:-----
-----
S:c4_lgc_regp      0x81cb8000
S:c4_phyp:
S:      0xb6ae4100      0x0                0x0                0x0

S:      0x0                0x0                0x0                0x0

S:master_phyp      0xb6ae4100      if_id
0x43020017
S:min_phyp      0x0                max_phyp      0x0
S:num_phy_ports      1                lgc_num      23
S:num_iu_to      0                sw_txq_bm
0
S:port_fid      128                unused      0
S:port_group      2                lgc_stats_clear_ts
1725611419
S:domain_tbl_sel      0                area_tbl_sel
0
S:egid_tbl_sel      0
S:serv_lo_bm      0x0
S:
S:Proto Phy Variables:
S:-----
-----
S:magic_id      0xc4123456      asic_phyp
0xb6ae4100
S:port_id      0x43028017      phy_cfg
0xb6ae5140
S:upsm_hdl      0xb8017280      physm_hdl
0xb8017000
S:ov_snsn_hdl      0xb8016e60      sw_snsn_hdl
0xb8016f00
S:ov_lksm_hdl      0xb80170a0      sw_lksm_hdl

```


0xb8017140
S:trksm_hdl 0xb80171e0 lr_flag 0x0
S:lr_active 0x0 qsfp_tsrx_rate_sel
0x0

S:
S:UPSM UP00: UPST_PORT_DISABLED --> UP01:
UPST_START_PORT_INIT
S:SNSM(OV) SN00: OV_SNST_STOPPED --> SN00: OV_SNST_STOPPED
S:SNSM(SW) SW00: SW_SNST_STAGE_WS --> SW00: SW_SNST_STAGE_WS
S:PHYSM UNKNOWN --> PP03: PHYST_NO_SIGNAL
S:LKSM(OV) LK00: OV_LKST_INACTIVE --> LK00: OV_LKST_INACTIVE
S:LKSM(SW) SW13: INACTIVE --> SW13: INACTIVE
S:TRKSM TRK0: TRKST_INIT --> TRK0: TRKST_INIT

S:
S:physm variables:

S:-----

S:proto_phyp 0xb880a7e0 physm_hdl
0xb8017000
S:force_offline 0 copper 0
S:fault_reason 0: UNKNOWN
S:phy_media_present 1

S:
S:sns variables:

S:-----

S:speed 0xff proto_phyp
0xb880a7e0
S:hw_sn_tries_left 0x0 sw_sn_tries_left 0x0
S:curr_txsp_count 0x0
S:tx_max 0x0 curr_tx_indx
0x0
S:curr_tx 0x0 curr_rxsp_count
0x0
S:rx_max 0x0 curr_rx_indx
0x0
S:curr_rx 0x0 rx_mem
0x0
S:rxsp_rec_count 0x0
S:nc_start 0x0 tx_start 0x0
S:sync_start 0x0 sync_present 0x0
S:diag_auto 0x0 diag_speed 0xff
S:striped_wd_tov 3000 hw_wd_tov
3000
S:step 0x0 qsfp28_speed_mode
0x0
S:qsfp_mode0_hw_sn_tries_left 0x0
S:qsfp_mode1_hw_sn_tries_left 0x0

S:
S:lksm variables:

S:-----

S:proto_phyp 0xb880a7e0 ov_lksm_hdl
0xb80170a0

```

sw_lksm_hdl          0xb8017140
num_lf1              0
S:hw_link_tries_left 0          sw_link_tries_left 0
S:buf_ptype          0x0          stored_entry_state 0x6
S:handshake_owner    0x0          0x0          mark_unsent
          0x0
S:busybuf_stuck      0x0          lr_wait          0x0
S:
S:trksm variables:
S:-----

```

```

S:Not a trunk port
S:
S:upsm variables:
S:-----

```

```

S:proto_phyp        0xb880a7e0    upsm_hdl
0xb8017280
S:bb_credits         0          port_beacon      0
S:port_diag_flag    0          force_offline
0
S:port_fault_rsn    0: PORT_NO_FAULT
S:retry_init_rsn    0: UNKNOWN
S:linit_reason       0          linit_result     0
S:ie_fctl_mode       0          fec_in_sync_tries_left 0
S:retry_sn_fail_init 0
retry_link_fail_init 0
S:excess_lr_count   0
S:
S:c4_ch_cfg
S:-----

```

```

S:c4_desc_ring_size 256      292      256      256      292
292      2      292      292
S:thresh_def         0          16         1          0
S:intr_tries         500          cmem_pattern
0xdeadbeef
S:cmem_pattern_upwd 2          cmem_init_time 16
S:cmem_init_tries   5
S:ctrl_par_thresh   2          data_par_thresh
4
S:cam_par_thresh     4          buf_loss_thresh
12
S:crit_par_thresh    2          non_crit_par_thresh
6
S:pci_abort_thresh   10         pci_err_thresh 5
S:excess_chintr_thresh 8          sw_err_thresh 20
S:err_sample_period 300          intr_sleep
20000
S:frame_timeout      2500          proxy_dev        16384
S:vf_route           81920          qos              2048
S:stats              2048          f_redirect       2048
S:rsp_trap           2048          lun_zoning       20480
S:area_mode          0          ftb_max_loop[0] 0

```

```

S:ftb_max_loop[1]      6          ftb_max_loop[2]      9
S:ftb_max_loop[3]     10         ftb_max_loop[4]     10
S:ftb_max_loop[5]     5          ftb_max_loop[6]     6
S:ftb_seg_size[0]     0          ftb_seg_size[1]
16384
S:ftb_seg_size[2]     65536     ftb_seg_size[3]
16384
S:ftb_seg_size[4]     16384     ftb_seg_size[5]
65536
S:ftb_seg_size[6]     16384     ftb_seg_base[0]      0
S:ftb_seg_base[1]     0          ftb_seg_base[2]
65536
S:ftb_seg_base[3]     16384     ftb_seg_base[4]
32768
S:ftb_seg_base[5]     131072    ftb_seg_base[6]
49152
asic_err_monitor_period1 300
asic_err_monitor_period2 86400
zone_chk_to_poll_period 25
zone_chk_class2_reject_tov 220
S:
S:c4_phy_cfg
S:-----
-----
S:version = 2.1
S:pt      0x43028017      fab_ptr
0x9a800000
S:fabattr      0x9a8000d4      fab_iop
0x9a800050
S:cfgbm      0xbb8458c4      port_ctrl
0xb6ae5158
S:pcap.pcap_bm      0x8d215547      pcap.pcap2_bm
0x588289
S:pcap.pcap3_bm      0x1bea60c
ui_idx      44          S:slot_no
0
is_icl      0          S:sw_usr_ports      400
S:neg_speed      0 0 0 0 0 0
S:my_domain      0x1          port_mode      0x0
S:hw_sn_maxtries      100          sw_sn_maxtries
0
S:hw_link_maxtries      10          sw_link_maxtries      5
S:rx_cyc_tov      28          rttov      300
S:bufrdy_tov      300          busybuf_tov      286
S:mark_tov      300          lksm_tov      3000
S:buf_dealloc_wait      4          hw_wd_tov      3000
S:hw_lk_train_tov      540          hw_lk_test_tov
150
S:syswait_tx_12_lips      1          lip_rx_tov      55
S:al_time_tov      15          lp_tov      2000
S:intr_tries_port      500          intr_mod_debounce
250
S:intr_lsrflt_debounce      500          intr_efifo_debounce      100
S:port_no_fid      3          excess_ptintr_thresh      8

```

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S:port_fault1_thresh      100          port_fault1_spur_thresh 250
S:port_fault1_disc_thresh      500
port_fault1_disc_spur_thresh 1000
S:port_fault2_thresh      5          losync_tov          100
S:port_sw_link_to          15          en_8g_scramble
      1
frc_hw_sn_mode            0x1
S:enc_poll_thresh          0          fec_enable
      0
S:fec_in_sync_to          50          fec_in_sync_try_max
      4
S:port_be_lto_threshold      100          port_be_lr_threshold
      2
S:be_cr_in_sync_to          5
port_credit_overrun_thresh      10
S:jda_sfp_losig_tov          400
jda_sfp_losig_try_max          30
S:striped_wd_tov            3000
no_sync_debounce            1200
S:
S:      fab_iop
S:=====
S:fab_iop->interop_mode 0x0          fab_iop->lab_mode      0x0
S:fab_iop->fl_bbc          0x0          fab_iop->fl_fan
      0x0
S:fab_iop->fl_cls          0x4          fab_iop->fl_rscn
      0x0
S:fab_iop->domain_id_offset 0x60          fab_iop-
>mcdt_fabric_mode          0x0
S:fab_iop->mcdt_default_zone 0x0          fab_iop-
>mcdt_safe_zone            0x0
S:
S:      port_ctrl
S:=====
S:port_ctrl.port_type      1          port_ctrl.port_grp      2
S:port_ctrl.port_number 44          port_ctrl.vc_mode        1
S:
S:      port_ctrl.lcap
S:=====
S:has_serdes                0          has_media                1
S:topology                  1          skip_nego                 0
S:skip_pnego                 0          skip_init_event           0
S:en_shim                    0          speed_neg
      1
S:loop_back                  0          num_speeds                5
S:fec_enable                  0
S:
S:      port_ctrl.speed_list array
S:=====
S:speed_list[0].auto_neg    1          speed_list[0].lnk_speed  0x0000000a
S:speed_list[1].auto_neg    1          speed_list[1].lnk_speed  0x00000008
S:speed_list[2].auto_neg    0          speed_list[2].lnk_speed  0x00000006
S:speed_list[3].auto_neg    1          speed_list[3].lnk_speed  0x00000005
S:speed_list[4].auto_neg    0          speed_list[4].lnk_speed  0x00000003

```

```

S:speed_list[5].auto_neg  0      speed_list[5].lnk_speed  0x00000000
S:
S:      port_ctrl.cm
S:=====
S:port_ctrl.cm.num_vcs      8
S:port_ctrl.cm.min_bufs    8
S:port_ctrl.cm.cr_shar_bufs 0
S:port_ctrl.vc_alloc
S:port_ctrl.vc_alloc      2 0 1 1 1 1 1 1
S:port_ctrl.vc_alloc      0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.norm_vc_alloc
S:port_ctrl.norm_vc_alloc  4 0 5 5 5 5 1 1
S:port_ctrl.norm_vc_alloc  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.cm.skip_bb_credit      0
S:port_ctrl.cm.use_shim_based_sublist      0
S:
S:      port_ctrl.serdes_set
S:=====
S:serdes_type      0x8
S:serdes_data_t.ibm_hss_serdes.tx_drive_power      0x1
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b_sign  0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b      0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_a      0x0
S:serdes_data_t.ibm_hss_serdes.rxeq      0x0
S:
S:      cfgbm
S:=====
S:old_distance      0x0      gport_lockdown      0x0
S:tport      0x1      speed      0x0
S:disable_eport      0x0      fcacc      0x0
S:lport_lockdown      0x0      priv_lport_lockdown
0x0
S:vcxlt_linit      0x0      delay_flogi      0x0
S:isl_interop      0x0      distance      0x0
S:BufStarvFlag      0x0      credit_sharing      0x0
S:lport_halfduplex  0x0      lport_fairness      0x0
S:soft_neg      0x0      asn_frc_hwretry      0x0
S:cr_recov      0x0      fport_buffers      0x0
S:export      0x0      export_mode
0x0
S:csctl_en      0x0      mirror_port      0x0
S:fault_delay      0x0      non_dfe      0x0
S:fec_configured*(0=ENAB)  0      fec_tts
0
S:port_persistently_disabled (permanently) 0 (0)
S:
S:      cfg property
S:=====
S:priv_pcfg_bm      0x00000000      lgcl_pcfg_bm
0xbb845904
S:fport_buffer      0x00000000
S:

```

```

S:
S:C4 Discard Cntrs: rxlp_stats = 0xb6ae44b0
S:-----
-----
S:disc_mcast_wka          0x0          disc_inv_did          0x0
S:disc_cl1_cl4           0x0          disc_sid_chk_fail    0x0
S:disc_inv_dom_egid_txpt 0x0          disc_vft_hop_cnt_1
0x0
S:disc_classf            0x0          disc_fcp_cdb_inv     0x0
S:disc_vfid_trap_enabled 0x0          0x0
disc_vfid_hdr_chk_fail 0x0
S:disc_shim_cksum_fail   0x0          disc_fed_edit_cmd_err 0x0
S:disc_shim_cksum_fail   0x0          disc_fed_edit_cmd_err 0x0
S:disc_ftb_vm_mode       0x0          disc_ftb_agnt2_miss  0x0
S:disc_ecb_de_pad_err     0x0          disc_ecb_de_tag_err  0x0
S:disc_ecb_de_seq_err     0x0          disc_ecb_err          0x0
S:disc_ftb_type4_match   0x0          disc_fcp_rsp_ftb_type4 0x0
S:disc_fcp_rsp_ftb_type4 0x0          disc_ftb_type5_match
0x0
S:disc_ftb_type3_match   0x0          disc_els_ftb_type3   0x0
S:disc_ftb_type1_match   0x0          disc_els_rsp_ex_port 0x0
S:disc_inv_drp_dps       0x0          disc_did_lookup_miss 0x0
S:disc_ftb_type2_match   0x0          disc_trpd_plogi_pdisc 0x0
S:disc_type2_lookup_miss 0x0          disc_ftb_type6_match
0x0
S:disc_els_rep_ex_port   0x0          disc_els_sid_lkup_bit1 0x0
S:disc_els_sid_lkup_bit0 0x0          0x0
disc_bls_frm_trap_bit1 0x0
S:disc_ftb_token_err     0x0          disc_asic_internal_err 0x0
S:disc_hard_zone_miss    0x0          disc_lun_zone_miss   0x0
S:discflt_frame_disc     0x0          discflt_parity_err   0x0
S:disc_frame_marked_du   0x0          disc_frame_marked_to 0x0
E:Connection type: FE
E:Port type: F_port
E:Trunk port: No
E:Configured Speed: AUTO_SPEED_NEGO
E:Max Capable Speed: 32G
E:Current SNSM Speed: UNDEFINED
E:Hardware TX Speed: 32G (0x00000004)
E:Hardware RX Speed: 32G (0x00000040)
E:
E:Interrupts: 0          Link_failure: 0
Loss_of_sync: 0          Loss_of_sig: 0
E:Lli: 0                Invalid_word: 0
E:trapped_frm: 0          fwd_status_ok: 0
E:fwd_timeout: 0          fwd_tx_unavail: 0
E:fwd_unroutable: 0          fwd_zone_out: 0
E:fwd_other_err: 0          frm_err_discard: 0
E:Fltr listA: 0          Fltr listB: 0
E:Zone trap fwd: 0          Zone trap disc: 0
E:shim_csum: 0           RTE_perr: 0
E:Invalid_crc: 0          Delim_err: 0
E:Protocol_err: 0
E:Lr_in: 0               Lr_out: 0

```

E:0ls_in: 0 0ls_out: 0

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FILTER DATA

Shadow settings:

- Filter Enable: 0x00000000
- Redir RAM[0]: 0x00000000
- Redir RAM[1]: 0x00000000
- Redir RAM[2]: 0x00000000
- Redir RAM[3]: 0x00000000
- Redir RAM[4]: 0x00000000
- Redir RAM[5]: 0x00000000
- Redir RAM[6]: 0x00000000
- Redir RAM[7]: 0x00000000
- Redir RAM[8]: 0x00000000
- Redir RAM[9]: 0x00000000
- Redir RAM[10]: 0x00000000
- Redir RAM[11]: 0x00000000
- Redir RAM[12]: 0x00000000
- Redir RAM[13]: 0x00000000
- Redir RAM[14]: 0x00000000
- Redir RAM[15]: 0x00000000
- Redir RAM[16]: 0x00000000
- Redir RAM[17]: 0x00000000
- Redir RAM[18]: 0x00000000
- Redir RAM[19]: 0x00000000
- Redir RAM[20]: 0x00000000
- Redir RAM[21]: 0x00000000
- Redir RAM[22]: 0x00000000
- Redir RAM[23]: 0x00000000
- Redir RAM[24]: 0x00000000
- Redir RAM[25]: 0x00000000
- Redir RAM[26]: 0x00000000
- Redir RAM[27]: 0x00000000
- Redir RAM[28]: 0x00000000
- Redir RAM[29]: 0x00000000
- Redir RAM[30]: 0x00000000
- Redir RAM[31]: 0x00000000
- Bypass: 0x00000000

Real settings:

- Enable RAM: 0x00000000, 0x00000000
- Redir RAM[0]: 0x00000000
- Redir RAM[1]: 0x00000000
- Redir RAM[2]: 0x00000000
- Redir RAM[3]: 0x00000000
- Redir RAM[4]: 0x00000000
- Redir RAM[5]: 0x00000000
- Redir RAM[6]: 0x00000000
- Redir RAM[7]: 0x00000000
- Redir RAM[8]: 0x00000000
- Redir RAM[9]: 0x00000000

Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass RAM: 0x00000000

Shadowed filters:

Filter 0: Not Installed (MIRROR1)(LISTA)
c4_fldenable[0] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[0] = 0x00000000,c4_fltr_config[0] = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
c4_fldenable[1] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[1] = 0x00000000,c4_fltr_config[1] = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
c4_fldenable[2] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[2] = 0x00000000,c4_fltr_config[2] = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
c4_fldenable[3] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[3] = 0x00000000,c4_fltr_config[3] = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
c4_fldenable[4] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[4] = 0x00000000,c4_fltr_config[4] = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
c4_fldenable[5] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[5] = 0x00000000,c4_fltr_config[5] = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
c4_fldenable[6] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[6] = 0x00000000,c4_fltr_config[6] = 0x00000000

Filter 7: Not Installed (TIN TRAP)(LISTA)
c4_fldenable[7] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[7] = 0x00000000,c4_fltr_config[7] = 0x00000000

Filter 8: Not Installed (FICON CUP)(LISTA)
c4_fldenable[8] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[8] = 0x00000000,c4_fltr_config[8] = 0x00000000

Filter 9: Not Installed (FICON CUP DST)(LISTA)
c4_fldenable[9] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[9] = 0x00000000,c4_fltr_config[9] = 0x00000000

Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
c4_fldenable[10] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[10] = 0x00000000,c4_fltr_config[10] =
0x00000000

Filter 11: Not Installed (SIM)(LISTA)
c4_fldenable[11] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[11] = 0x00000000,c4_fltr_config[11] =
0x00000000

Filter 12: Not Installed (UNUSED)(LISTA)
c4_fldenable[12] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[12] = 0x00000000,c4_fltr_config[12] =
0x00000000

Filter 13: Not Installed (UNUSED)(LISTA)
c4_fldenable[13] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[13] = 0x00000000,c4_fltr_config[13] =
0x00000000

Filter 14: Not Installed (UNUSED)(LISTA)
c4_fldenable[14] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[14] = 0x00000000,c4_fltr_config[14] =
0x00000000

Filter 15: Not Installed (UNUSED)(LISTA)
c4_fldenable[15] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[15] = 0x00000000,c4_fltr_config[15] =
0x00000000

Filter 16: Not Installed (PERF1)(LISTA)
c4_fldenable[16] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[16] = 0x00000000,c4_fltr_config[16] =
0x00000000

Filter 17: Not Installed (PERF2)(LISTA)
c4_fldenable[17] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[17] = 0x00000000,c4_fltr_config[17] =
0x00000000

Filter 18: Not Installed (PERF3)(LISTA)
c4_fldenable[18] = 0x00000000 0x00000000 0x00000000

```
0x00000000
    c4_fldnegate[18] = 0x00000000,c4_fltr_config[18] =
0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
    c4_fldenable[19] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[19] = 0x00000000,c4_fltr_config[19] =
0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
    c4_fldenable[20] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[20] = 0x00000000,c4_fltr_config[20] =
0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
    c4_fldenable[21] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[21] = 0x00000000,c4_fltr_config[21] =
0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
    c4_fldenable[22] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[22] = 0x00000000,c4_fltr_config[22] =
0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
    c4_fldenable[23] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[23] = 0x00000000,c4_fltr_config[23] =
0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
    c4_fldenable[24] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[24] = 0x00000000,c4_fltr_config[24] =
0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
    c4_fldenable[25] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[25] = 0x00000000,c4_fltr_config[25] =
0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
    c4_fldenable[26] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[26] = 0x00000000,c4_fltr_config[26] =
0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
    c4_fldenable[27] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[27] = 0x00000000,c4_fltr_config[27] =
0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
    c4_fldenable[28] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[28] = 0x00000000,c4_fltr_config[28] =
0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
```

```
    c4_fldenable[29] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[29] = 0x00000000,c4_fltr_config[29] =
0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    c4_fldenable[30] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[30] = 0x00000000,c4_fltr_config[30] =
0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    c4_fldenable[31] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[31] = 0x00000000,c4_fltr_config[31] =
0x00000000
```

Real filters:

```
Filter 0: Not Installed (MIRROR1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
```

Filter 9: Not Installed (FICON CUP DST)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 11: Not Installed (SIM)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 12: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 13: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 14: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 15: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 16: Not Installed (PERF1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 17: Not Installed (PERF2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 18: Not Installed (PERF3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 19: Not Installed (PERF4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 20: Not Installed (PERF5)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 21: Not Installed (PERF6)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 22: Not Installed (PERF7)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,

```

0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000

```

```

Filter dirty indicator: 0x00000000
Performance filters: 0
Port Mirror filters: 0 (0x0)

```

FIELD DATA

Shadowed fields:

```

fldoffset[0] = 0x00, fldmask[0] = 0x00, fldvalue_dyna[0]: 0x00 0x00
0x00 0x00
fldcontrol[0].inuse = 0x0  fldcontrol[0].refcnt = 0x00 0x00 0x00
0x00
fldoffset[1] = 0x00, fldmask[1] = 0x00, fldvalue_dyna[1]: 0x00 0x00

```

```
0x00 0x00
fldcontrol[1].inuse = 0x0  fldcontrol[1].refcnt = 0x00 0x00 0x00
0x00
fldoffset[2] = 0x00, fldmask[2] = 0x00, fldvalue_dyna[2]:0x00 0x00
0x00 0x00
fldcontrol[2].inuse = 0x0  fldcontrol[2].refcnt = 0x00 0x00 0x00
0x00
fldoffset[3] = 0x00, fldmask[3] = 0x00, fldvalue_dyna[3]:0x00 0x00
0x00 0x00
fldcontrol[3].inuse = 0x0  fldcontrol[3].refcnt = 0x00 0x00 0x00
0x00
fldoffset[4] = 0x00, fldmask[4] = 0x00, fldvalue_dyna[4]:0x00 0x00
0x00 0x00
fldcontrol[4].inuse = 0x0  fldcontrol[4].refcnt = 0x00 0x00 0x00
0x00
fldoffset[5] = 0x00, fldmask[5] = 0x00, fldvalue_dyna[5]:0x00 0x00
0x00 0x00
fldcontrol[5].inuse = 0x0  fldcontrol[5].refcnt = 0x00 0x00 0x00
0x00
fldoffset[6] = 0x00, fldmask[6] = 0x00, fldvalue_dyna[6]:0x00 0x00
0x00 0x00
fldcontrol[6].inuse = 0x0  fldcontrol[6].refcnt = 0x00 0x00 0x00
0x00
fldoffset[7] = 0x00, fldmask[7] = 0x00, fldvalue_dyna[7]:0x00 0x00
0x00 0x00
fldcontrol[7].inuse = 0x0  fldcontrol[7].refcnt = 0x00 0x00 0x00
0x00
fldoffset[8] = 0x00, fldmask[8] = 0x00, fldvalue_dyna[8]:0x00 0x00
0x00 0x00
fldcontrol[8].inuse = 0x0  fldcontrol[8].refcnt = 0x00 0x00 0x00
0x00
fldoffset[9] = 0x00, fldmask[9] = 0x00, fldvalue_dyna[9]:0x00 0x00
0x00 0x00
fldcontrol[9].inuse = 0x0  fldcontrol[9].refcnt = 0x00 0x00 0x00
0x00
fldoffset[10] = 0x00, fldmask[10] = 0x00, fldvalue_dyna[10]:0x00 0x00
0x00 0x00
fldcontrol[10].inuse = 0x0  fldcontrol[10].refcnt = 0x00 0x00 0x00
0x00
fldoffset[11] = 0x00, fldmask[11] = 0x00, fldvalue_dyna[11]:0x00 0x00
0x00 0x00
fldcontrol[11].inuse = 0x0  fldcontrol[11].refcnt = 0x00 0x00 0x00
0x00
fldoffset[12] = 0x00, fldmask[12] = 0x00, fldvalue_dyna[12]:0x00 0x00
0x00 0x00
fldcontrol[12].inuse = 0x0  fldcontrol[12].refcnt = 0x00 0x00 0x00
0x00
fldoffset[13] = 0x00, fldmask[13] = 0x00, fldvalue_dyna[13]:0x00 0x00
0x00 0x00
fldcontrol[13].inuse = 0x0  fldcontrol[13].refcnt = 0x00 0x00 0x00
0x00
fldoffset[14] = 0x00, fldmask[14] = 0x00, fldvalue_dyna[14]:0x00 0x00
0x00 0x00
fldcontrol[14].inuse = 0x0  fldcontrol[14].refcnt = 0x00 0x00 0x00
```

```
0x00
fldoffset[15] = 0x00, fldmask[15] = 0x00, fldvalue_dyna[15]:0x00 0x00
0x00 0x00
fldcontrol[15].inuse = 0x0 fldcontrol[15].refcnt = 0x00 0x00 0x00
0x00
fldoffset[16] = 0x00, fldmask[16] = 0x00, fldvalue_dyna[16]:0x00 0x00
0x00 0x00
fldcontrol[16].inuse = 0x0 fldcontrol[16].refcnt = 0x00 0x00 0x00
0x00
fldoffset[17] = 0x00, fldmask[17] = 0x00, fldvalue_dyna[17]:0x00 0x00
0x00 0x00
fldcontrol[17].inuse = 0x0 fldcontrol[17].refcnt = 0x00 0x00 0x00
0x00
fldoffset[18] = 0x00, fldmask[18] = 0x00, fldvalue_dyna[18]:0x00 0x00
0x00 0x00
fldcontrol[18].inuse = 0x0 fldcontrol[18].refcnt = 0x00 0x00 0x00
0x00
fldoffset[19] = 0x00, fldmask[19] = 0x00, fldvalue_dyna[19]:0x00 0x00
0x00 0x00
fldcontrol[19].inuse = 0x0 fldcontrol[19].refcnt = 0x00 0x00 0x00
0x00
```

Real fields:

```
fldoffset RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000
fldmask RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000
fld value4 RAM:
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
Field dirty indicator: 0x00000000
```

```
FDB reference count fdb: 0 [0 0 0 0 ]
FDB reference count fdb: 1 [0 0 0 0 ]
FDB reference count fdb: 2 [0 0 0 0 ]
```

FDB reference count fdb: 3 [0 0 0 0]
FDB reference count fdb: 4 [0 0 0 0]
FDB reference count fdb: 5 [0 0 0 0]
FDB reference count fdb: 6 [0 0 0 0]
FDB reference count fdb: 7 [0 0 0 0]
FDB reference count fdb: 8 [0 0 0 0]
FDB reference count fdb: 9 [0 0 0 0]
FDB reference count fdb: 10 [0 0 0 0]
FDB reference count fdb: 11 [0 0 0 0]
FDB reference count fdb: 12 [0 0 0 0]
FDB reference count fdb: 13 [0 0 0 0]
FDB reference count fdb: 14 [0 0 0 0]
FDB reference count fdb: 15 [0 0 0 0]
FDB reference count fdb: 16 [0 0 0 0]
FDB reference count fdb: 17 [0 0 0 0]
FDB reference count fdb: 18 [0 0 0 0]
FDB reference count fdb: 19 [0 0 0 0]

Filter counters:

Filter counter 0: 0 (MIRROR1)
Filter counter 1: 0 (MIRROR2)
Filter counter 2: 0 (MIRROR3)
Filter counter 3: 0 (MIRROR4)
Filter counter 4: 0 (AEPORT_NON_MIRR_DROP)
Filter counter 5: 0 (ZONING TRAP)
Filter counter 6: 0 (FCR_EXPORT_DC)
Filter counter 7: 0 (TIN TRAP)
Filter counter 8: 0 (FICON CUP)
Filter counter 9: 0 (FICON CUP DST)
Filter counter 10: 0 (WELL KNOWN ADDR)
Filter counter 11: 0 (SIM)
Filter counter 12: 0 (UNUSED)
Filter counter 13: 0 (UNUSED)
Filter counter 14: 0 (UNUSED)
Filter counter 15: 0 (UNUSED)
Filter counter 16: 0 (PERF1)
Filter counter 17: 0 (PERF2)
Filter counter 18: 0 (PERF3)
Filter counter 19: 0 (PERF4)
Filter counter 20: 0 (PERF5)
Filter counter 21: 0 (PERF6)
Filter counter 22: 0 (PERF7)
Filter counter 23: 0 (PERF8)
Filter counter 24: 0 (PERF9)
Filter counter 25: 0 (PERF10)
Filter counter 26: 0 (PERF11)
Filter counter 27: 0 (PERF12)
Filter counter 28: 0 (OPM1)
Filter counter 29: 0 (OPM2)
Filter counter 30: 0 (IPM1)
Filter counter 31: 0 (IPM2)

ACL DATA

Logical port 23: Hard Zoning disabled, Soft Zoning disabled
Zone type: WWN Zoning
Frames with hard zone miss: 0

*** Please use filterportshow on user port 56 to display ACL hash tables and Mirroring resources of thischip.
***We show this data only for the first physical port which is an external port.

portFcPortCmdShow --slot 0 45 3
doing portFcPortCmdShow: arg1 = 3, arg2 = -2

portshow 45
portDisableReason: None
portCFlags: 0x1
portFlags: 0x1 PRESENT U_PORT
LocalSwcFlags: 0x0
portType: 26.0
POD Port: Port is licensed
portState: 2 Offline
Protocol: FC
portPhys: 4 No_Light portScn: 2 Offline
port generation number: 0
state transition count: 1

portId: 012d00
portIfId: 43020014
portWwn: 20:2d:d8:1f:cc:2c:99:90
portWwn of device(s) connected:
16b Area list:
Distance: normal
portSpeed: N32Gbps

FEC: Inactive
Credit Recovery: Inactive
LE domain: 0
Peer beacon: Off
FC Fastwrite: OFF

| | | | | |
|-------------|---|---------------|---|-------|
| Interrupts: | 0 | Link_failure: | 0 | Frjt: |
| 0 | | | | |
| Unknown: | 0 | Loss_of_sync: | 0 | Fbsy: |
| 0 | | | | |
| Lli: | 0 | Loss_of_sig: | 0 | |
| Proc_rqrd: | 0 | Protocol_err: | 0 | |
| Timed_out: | 0 | Invalid_word: | 0 | |
| Tx_unavail: | 0 | Invalid_crc: | 0 | |
| Delim_err: | 0 | Address_err: | 0 | |
| Lr_in: | 0 | Ols_in: | 0 | |
| Lr_out: | 0 | Ols_out: | 0 | |

portloginshow 45
Type PID World Wide Name credit df_sz cos
=====

portloginshow 45 -history

| Type | PID | World Wide Name | logout time |
|------|-----|-----------------|-------------|
|------|-----|-----------------|-------------|

=====

portregshow 45

LED registers

=====

| | | |
|---------------------------|----------|-------------|
| 0x81ca2000: c4_led_status | 00000000 | 0x81ca2004: |
| c4_led_ctl | 00000000 | |

FPL registers

=====

| | | |
|---------------------------------|----------|-------------|
| 0x81ca0200: fpl_port_config | 23298002 | |
| 0x81ca020c: fpl_port_id_ctl | 00000000 | 0x81ca0210: |
| fpl_port_id_addr | 00012d00 | |
| 0x81ca0214: fpl_port_speed | 00000004 | 0x81ca021c: |
| fpl_lli_ctl | 00000100 | |
| 0x81ca0228: fpl_lli_os_ctl | bc94ffff | 0x81ca022c: |
| fpl_lli_send_word | bc95b5b5 | |
| 0x81ca0230: fpl_lli_mark_rx | 00000000 | 0x81ca0234: |
| fpl_lli_rnd_trip_time | 00000000 | |
| 0x81ca0238: fpl_lli_ns_status | 00130007 | 0x81ca023c: |
| fpl_lli_intr_status | 00030007 | |
| 0x81ca0244: fpl_lli_def | 00100000 | 0x81ca0254: |
| fpl_lli_intr_enable_clr | 001c0000 | |
| 0x81ca0258: fpl_err_intr_status | 00000000 | 0x81ca0260: |
| fpl_err_intr_enable_clr | 00000000 | |
| 0x81ca0268: fpl_err_first_error | 00000000 | 0x81ca026c: |
| fpl_speed_neg_ctl | 00000000 | |
| 0x81ca0270: fpl_speed_neg_stat | 00000000 | 0x81ca0274: |
| fpl_softasn_ctl | 0000000f | |
| 0x81ca0278: fpl_link_init_ctl | 00000000 | 0x81ca027c: |
| fpl_link_init_stat | 00000000 | |
| 0x81ca0280: fpl_aec_ctl | 001c1060 | 0x81ca0284: |
| fpl_aec_ctl2 | 04009f60 | |
| 0x81ca0288: fpl_pcs_ctl | 00000170 | 0x81ca028c: |
| fpl_fec_ctl | 00000424 | |
| 0x81ca0290: fpl_fec_cor | 00000000 | 0x81ca0294: |
| fpl_fec_uncor | 00000000 | |
| 0x81ca0298: fpl_hss_link_ctl | 0031f040 | 0x81ca029c: |
| fpl_afifo_link_ctl | 00000a86 | |
| 0x81ca02a0: fpl_echo_lb_ctl | 0000028c | 0x81ca02a4: |
| fpl_scratch | 00000121 | |
| 0x81ca02a8: fpl_debug | 00060005 | 0x81ca02ac: |
| fpl_misc_debug | 00000800 | |
| 0x00000000: SW_shadow_reg | 00000000 | 0x00000000: |
| SW_c4_phyp->cfgptr | 00030003 | |

per-fpg (per octet) registers

=====

```

0x8181382c: fpg_serdes_ctla0      81a37be7    0x81813830:
fpg_serdes_ctla1      81a37be7
0x81813834: fpg_serdes_ctlb0      81a1c3c3    0x81813838:
fpg_serdes_ctlb1      81a1c3c3
0x8181383c: fpg_serdes_xgmii_1ms  00067c28    0x81813840:
fpg_serdes_regtimctl  40e47946
0x81813844: fpg_serdes_asnrsttimctl 00000102

```

HSS PLL registers

=====

```

0x81813400: 00_hssplla_vco_coarse_cal0  00000000    0x81813404:
01_hssplla_vco_coarse_cal1    00000014
0x81813408: 02_hssplla_vco_coarse_cal2  00000000    0x8181340c:
03_hssplla_vco_coarse_cal3    00000000
0x81813410: 04_hssplla_vco_coarse_cal4  00000000    0x81813424:
09_hssplla_power_ctl          00000000
0x81813428: 0A_hssplla_charge_pump_ctl   00000004    0x81813438:
0E_hssplla_pll_misc_ctl       00000000
0x8181343c: 0F_hssplla_pclk_ctl          000000f8    0x81813440:
10_hssplla_eyem_intv_ctl      00000000
0x81813444: 11_hssplla_eyem_intv_lim1    00000000    0x81813448:
12_hssplla_eyem_intv_lim2    00000000
0x8181344c: 13_hssplla_eyem_intv_lim3    00000000    0x81813450:
14_hssplla_eyem_intv_lim4    00000000
0x818134f0: 3C_hssplla_macro_tst_ctl4    00000000    0x818134f4:
3D_hssplla_macro_tst_ctl3    00000000
0x818134f8: 3E_hssplla_macro_tst_ctl2    00000000    0x818134fc:
3F_hssplla_macro_tst_ctl1    00000000
0x81813500: 00_hssppll_vco_coarse_cal0  0000000a    0x81813504:
01_hssppll_vco_coarse_cal1    00000014
0x81813508: 02_hssppll_vco_coarse_cal2  00000000    0x8181350c:
03_hssppll_vco_coarse_cal3    00000000
0x81813510: 04_hssppll_vco_coarse_cal4  00000000    0x81813524:
09_hssppll_power_ctl          00000000
0x81813528: 0A_hssppll_charge_pump_ctl   00000004    0x81813538:
0E_hssppll_pll_misc_ctl       00000000
0x8181353c: 0F_hssppll_pclk_ctl          000000f8    0x81813540:
10_hssppll_eyem_intv_ctl      00000000
0x81813544: 11_hssppll_eyem_intv_lim1    00000000    0x81813548:
12_hssppll_eyem_intv_lim2    00000000
0x8181354c: 13_hssppll_eyem_intv_lim3    00000000    0x81813550:
14_hssppll_eyem_intv_lim4    00000000
0x818135f0: 3C_hssppll_macro_tst_ctl4    00000000    0x818135f4:
3D_hssppll_macro_tst_ctl3    00000000
0x818135f8: 3E_hssppll_macro_tst_ctl2    00000000    0x818135fc:
3F_hssppll_macro_tst_ctl1    00000000

```

HSS TX registers

=====

```

0x81812000: 00_hsstx_cfg_mode_PHY        00009f48    0x81812004:
01_hsstx_test_ctl             00000000
0x81812008: 02_hsstx_coeff_ctl_INV       00000000    0x8181200c:
03_hsstx_drv_mode_ctl         00000000
0x81812010: 04_hsstx_drv_ovrd_ctl        00000010    0x81812014:

```

| | | | |
|---|----------|----------|-------------|
| 05_hsstx_dclk_align_ovrd | 00000080 | | |
| 0x81812018: 06_hsstx_imp_cal_ovrd | | 00000c0c | 0x8181201c: |
| 07_hsstx_dclk_drift_tol | 00000004 | | |
| 0x81812020: 08_hsstx_tap0_coeff_TUNE | | 00000000 | 0x81812024: |
| 09_hsstx_tap1_coeff_TUNE | 00000003 | | |
| 0x81812028: 0A_hsstx_tap2_coeff_TUNE | | 00000019 | 0x8181202c: |
| 0B_hsstx_tap3_coeff_TUNE | 00000003 | | |
| 0x81812034: 0D_hsstx_pol_INV | | 0000000a | 0x81812038: |
| 0E_hsstx_ae_cmd | 00000000 | | |
| 0x8181203c: 0F_hsstx_ae_stat | | 00000000 | 0x81812040: |
| 10_hsstx_ae_tap0_TUNE | 00000000 | | |
| 0x81812044: 11_hsstx_ae_tap1_TUNE | | 00000000 | 0x81812048: |
| 12_hsstx_ae_tap2_TUNE | 00000028 | | |
| 0x8181204c: 13_hsstx_ae_tap3_TUNE | | 00000000 | 0x81812054: |
| 15_hsstx_app_tune | 0000120e | | |
| 0x81812058: 16_hsstx_analog_diag | | 00000000 | 0x81812060: |
| 18_hsstx_4x_seg_app | 0000aa00 | | |
| 0x81812064: 19_hsstx_2x_seg_app | | 000000aa | 0x81812068: |
| 1A_hsstx_1x_seg_app | 0000f5e4 | | |
| 0x8181206c: 1B_hsstx_seg_4x_term_app | | 0000000f | 0x81812070: |
| 1C_hsstx_seg_2x1x_term_app | 00000001 | | |
| 0x81812074: 1D_hsstx_tap_sign_app | | 0000000a | 0x81812078: |
| 1E_hsstx_ext_addr_data | 00000001 | | |
| 0x8181207c: 1F_hsstx_ext_addr_addr | | 00000000 | 0x81812080: |
| 20_hsstx_pat_buf_bytes_1_0 | 00000000 | | |
| 0x81812084: 21_hsstx_pat_buf_bytes_3_2 | | 00000000 | 0x81812088: |
| 22_hsstx_pat_buf_bytes_5_4 | 00000000 | | |
| 0x8181208c: 23_hsstx_pat_buf_bytes_7_6 | | 00000000 | 0x8181209c: |
| 27_hsstx_8023az_ctl | 00000000 | | |
| 0x818120a0: 28_hsstx_dcc_ctl | | 000060c0 | 0x818120a4: |
| 29_hsstx_dcc_ovrd | 00000000 | | |
| 0x818120a8: 2A_hsstx_dcc_app | | 00000102 | 0x818120ac: |
| 2B_hsstx_dcc_timeout | 0000ffff | | |
| 0x818120c0: 30_hsstx_tap_sign_ovrd | | 00000000 | 0x818120c8: |
| 32_hsstx_seg_4x_ovrd | 00000000 | | |
| 0x818120cc: 33_hsstx_seg_2x_ovrd | | 00000000 | 0x818120d0: |
| 34_hsstx_seg_1x_ovrd | 00000000 | | |
| 0x818120d8: 36_hsstx_tap_seg_4x_term_ovrd | | 00000000 | 0x818120dc: |
| 37_hsstx_tap_seg_2x_term_ovrd | 00000000 | | |
| 0x818120e0: 38_hsstx_tap_seg_1x_term_ovrd | | 00000000 | 0x818120ec: |
| 3B_hsstx_mac_test_ctl5 | 00000000 | | |
| 0x818120f0: 3C_hsstx_mac_test_ctl4 | | 00000000 | 0x818120f4: |
| 3D_hsstx_mac_test_ctl3 | 00000000 | | |
| 0x818120f8: 3E_hsstx_mac_test_ctl2 | | 00000000 | 0x818120fc: |
| 3F_hsstx_mac_test_ctl1 | 000000c6 | | |

HSS RX registers

=====

| | | | |
|------------------------------------|----------|----------|-------------|
| 0x81812200: 00_hssrx_cfg_mode_PHY | | 00009e78 | 0x81812204: |
| 01_hssrx_test_ctl | 00000000 | | |
| 0x81812208: 02_hssrx_phs_rot_ctl | | 0000cb80 | 0x8181220c: |
| 03_hssrx_phs_rot_ofs_ctl | 00000610 | | |
| 0x81812210: 04_hssrx_phs_rot_posn1 | | 00001f1d | 0x81812214: |
| 05_hssrx_phs_rot_posn2 | 0000000d | | |

| | | |
|--|----------------|-------------|
| 0x81812218: 06_hssrx_phs_rot_sta_ofs1 | 00000102 | 0x8181221c: |
| 07_hssrx_phs_rot_sta_ofs2 | 00000000 | |
| 0x81812220: 08_hssrx_dfe_ctl_PHY | 00002002 | 0x81812224: |
| 09_hssrx_dfe_smpl_snap1 | 00000000 | |
| 0x81812228: 0A_hssrx_dfe_smpl_snap2 | 00008000 | 0x8181222c: |
| 0B_hssrx_vga_ctl1 | 000041fb | |
| 0x81812230: 0C_hssrx_vga_ctl2 | 00007aa0 | 0x81812234: |
| 0D_hssrx_vga_ctl3 | 000009e4 | |
| 0x81812238: 0E_hssrx_pwr_mgmt_ctl | 0000001f | 0x8181223c: |
| 0F_hssrx_iqamp_ctl1 | 00000019 | |
| 0x81812240: 10_hssrx_iqamp_ctl2 | 00000016 | 0x81812244: |
| 11_hssrx_dacap_dacan_sel | 00000003 | |
| 0x81812248: 12_hssrx_dacap_dacan | 00000201 | 0x8181224c: |
| 13_hssrx_daca_min | 00000000 | |
| 0x81812250: 14_hssrx_adac_ctl | 00000001 | 0x81812254: |
| 15_hssrx_ac_cp_ctl | 000031c3 | |
| 0x81812258: 16_hssrx_ac_cp_val | 00000054 | 0x8181225c: |
| 17_hssrx_dfe_h1h2h3_lcl_off_ch | 00000014 | |
| 0x81812260: 18_hssrx_dfe_h1h2h3_lcl_off_val | 00000000 | 0x81812264: |
| 19_hssrx_peaked_intg | 000000ff | |
| 0x81812268: 1A_hssrx_cdr_analog_sw | 0000ce00 | 0x8181226c: |
| 1B_hssrx_peaking_amp_init_c_PHY | 00000000 | |
| 0x81812270: 1C_hssrx_dac_dpc | 00000040 | 0x81812274: |
| 1D_hssrx_ddc | 00000000 | |
| 0x81812278: 1E_hssrx_int_stat_PHY | 00000c0f | 0x8181227c: |
| 1F_hssrx_dfe_func_ctl1_PHY | 0000ffff | |
| 0x81812280: 20_hssrx_dfe_func_ctl2_INV | 00007eff | 0x81812284: |
| 21_hssrx_ofs_ch_dcc_qcc_idx | 00002000 | |
| 0x81812288: 22_hssrx_dfe_ofs_val | 00007b7f | 0x8181228c: |
| 23_hssrx_h_coeff_bist | 00000401 | |
| 0x81812290: 24_hssrx_ac_cap_bist | 00000000 | 0x81812294: |
| 25_hssrx_max_gain_path_idx_res | 00007800 | |
| 0x81812298: 26_hssrx_loff_ctl | 00000054 | 0x8181229c: |
| 27_hssrx_sigdet_ctl | 00002180 | |
| 0x818122a0: 28_hssrx_ana_ctl_sw | 00000000 | 0x818122a4: |
| 29_hssrx_intg_dac_ofs | 0000acde | |
| 0x818122a8: 2A_hssrx_eye_ctl | 00000000 | 0x818122ac: |
| 2B_hssrx_eye_met | 00000004 | |
| 0x818122b0: 2C_hssrx_eye_met_err_cnt | 00000000 | 0x818122b4: |
| 2D_hssrx_eye_met_pdf_eyec | 00000000 | |
| 0x818122b8: 2E_hssrx_eye_met_pat_len | 0000007f | 0x818122bc: |
| 2F_hssrx_dfe_func_ctl3 | 0000dfff | |
| 0x818122c0: 30_hssrx_dfe_tap_ctl_idx_ptr | 00000008 | 0x818122c4: |
| 31_hssrx_dfe_tap | 00003030 | |
| 0x818122c8: 32_hssrx_lte_ctl_TUNE | 00000600 | 0x818122e4: |
| 39_hssrx_int_stat2 | 000041ff | |
| 0x818122e8: 3A_hssrx_ac_cpl_cur_src_adj | 00000040 | 0x818122ec: |
| 3B_hssrx_dcd_ctl | 00007c42 | |
| 0x818122f0: 3C_hssrx_dcc_ctl | 00000d00 | 0x818122f4: |
| 3D_hssrx_qcc_ctl | 00006942 | |
| 0x818122f8: 3E_hssrx_mac_test_ctl2 | 00000000 | 0x818122fc: |
| 3F_hssrx_mac_test_ctl1 | 00000000 | |
| 0x81812248: 12_hssrx_dacap_dacan[02] | 0200 0201 | |
| 0x81812260: 18_hssrx_dfe_h1h2h3_lcl_off_va[00] | 0000 0000 0000 | |

```

0000 0000 0000 0000 0000
0x81812260: 18_hssrx_dfe_h1h2h3_lcl_off_va[08] 0000 0000 0000
0000 0000 0000 0000 0000
0x81812260: 18_hssrx_dfe_h1h2h3_lcl_off_va[16] 0000 0000 0000
0000 0000
0x81812288: 22_hssrx_dfe_ofs_val[00][00] 7b7f 0000 7b7f
0000 7d7f 0000
0x81812288: 22_hssrx_dfe_ofs_val[03][00] 0379 0000 7d05
007f 057a 7f00
0x81812288: 22_hssrx_dfe_ofs_val[06][00] 7b7f 0000 0679
7f00 0507 7f7f
0x81812288: 22_hssrx_dfe_ofs_val[09][00] 0907 7f7f 017d
0000 077d 7f00
0x81812288: 22_hssrx_dfe_ofs_val[12][00] 0c7d 7f00 0201
0000 0301 0000
0x81812288: 22_hssrx_dfe_ofs_val[15][00] 0307 0000 7c01
0000 7d02 0000
0x81812288: 22_hssrx_dfe_ofs_val[18][00] 0779 7f00 027f
0000 0001 0000
0x81812288: 22_hssrx_dfe_ofs_val[21][00] 0001 0000 0001
0000 0001 0000
0x81812288: 22_hssrx_dfe_ofs_val[24][00] 7d05 007f 077a
7f00 007e 0000
0x81812294: 25_hssrx_max_gain_path_idx_res[00] 005e 0852 1102
1892 20df 289f 3084 3800
0x81812294: 25_hssrx_max_gain_path_idx_res[08] 40bf 488a 5079
5800 6040 6803 7000 7800
0x818122c4: 31_hssrx_dfe_tap[00] fffe 8080 0000
0000 0030 0030 3030 3030
0x818122c4: 31_hssrx_dfe_tap[08] 3030 3030 3030
0000
0x818122e8: 3A_hssrx_ac_cpl_cur_src_adj[00] 0040 0040 0040
0040
0x818122ec: 3B_hssrx_dcd_ctl[00] 7c42 5c00 7c85
5c00 7c81
0x818122f0: 3C_hssrx_dcc_ctl[00] 0d00 0d83 0d81
0d41
0x818122f4: 3D_hssrx_qcc_ctl[00] 6948 6942

```

xfipcs, fec, aec, & aet registers

=====

```

0x81ca0400: xfipcs_reg [00] 00002040 00000080 00000000
00000000 00000001 00000008 00000000 00000000
0x81ca0420: xfipcs_reg [08] 00008401 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81ca0440: xfipcs_reg [16] 00000000 00000000 00000000
00000000 00000040 00000000 00000000 00000000
0x81ca0460: xfipcs_reg [24] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81ca0480: xfipcs_reg [32] 00000004 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81ca0620: fec_32g_128g_reg [08] 00000000 00008003 00000000
00000000 00000000 00000000 00000000
0x81ca0648: fec_32g_128g_reg [18] 00000000 00000000 00000000

```

```

00000000 00000000 00000000 00000000 00000000
0x81ca0a00: aec_reg [00] 00000000 00000000 00000000
00000000 00000040 00000000 00000000 00002490
0x81ca0c00: aet_reg [00] 000000b0 00007000 000008c4
00000000 00000000

```

bbc registers

=====

```

0x81ca1800: bbc_trc 0 0 0 0 0 0 0
0
0x81ca1840: bbc_trc 0 0 0 0 0 0 0
0
0x81ca1880: bbc_trc 0 0 0 0 0 0 0
0
0x81ca18c0: bbc_trc 0 0 0 0 0 0 0
0
0x81ca1900: bbc_trc 0 0 0 0 0 0 0
0
0x81ca1804: bbc_mbc 0 0 0 0 0 0 0
0
0x81ca1844: bbc_mbc 0 0 0 0 0 0 0
0
0x81ca1884: bbc_mbc 0 0 0 0 0 0 0
0
0x81ca18c4: bbc_mbc 0 0 0 0 0 0 0
0
0x81ca1904: bbc_mbc 0 0 0 0 0 0 0
0
0x81ca1a00: bbc_rcc 0 0 0 0 0 0 0
0
0x81ca1a20: bbc_rcc 0 0 0 0 0 0 0
0
0x81ca1a40: bbc_rcc 0 0 0 0 0 0 0
0
0x81ca1a60: bbc_rcc 0 0 0 0 0 0 0
0
0x81ca1a80: bbc_rcc 0 0 0 0 0 0 0
0
0x81ca1c00: bbc_rqc 0 0 0 0 0 0 0
0
0x81ca1c20: bbc_rqc 0 0 0 0 0 0 0
0
0x81ca1c40: bbc_rqc 0 0 0 0 0 0 0
0
0x81ca1c60: bbc_rqc 0 0 0 0 0 0 0
0
0x81ca1c80: bbc_rqc 0 0 0 0 0 0 0
0
0x81ca1d00: bbc_fbpc 00000000 0x81ca1d04: bbc_csc
00000000
0x81ca1d08: bbc_rcc_inc 00000000 0x81ca1d0c:
bbc_rqc_inc 00000000
0x81ca1d10: bbc_fbpc_inc 00000000 0x81ca1d14:
bbc_tmc_inc 00000000

```

| | | |
|-------------------------------------|----------|----------------------|
| 0x81ca1d18: bbc_threshold | 00080100 | 0x81ca1d1c: |
| bbc_counter_clr | 00000000 | |
| 0x81ca1d20: bbc_debug_en | 00000000 | 0x81ca1d24: bbc_ctrl |
| 00200120 | | |
| 0x81ca1d28: bbc_rqc_rcc_thresh | 00000055 | 0x81ca1d34: |
| bbc_bb_sc_n | 00000000 | |
| 0x81ca1d38: bbc_crd_reco_debug | 00000000 | 0x81ca1d3c: |
| bbc_crd_reco_debug_data | 00000000 | |
| 0x81ca1d40: bbc_multi_frm_loss_cnt | 00000000 | 0x81ca1d44: |
| bbc_multi_rdy_loss_cnt | 00000000 | |
| 0x81ca1d48: bbc_1frm_loss_recov_cnt | 00000000 | 0x81ca1d4c: |
| bbc_1rdy_loss_recov_cnt | 00000000 | |
| 0x81ca1d58: bbc_int_status | 00000000 | 0x81ca1d5c: |
| bbc_int_set | 00000000 | |
| 0x81ca1d60: bbc_int_first | 00000000 | 0x81ca1d64: |
| bbc_frm_rdy_rx_err_addr | 00000000 | |
| 0x81ca1d68: bbc_frm_rdy_tx_err_addr | 00000000 | 0x81ca1d6c: |
| bbc_trc_mbc_err_addr | 00000000 | |
| 0x81ca1d70: bbc_frm_rdy_rx_dbl_ecc | 00000000 | 0x81ca1d74: |
| bbc_frm_rdy_tx_dbl_ecc | 00000000 | |
| 0x81ca1d78: bbc_trc_mbc_dbl_ecc | 00000000 | |
| 0x81ca1d7c: bbc_fsm_status | 00001011 | 0x81ca1d80: |
| bbc_force_err | 00000000 | |
| 0x81ca1d84: bbc_crdt_avail0 | 00000000 | 0x81ca1d88: |
| bbc_crdt_avail1 | 00000000 | |
| 0x81ca1d8c: bbc_scratch | 00000000 | |

FPS registers

=====

| | | |
|--------------------------------|----------|-------------|
| 0x81ca0004: fps_er_enc_in | 00000000 | 0x81ca0008: |
| fps_er_crc | 00000000 | |
| 0x81ca000c: fps_er_trunc | 00000000 | 0x81ca0010: |
| fps_er_toolong | 00000000 | |
| 0x81ca0014: fps_er_bad_eof | 00000000 | 0x81ca0018: |
| fps_er_enc_out | 00000000 | |
| 0x81ca001c: fps_er_bad_os | 00000000 | 0x81ca0020: |
| fps_er_flush | 00000000 | |
| 0x81ca0024: fps_er_ifg | 00000000 | 0x81ca0038: |
| fps_er_crc_good_eof | 00000000 | |
| 0x81ca003c: fps_inv_arb | 00000000 | 0x81ca0040: |
| fps_slow_sts_status | 00000000 | |
| 0x81ca0044: fps_tx_frm_cnt | 00000000 | 0x81ca0048: |
| fps_rx_frm_cnt | 00000000 | |
| 0x81ca0050: fps_tx_word_cnt_hi | 00000000 | 0x81ca004c: |
| fps_tx_word_cnt_lo | 00000000 | |
| 0x81ca0058: fps_rx_word_cnt_hi | 00000000 | 0x81ca0054: |
| fps_rx_word_cnt_lo | 00000000 | |

BAL registers

=====

| | | |
|-----------------------------|----------|-------------|
| 0x81ca7000: bal_desired_buf | 00000000 | 0x81ca7004: |
| bal_alloc_buf | 00000000 | |
| 0x81ca7008: bal_busy_buf | 00000000 | 0x81ca700c: |
| bal_usable_buf | 00000000 | |

0x81ca7010: bal_max_bor_buf 00000000
0x81ca7014: bal_busy_buf_thresh 00000002

TXQ registers

=====

0x81ca3004: txq_phys_port_ctl 00440000
0x81ca3050: txq_link_skew 00000000
0x81ca3068: txq_cr_lk_dttm_intr_sts [00] 00000000 00000000
0x81ca3070: txq_cr_lk_dttm_intr_en [00] 00000000 00000000
0x81ca3024: txq_disc_frm_trap_cnt 00000014

FDS registers

=====

0x81ca4000: fds_rxf_ctl 00000002 0x81ca4004:
fds_rxf_wait_thresh 00000909
0x81ca4018: fds_rxf_first_error 00000000 0x81ca401c:
fds_rxf_first_error_info 00000000
0x81ca4020: fds_rxf_inout_pkt_cnt 00000000
0x81ca4008: fds_rxf_err_int_status 00000000 0x81ca4024:
fds_rxf_fifo_status 00888888
0x81ca5000: fds_txf_ctl 0000003a 0x81ca5004:
fds_txf_wait_ifg_thresh 00a00106
0x81ca5008: fds_txf_err_int_status 00000000 0x81ca5024:
fds_txf_fifo_status 00088888
0x81ca502c: fds_txf_bbc_scs 00000000

Logical TXQ registers

=====

0x81ca3000: txq_log_port_ctl 00000002 0x81ca3008:
txq_port_status 00000000
0x81ca300c: txq_todo_flags [00] 00000000 00000000
0x81ca3014: txq_spd_match_desc [00] 00000000 00000000 00000000
00000000
0x81ca3024: txq_spd_match_desc [04] 00000014
0x81ca3028: txq_vc_weight [00] 01010101 01010101 01010101
01010101
0x81ca3038: txq_vc_weight [04] 01010101 01010101 01010101
01010101
0x81ca3048: txq_vc_weight [08] 01010101 00010101
0x81ca3054: txq_cong_dttm_ctrl 00000106
0x81ca3058: txq_cong_dttm_intr_sts [00] 00000000 00000000
0x81ca3060: txq_cong_dttm_intr_en [00] 00000000 00000000
0x81ca3078: txq_bw_limit_en_reg [00] 00000000 00000000
0x81ca3080: txq_bw_gua_en_reg [00] 00000000 00000000
0x81ca3088: txq_vc_group [00] 03030300 03030303 03030303
03030303
0x81ca3098: txq_vc_group [04] 03030303 03030303 03030303
03030303
0x81ca30a8: txq_vc_group [08] 03030303 03030303 00000000
00000000
0x81ca30b0: txq_bw_thresh_group [00] 00000000 00000000 00000000
00000000
0x81ca30c0: txq_bw_thresh_group [04] 00000000 00000000 00000000
00000000

| | | | | |
|---------------------------------|------|----------|----------|----------|
| 0x81ca30d0: txq_bw_thresh_group | [08] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81ca30e0: txq_bw_thresh_group | [12] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81ca30f0: txq_bw_thresh_group | [16] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81ca3100: txq_bw_thresh_group | [20] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81ca3110: txq_bw_thresh_group | [24] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81ca3120: txq_bw_thresh_group | [28] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81ca3130: txq_bw_thresh_group | [32] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81ca3140: txq_bw_thresh_group | [36] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |

txq Congestion detection Statistics RAM

=====

| | | |
|--------------------|----------|--------------------|
| 0x81090c80: vc[0] | 00000000 | 0x81090c84: vc[1] |
| 00000000 | | |
| 0x81090c88: vc[2] | 00000000 | 0x81090c8c: vc[3] |
| 00000000 | | |
| 0x81090c90: vc[4] | 00000000 | 0x81090c94: vc[5] |
| 00000000 | | |
| 0x81090c98: vc[6] | 00000000 | 0x81090c9c: vc[7] |
| 00000000 | | |
| 0x81090ca0: vc[8] | 00000000 | 0x81090ca4: vc[9] |
| 00000000 | | |
| 0x81090ca8: vc[10] | 00000000 | 0x81090cac: vc[11] |
| 00000000 | | |
| 0x81090cb0: vc[12] | 00000000 | 0x81090cb4: vc[13] |
| 00000000 | | |
| 0x81090cb8: vc[14] | 00000000 | 0x81090cbc: vc[15] |
| 00000000 | | |
| 0x81090cc0: vc[16] | 00000000 | 0x81090cc4: vc[17] |
| 00000000 | | |
| 0x81090cc8: vc[18] | 00000000 | 0x81090ccc: vc[19] |
| 00000000 | | |
| 0x81090cd0: vc[20] | 00000000 | 0x81090cd4: vc[21] |
| 00000000 | | |
| 0x81090cd8: vc[22] | 00000000 | 0x81090cdc: vc[23] |
| 00000000 | | |
| 0x81090ce0: vc[24] | 00000000 | 0x81090ce4: vc[25] |
| 00000000 | | |
| 0x81090ce8: vc[26] | 00000000 | 0x81090cec: vc[27] |
| 00000000 | | |
| 0x81090cf0: vc[28] | 00000000 | 0x81090cf4: vc[29] |
| 00000000 | | |
| 0x81090cf8: vc[30] | 00000000 | 0x81090cfc: vc[31] |
| 00000000 | | |
| 0x81090d00: vc[32] | 00000000 | 0x81090d04: vc[33] |
| 00000000 | | |
| 0x81090d08: vc[34] | 00000000 | 0x81090d0c: vc[35] |

```

00000000
0x81090d10: vc[36]      00000000      0x81090d14: vc[37]
00000000
0x81090d18: vc[38]      00000000      0x81090d1c: vc[39]
00000000

```

Logical STS registers

```

=====
0x81584f84: sts_ftb_type1_miss      00000000
0x81584f88: sts_ftb_type2_miss      00000000
0x81584f8c: sts_ftb_type6_miss      00000000
0x81584f90: sts_hard_zoning_miss    00000000
0x81584f94: sts_lun_zoning_miss     00000000
0x81584f9c: sts_unroutable          00000000
0x81581fb4: sts_rte_cl2             00000000      0x81581fb8:
sts_rte_cl3             00000000      0x81581fbc: sts_rte_link_ctl
00000000      0x81584fa8: sts_tx_timeout          00000000

```

Logical STS filter registers

```

=====
0x81584f00: stsflt_trig      [00] 00000000 00000000 00000000
00000000
0x81584f10: stsflt_trig      [04] 00000000 00000000 00000000
00000000
0x81584f20: stsflt_trig      [08] 00000000 00000000 00000000
00000000
0x81584f30: stsflt_trig      [12] 00000000 00000000 00000000
00000000
0x81584f40: stsflt_trig      [16] 00000000 00000000 00000000
00000000
0x81584f50: stsflt_trig      [20] 00000000 00000000 00000000
00000000
0x81584f60: stsflt_trig      [24] 00000000 00000000 00000000
00000000
0x81584f70: stsflt_trig      [28] 00000000 00000000 00000000
00000000
0x81584f80: stsflt_trig      [32]

```

Logical STS discard registers

```

=====
0x81582d10: disc_mcast_wka      00000000      0x81582d14:
disc_inv_did      00000000
0x81582d18: disc_cl1_cl4          00000000      0x81582d1c:
disc_sid_chk_fail 00000000
0x81582d20: disc_inv_dom_egid_txpt 00000000      0x81582d24:
disc_vft_hop_cnt_1 00000000
0x81582d28: disc_classf          00000000      0x81582d2c:
disc_fcp_cdb_inv   00000000
0x81582d30: disc_vfid_trap_enabled 00000000      0x81582d34:
disc_vfid_hdr_chk_fail 00000000
0x81582d38: disc_shim_cksum_fail 00000000      0x81582d3c:
disc_fed_edit_cmd_err 00000000
0x81582d40: disc_ftb_vm_mode      00000000      0x81582d44:

```

```

disc_ftb_agnt2_miss      00000000
0x81582d48: disc_ecb_reserved      00000000      0x81582d4c:
disc_ecb_de_pad_err      00000000
0x81582d50: disc_ecb_de_tag_err      00000000      0x81582d54:
disc_ecb_de_seq_err      00000000
0x81582d58: disc_ecb_err      00000000      0x81582d5c:
disc_ftb_type4_match      00000000
0x81582d60: disc_fcp_rsp_ftb_type4      00000000      0x81582d64:
disc_ftb_type5_match      00000000
0x81582d68: disc_ftb_type3_match      00000000      0x81582d6c:
disc_els_ftb_type3      00000000
0x81582d70: disc_ftb_type1_match      00000000      0x81582d74:
disc_els_rsp_ex_port      00000000
0x81582d78: disc_inv_drp_dps      00000000      0x81582d7c:
disc_did_lookup_miss      00000000
0x81582d80: disc_ftb_type2_match      00000000      0x81582d84:
disc_trpd_plogi_pdisc      00000000
0x81582d88: disc_type2_lookup_miss      00000000      0x81582d8c:
disc_ftb_type6_match      00000000
0x81582d90: disc_els_rep_ex_port      00000000      0x81582d94:
disc_els_sid_lkup_bit1      00000000
0x81582d98: disc_els_sid_lkup_bit0      00000000      0x81582d9c:
disc_bls_frm_trap_bit1      00000000
0x81582da0: disc_ftb_token_err      00000000      0x81582da4:
disc_asic_internal_err      00000000
0x81582da8: disc_hard_zone_miss      00000000      0x81582dac:
disc_lun_zone_miss      00000000
0x81582db0: discflt_frame_disc      00000000      0x81582db4:
discflt_parity_err      00000000
0x81582db8: disc_frame_marked_du      00000000      0x81582dbc:
disc_frame_marked_to      00000000
0x81582dc0: disc_lkup_rte_prty_err      00000000

```

portstatsshow 45

```

stat_wtx      0      4-byte words transmitted
stat_wrx      0      4-byte words received
stat_ftx      0      Frames transmitted
stat_frx      0      Frames received
stat_c2_frx      0      Class 2 frames received
stat_c3_frx      0      Class 3 frames received
stat_lc_rx      0      Link control frames
received
stat_mc_rx      0      Multicast frames
received
stat_mc_to      0      Multicast timeouts
stat_mc_tx      0      Multicast frames
transmitted
tim_txcrd_z      0      Time TX Credit Zero
(2.5Us ticks)
tim_txcrd_z_vc 0- 3: 0      0      0      0
tim_txcrd_z_vc 4- 7: 0      0      0      0
tim_txcrd_z_vc 8-11: 0      0      0      0
tim_txcrd_z_vc 12-15: 0      0      0      0

```

| | | | | | |
|----------------|--------|---|---|---|---|
| lat_tot_pkt_vc | 0- 3: | 1 | 1 | 1 | 1 |
| lat_tot_pkt_vc | 4- 7: | 1 | 1 | 1 | 1 |
| lat_tot_pkt_vc | 8-11: | 1 | 1 | 1 | 1 |
| lat_tot_pkt_vc | 12-15: | 1 | 1 | 1 | 1 |
| lat_hi_time_vc | 0- 3: | 0 | 0 | 0 | 0 |
| lat_hi_time_vc | 4- 7: | 0 | 0 | 0 | 0 |
| lat_hi_time_vc | 8-11: | 0 | 0 | 0 | 0 |
| lat_hi_time_vc | 12-15: | 0 | 0 | 0 | 0 |
| lat_lo_time_vc | 0- 3: | 1 | 1 | 1 | 1 |
| lat_lo_time_vc | 4- 7: | 1 | 1 | 1 | 1 |
| lat_lo_time_vc | 8-11: | 1 | 1 | 1 | 1 |
| lat_lo_time_vc | 12-15: | 1 | 1 | 1 | 1 |
| max_latency_vc | 0- 3: | 1 | 1 | 1 | 1 |
| max_latency_vc | 4- 7: | 1 | 1 | 1 | 1 |
| max_latency_vc | 8-11: | 1 | 1 | 1 | 1 |
| max_latency_vc | 12-15: | 1 | 1 | 1 | 1 |

latency_dma_ts 09-09-2024 UTC Mon 08:47:25 TXQ

Latency DMA TimeStamp

| | | |
|------------------------------|---|-------------------------|
| fec_cor_detected | 0 | Count of blocks that |
| were corrected by FEC | | |
| fec_uncor_detected | 0 | Count of blocks that |
| were left uncorrected by FEC | | |
| er_enc_in | 0 | Encoding errors inside |
| of frames | | |
| er_crc | 0 | Frames with CRC errors |
| er_trunc | 0 | Frames shorter than |
| minimum | | |
| er_toolong | 0 | Frames longer than |
| maximum | | |
| er_bad_eof | 0 | Frames with bad end-of- |
| frame | | |
| er_enc_out | 0 | Encoding error outside |
| of frames | | |
| er_bad_os | 0 | Invalid ordered set |
| er_pcs_blk | 0 | PCS block errors |
| er_rx_c3_timeout | 0 | Class 3 receive frames |
| discarded due to timeout | | |
| er_tx_c3_timeout | 0 | Class 3 transmit frames |
| discarded due to timeout | | |
| er_unroutable | 0 | Frames that are |
| unroutable | | |
| er_unreachable | 0 | Frame with unreachable |
| destination | | |
| er_other_discard | 0 | Other discards |
| er_type1_miss | 0 | frames with FTB type 1 |
| miss | | |
| er_type2_miss | 0 | frames with FTB type 2 |
| miss | | |
| er_type6_miss | 0 | frames with FTB type 6 |
| miss | | |
| er_zone_miss | 0 | frames with hard zoning |
| miss | | |
| er_lun_zone_miss | 0 | frames with LUN zoning |
| miss | | |

```

er_crc_good_eof      0          Crc error with good eof
er_inv_arb           0          Invalid ARB
er_single_credit_loss 0          Single vcrdy/frame loss
on link
er_multi_credit_loss 0          Multiple vcrdy/frame
loss on link
other_credit_loss    0          Link timeout/complete
credit loss
phy_stats_clear_ts   09-06-2024 UTC Fri 08:30:19    Timestamp of
phy_port stats clear
lgc_stats_clear_ts   09-06-2024 UTC Fri 08:30:19    Timestamp of
lgc_port stats clear
fec_corrected_rate   0          FEC Corrected blocks per
second

```

portstats64show 45

```

stat64_wtx           0          top_int : 4-byte words transmitted
                                0          bottom_int : 4-byte words transmitted
stat64_wrx           0          top_int : 4-byte words received
                                0          bottom_int : 4-byte words received
stat64_ftx           0          top_int : Frames transmitted
                                0          bottom_int : Frames transmitted
stat64_frx           0          top_int : Frames received
                                0          bottom_int : Frames received
stat64_c2_frx        0          top_int : Class 2 frames received
                                0          bottom_int : Class 2 frames received
stat64_c3_frx        0          top_int : Class 3 frames received
                                0          bottom_int : Class 3 frames received
stat64_lc_rx         0          top_int : Link control frames received
                                0          bottom_int : Link control frames
received
stat64_mc_rx         0          top_int : Multicast frames received
                                0          bottom_int : Multicast frames received
stat64_mc_to         0          top_int : Multicast timeouts
                                0          bottom_int : Multicast timeouts
stat64_mc_tx         0          top_int : Multicast frames transmitted
                                0          bottom_int : Multicast frames
transmitted
tim64_rdy_pri        0          top_int : Time R_RDY high priority
                                0          bottom_int : Time R_RDY high priority
tim64_txcrd_z        0          top_int : Time BB_credit zero
                                0          bottom_int : Time BB_credit zero
er64_enc_in          0          top_int : Encoding errors inside of
frames
                                0          bottom_int : Encoding errors inside of
frames
er64_crc             0          top_int : Frames with CRC errors
                                0          bottom_int : Frames with CRC errors
er64_trunc           0          top_int : Frames shorter than minimum
                                0          bottom_int : Frames shorter than minimum
er64_toolong         0          top_int : Frames longer than maximum
                                0          bottom_int : Frames longer than maximum
er64_bad_eof         0          top_int : Frames with bad end-of-frame
                                0          bottom_int : Frames with bad end-of-

```

| | | | |
|---|---|--|--|
| frame | | | |
| er64_enc_out | 0 | | top_int : Encoding error outside of |
| frames | | | |
| | 0 | | bottom_int : Encoding error outside of |
| frames | | | |
| er64_disc_c3 | 0 | | top_int : Class 3 frames discarded |
| | 0 | | bottom_int : Class 3 frames discarded |
| er64_pcs_blk | 0 | | top_int : PCS block errors |
| | 0 | | bottom_int : PCS block errors |
| stat64_rateTxFrame | 0 | | Tx frame rate (fr/sec) |
| stat64_rateRxFrame | 0 | | Rx frame rate (fr/sec) |
| stat64_rateTxPeakFrame | 0 | | Tx peak frame rate (fr/sec) |
| stat64_rateRxPeakFrame | 0 | | Rx peak frame rate (fr/sec) |
| stat64_rateTxWord | 0 | | Tx Word rate (words/sec) |
| stat64_rateRxWord | 0 | | Rx Word rate (words/sec) |
| stat64_rateTxPeakWord | 0 | | Tx peak Word rate (words/sec) |
| stat64_rateRxPeakWord | 0 | | Rx peak Word rate (words/sec) |
| stat64_PRJTFrames | 0 | | top_int : Number of PRJT frames |
| returned to this port | | | |
| | 0 | | bottom_int : Number of PRJT |
| frames returned to this port | | | |
| stat64_PBSYFrames | 0 | | top_int : Number of PBSY frames |
| returned to this port | | | |
| | 0 | | bottom_int : Number of PBSY |
| frames returned to this port | | | |
| stat64_inputBuffersFull | 0 | | top_int : Number of occurrences |
| when all input buffers full | | | |
| | 0 | | bottom_int : Number of |
| occurrences when all input buffers full | | | |
| stat64_rxClass1Frames | 0 | | top_int : Number of class 1 |
| frames received | | | |
| | 0 | | bottom_int : Number of class 1 |
| frames received | | | |
| stat64_aveTxFrameSize | 0 | | Average Tx Frame size |
| stat64_aveRxFrameSize | 0 | | Average Rx Frame size |
| Lr_in | 0 | | top_int |
| | 0 | | bottom_int |
| Ols_in | 0 | | top_int |
| | 0 | | bottom_int |
| Lr_out | 0 | | top_int |
| | 0 | | bottom_int |
| Ols_out | 0 | | top_int |
| | 0 | | bottom_int |
| Link_failure | 0 | | top_int |
| | 0 | | bottom_int |
| Invalid_CRC | 0 | | top_int |
| | 0 | | bottom_int |
| Invalid_word | 0 | | top_int |
| | 0 | | bottom_int |
| Protocol_err | 0 | | top_int |
| | 0 | | bottom_int |
| Loss_of_sig | 0 | | top_int |
| | 0 | | bottom_int |
| Loss_of_sync | 0 | | top_int |

```

er_bad_os          0          bottom_int
                   0          top_int : Invalid ordered set
                   0          bottom_int: Invalid ordered set

```

```

portrouteshow 45
port address ID: 0x012d00
external unicast routing table:
  0: Embedded
 255: Embedded
internal unicast routing table:
  0: Embedded

```

```
portcamshow 45
```

```

-----
Port  SID used  DID used  SID entries  DID entries
45    0         0        000000      000000
-----

```

```
ptbufshow, ptcreditshow, ptdatashow, ptstatsshow 45
```

```

S:
S:VF Enable:          1
S:
S:C4 Global Variable:
S:-----
-----
S:trace_stop:        0
S:
S:C4 Phy Data Pointers: c4_phyp = 0xb6add140
S:-----
-----
S:tnodep              0xbb8422a0      pt
   0x43028014
S:proto_phyp          0xb8809d80      phy_cfg
0xb6ade180
S:c4_chp              0x97e28000      c4_lgcp
0x97f98000
S:c4_phy_regp         0x81ca0000      proc_dir
0xb851aa00
S:-----
-----
S:magic_id            0xc4345678      num_port_timer    12
S:prev_if_id         0x43020014      S:ftx              0
   tov              0
S:initialized         1                port_idx           20
S:ui_idx              45                slot_no
   0
S:blade_idx           20                sw_usr_ports       400
S:unused              0                intr_debounced
   0
S:aec_status          0x0              reason_code
   0
S:debug               0x00000004      debug_trc_line     0
S:rxbuf_list_head    0xffffffff      rxbuf_list_tail

```


| | | | |
|------------------------------|------------|-----------------------|-----|
| 0xffffffff | | | |
| S:isAePort | 0 | port_misc_data | |
| | 0 | | |
| S:num_fault1_rx_disc | 0 | num_fault2_rx_disc | 0 |
| S:p_lli_cause0 | 0 | p_sig_regained | 0 |
| S:p_sync_regained | 0 | enc_out | |
| | 0x0 | | |
| S:cached_fps_status | 0 | cached_sts_status | 0 |
| S:cached_er_crc_good_eof | 0 | cached_er_too_long | 0 |
| S:cached_er_bad_os | 0 | | |
| S:cached_er_trunc | 0 | | |
| cached_tot_er_crc_good_eof | 0 | | |
| S:num_pt_excess_intr | 0 | num_no_fid | 0 |
| S:num_fault1_cnt | 0 | num_fault2_cnt | |
| | 0 | | |
| S:num_fault_lip | 0 | num_fault_lli | 0 |
| S:num_fault_rx_fifo | 0 | num_fault_hss | 0 |
| S:num_fault_bwait | 0 | lli_intr_prim | |
| | 0 | | |
| S:num_sw_link_to | 0 | | |
| be_link_err_mon_count | 0 | | |
| S:ecb_enc_enabled | 0 | ecb_comp_enabled | |
| | 0 | | |
| S:ecb_rsv_enc | 0 | ecb_rsv_comp | 0 |
| S:ecb_enc_bm | 0x0 | ecb_key_index | |
| 0xffffffff | | | |
| S:fab_idx | 0 | | |
| S:num_be_lto | 0 | lto_count_reset_intvl | |
| | 0 | | |
| S:lr_count_reset_intvl | 0 | num_be_lr | |
| | 0 | | |
| S:num_fault_qsfm | 0 | check_lto | |
| | 0 | | |
| S:credit_loaded | 0 | num_credit_overrun | |
| | 0 | | |
| S:fec_enabled | 0x0 | fec_los_to_flag | 0x0 |
| S:phy_stats_clear_ts | 1725611419 | pcs_err_online | |
| | 0 | | |
| S:pcs_err_light_det | 0 | pcs_err_ignore | |
| | 0 | | |
| S:pcs_blk_err | 0 | pcs_hiber | 0 |
| S:phy_port_status | 0 | ecb_enc_lr_count | |
| | 0 | | |
| S:dport_mode | 0 | avoid_lto_det | 0 |
| S:sn_debounced | 0x0 | sn_started_kr_reqd | 0 |
| S:major_timer_started | 0x0 | ready_bm | 0x0 |
| S:parln_1_bm | 0x0 | parln_0_bm | 0x0 |
| S:be_los_of_sync_event_intvl | | 0 | |
| be_los_of_sync_event | 0 | | |
| S:errataPtenable_cntr | 0 | errataPoll_cntr | |
| | 0 | | |
| S:jda_rx_sig_loss_det | 0 | jda_rx_sig_loss_cnt | |
| | 0 | | |
| S:encrypt_blk_error | 0 | | |

```

S:
S:      c4_trunk
S:=====
S:mark_ts          0x0          deskew          0x0
S:master_phyp      0x0
S:
S:adelay[00]: 0x00000000 0x00000000 0x00000000 0x00000000
S:adelay[04]: 0x00000000 0x00000000 0x00000000 0x00000000
S:
S:      c4_buf
S:=====
S:tx_csc           0           rx_csc
0
S:ld_vc_credits    0           tx_flag      0x0
S:alloc_buffers    0           req_buffers   0
S:est_buffers      20          ld_use_est    0
S:bb_sc_n          0           rx_bb_sc_n
0
S:data_cr          5           nondata_cr
6
S:cr_enable        0
S:ld_nondata_cr    6           tnodep
0xbb842380
S:tx_credits[0] 0 0 0 0 0 0 0 0
S:tx_credits[8] 0 0 0 0 0 0 0 0
S:tx_credits[16] 0 0 0 0 0 0 0 0 0 0
S:tx_credits[24] 0 0 0 0 0 0 0 0 0 0
S:tx_credits[32] 0 0 0 0 0 0 0 0 0 0
S:rx_credits[0] 0 0 0 0 0 0 0 0
S:rx_credits[8] 0 0 0 0 0 0 0 0
S:rx_credits[16] 0 0 0 0 0 0 0 0 0 0
S:rx_credits[24] 0 0 0 0 0 0 0 0 0 0
S:rx_credits[32] 0 0 0 0 0 0 0 0 0 0
S:tx_mbc[0] 0 0 0 0 0 0 0 0
S:tx_mbc[8] 0 0 0 0 0 0 0 0
S:tx_mbc[16] 0 0 0 0 0 0 0 0
S:tx_mbc[24] 0 0 0 0 0 0 0 0
S:tx_mbc[32] 0 0 0 0 0 0 0 0
S:rx_mbc[0] 0 0 0 0 0 0 0 0
S:rx_mbc[8] 0 0 0 0 0 0 0 0
S:rx_mbc[16] 0 0 0 0 0 0 0 0
S:rx_mbc[24] 0 0 0 0 0 0 0 0
S:rx_mbc[32] 0 0 0 0 0 0 0 0
S:
S:C4 Chip Variables: c4_phyp->c4_chp = 0x97e28000
S:-----
-----
S:version = 2.1
S:magic_id         0xc4234567      init_state      0x8
S:reset_reg_mem    0x1
S:ch_int0_en_bm    0x0          intr0_cause     0x0
S:ch_int1_en_bm    0x0          intr1_cause     0x0
S:ch_int2_en_bm    0x0          intr2_cause     0x0
S:ch               0x43010080      ch_cfg

```

```

0xb7013ba0
S:raslog_hndl.hndl      0x0          obj_halted      0x0
S:c4_chip_regp         0x80000000   c4_fpg_regp
0x81800000
S:num_chip_timer      0x5
S:hi_task_bm          0x0          lo_task_bm      0x0
S:c4_deferq.q_head    0x0          c4_deferq.q_tail 0x0
S:c4_tmrq.q_head      0x0          c4_tmrq.q_tail  0x0
slot_no               0
S:chip_inst           0            chip_idx        0
S:pll_initialized     1            1
pll_serdes_initialized 1
S:init_tries          0            init_ptEnableBM
0xba01b488
S:tick_polling       0xb980c9c0   sec_polling
0xb980c960
S:bb_fid              129
S:ecb_key_bm[0]       0x0          ecb_key_bm[1]   0x0
S:ecb_key_bm[2]       0x0          ecb_key_bm[3]   0x0
S:is_chip_enc_enabled 0
is_chip_comp_enabled  0x0
S:ftb_rsrcp->ftb_flags 0x0          act_rsrcp->act_flag 0x1
S:lue_rsrcp->lue_flags[0] 0x0          lue_rsrcp->
>lue_flags[1] 0x0
S:c4_phyp[00]: 0xb6ab0000 0xb6ab2080 0xb6ab4100 0xb6ab6180
S:c4_phyp[04]: 0xb6ab9040 0xb6abb0c0 0xb6abd140 0xb6ac0000
S:c4_phyp[08]: 0xb6ac2080 0xb6ac4100 0xb6ac6180 0xb6ac9040
S:c4_phyp[12]: 0xb6acb0c0 0xb6acd140 0xb6ad0000 0xb6ad2080
S:c4_phyp[16]: 0xb6ad4100 0xb6ad6180 0xb6ad9040 0xb6adb0c0
S:c4_phyp[20]: 0xb6add140 0xb6ae0000 0xb6ae2080 0xb6ae4100
S:c4_phyp[24]: 0xb6ae6180 0xb6ae9040 0xb6aeb0c0 0xb6aed140
S:c4_phyp[28]: 0xb6af0000 0xb6af2080 0xb6af4100 0xb6af6180
S:c4_phyp[32]: 0xb6af9040 0xb6afb0c0 0xb6afd140 0xb6b00000
S:c4_phyp[36]: 0xb6b02080 0xb6b04100 0xb6b06180 0xb6b09040
S:c4_phyp[40]: 0xb6b0b0c0 0xb6b0d140 0xb6b10000 0xb6b12080
S:c4_phyp[44]: 0xb6b14100 0xb6b16180 0xb6b19040 0xb6b1b0c0
S:c4_phyp[48]: 0xb6b1d140 0xb6b20000 0xb6b22080 0xb6b24100
S:c4_phyp[52]: 0xb6b26180 0xb6b29040 0xb6b2b0c0 0xb6b2d140
S:c4_phyp[56]: 0xb6b30000 0xb6b32080 0xb6b34100 0xb6b36180
S:c4_phyp[60]: 0xb6b39040 0xb6b3b0c0 0xb6b3d140 0xb6b40000
S:c4_lgcp[00]: 0x97f48000 0x97f4c000 0x97f50000 0x97f54000
S:c4_lgcp[04]: 0x97f58000 0x97f5c000 0x97f60000 0x97f64000
S:c4_lgcp[08]: 0x97f68000 0x97f6c000 0x97f70000 0x97f74000
S:c4_lgcp[12]: 0x97f78000 0x97f7c000 0x97f80000 0x97f84000
S:c4_lgcp[16]: 0x97f88000 0x97f8c000 0x97f90000 0x97f94000
S:c4_lgcp[20]: 0x97f98000 0x97f9c000 0x97fa0000 0x97fa4000
S:c4_lgcp[24]: 0x97fa8000 0x97fac000 0x97fb0000 0x97fb4000
S:c4_lgcp[28]: 0x97fb8000 0x97fbc000 0x97fc0000 0x97fc4000
S:c4_lgcp[32]: 0x97fc8000 0x97fcc000 0x97fd0000 0x97fd4000
S:c4_lgcp[36]: 0x97fd8000 0x97fdc000 0x97fe0000 0x97fe4000
S:c4_lgcp[40]: 0x97fe8000 0x97fec000 0x97ff0000 0x97ff4000
S:c4_lgcp[44]: 0x97ff8000 0x97ffc000 0x8e000000 0x8e004000
S:c4_lgcp[48]: 0x8e008000 0x8e00c000 0x8e010000 0x8e014000
S:c4_lgcp[52]: 0x8e018000 0x8e01c000 0x8e020000 0x8e024000

```

```

S:c4_lgcp[56]: 0x8e028000 0x8e02c000 0x8e030000 0x8e034000
S:c4_lgcp[60]: 0x8e038000 0x8e03c000 0x8e040000 0x8e044000
S:chip_timers[00]: 0xb980c720 0xb980c780 0xb980c7e0 0xb980c840
S:chip_timers[04]: 0xb980c8a0 0xb980c900
S:disc_trap_enable_required      0x0                rxlp_disc_log_stop
      0x0
S:curr_rxlp_frm_cnt      0x0                curr_rxlp_disc_frm_cnt  0x0
S:sw_disc_frm_cnt      0x0                last_disc_frm_cnt      0x0
S:txq_nopop_pr_cnt      0x0                pollErrataDfe_ptBM
0xba01b4b0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][0]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][1] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][2]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][0] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][1]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][2] 0x0

```

S:
S:C4 Logical Port Variables

S:-----

```

S:c4_lgc_regp      0x81ca0000
S:c4_phyp:
S:      0xb6add140      0x0                0x0                0x0

S:      0x0                0x0                0x0                0x0

S:master_phyp      0xb6add140      if_id
0x43020014
S:min_phyp      0x0                max_phyp      0x0
S:num_phy_ports      1                lgc_num      20
S:num_iu_to      0                sw_txq_bm
0
S:port_fid      128                unused      0
S:port_group      2                lgc_stats_clear_ts
1725611419
S:domain_tbl_sel      0                area_tbl_sel
0
S:egid_tbl_sel      0
S:serv_lo_bm      0x0

```

S:
S:Proto Phy Variables:

S:-----

```

S:magic_id      0xc4123456      asic_phyp
0xb6add140
S:port_id      0x43028014      phy_cfg
0xb6ade180
S:upsm_hdl      0xb8016140      physm_hdl
0xb8015e60
S:ov_snsn_hdl      0xb8015d20      sw_snsn_hdl
0xb8015dc0
S:ov_lksm_hdl      0xb8015f00      sw_lksm_hdl
0xb8016000
S:trksm_hdl      0xb80160a0      lr_flag      0x0

```

```

S:lr_active          0x0          qsfm_txxrx_rate_sel
    0x0
S:
S:UPSM              UP00: UPST_PORT_DISABLED    --> UP01:
UPST_START_PORT_INIT
S:SNSM(OV)          SN00: OV_SNST_STOPPED        --> SN00: OV_SNST_STOPPED
S:SNSM(SW)          SW00: SW_SNST_STAGE_WS      --> SW00: SW_SNST_STAGE_WS
S:PHYSM             UNKNOWN          --> PP03: PHYST_NO_SIGNAL
S:LKSM(OV)          LK00: OV_LKST_INACTIVE      --> LK00: OV_LKST_INACTIVE
S:LKSM(SW)          SW13: INACTIVE            --> SW13: INACTIVE
S:TRKSM             TRK0: TRKST_INIT          --> TRK0: TRKST_INIT
S:
S:physm variables:
S:-----
-----
S:proto_phyp        0xb8809d80          physm_hdl
0xb8015e60
S:force_offline     0              copper              0
S:fault_reason      0: UNKNOWN
S:phy_media_present 1
S:
S:snsn variables:
S:-----
-----
S:speed             0xff              proto_phyp
0xb8809d80
S:hw_sn_tries_left  0x0              sw_sn_tries_left    0x0
S:curr_txsp_count   0x0
S:tx_max            0x0              curr_tx_indx
    0x0
S:curr_tx           0x0              curr_rxsp_count
    0x0
S:rx_max            0x0              curr_rx_indx
    0x0
S:curr_rx           0x0              rx_mem
    0x0
S:rxsp_rec_count    0x0
S:nc_start          0x0              tx_start            0x0
S:sync_start        0x0              sync_present        0x0
S:diag_auto         0x0              diag_speed          0xff
S:striped_wd_tov    3000              hw_wd_tov
    3000
S:step              0x0              qsfm28_speed_mode
    0x0
S:qsfm_mode0_hw_sn_tries_left  0x0
S:qsfm_mode1_hw_sn_tries_left  0x0
S:
S:lksm variables:
S:-----
-----
S:proto_phyp        0xb8809d80          ov_lksm_hdl
0xb8015f00
sw_lksm_hdl         0xb8016000
num_lf1             0

```

```

S:hw_link_tries_left      0          sw_link_tries_left      0
S:buf_ptype              0x0          stored_entry_state      0x6
S:handshake_owner        0x0          mark_unsent
      0x0
S:busybuf_stuck          0x0          lr_wait                  0x0
S:

```

S:trksm variables:

```

S:-----
-----

```

S:Not a trunk port

S:

S:upsm variables:

```

S:-----
-----

```

```

S:proto_phyph           0xb8809d80    upsm_hdl
0xb8016140
S:bb_credits             0          port_beacon             0
S:port_diag_flag        0          force_offline
      0
S:port_fault_rsn        0: PORT_NO_FAULT
S:retry_init_rsn        0: UNKNOWN
S:linit_reason           0          linit_result            0
S:ie_fctl_mode           0          fec_in_sync_tries_left  0
S:retry_sn_fail_init    0
retry_link_fail_init    0
S:excess_lr_count       0
S:

```

S:c4_ch_cfg

```

S:-----
-----

```

```

S:c4_desc_ring_size     256      292      256      256      292
292      2      292      292
S:thresh_def            0          16         1         0
S:intr_tries            500          cmem_pattern
0xdeadbeef
S:cmem_pattern_upwd     2          cmem_init_time          16
S:cmem_init_tries      5
S:ctrl_par_thresh      2          data_par_thresh
      4
S:cam_par_thresh       4          buf_loss_thresh
      12
S:crit_par_thresh      2          non_crit_par_thresh
      6
S:pci_abort_thresh     10          pci_err_thresh          5
S:excess_chintr_thresh 8          sw_err_thresh           20
S:err_sample_period    300          intr_sleep
20000
S:frame_timeout        2500          proxy_dev                16384
S:vf_route             81920          qos                      2048
S:stats 2048           f_redirect            2048
S:rsp_trap             2048          lun_zoning                20480
S:area_mode            0          ftb_max_loop[0]          0
S:ftb_max_loop[1]      6          ftb_max_loop[2]          9
S:ftb_max_loop[3]      10         ftb_max_loop[4]          10

```

```

S:ftb_max_loop[5]          5          ftb_max_loop[6]          6
S:ftb_seg_size[0]         0          ftb_seg_size[1]
16384
S:ftb_seg_size[2]         65536     ftb_seg_size[3]
16384
S:ftb_seg_size[4]         16384     ftb_seg_size[5]
65536
S:ftb_seg_size[6]         16384     ftb_seg_base[0]          0
S:ftb_seg_base[1]         0          ftb_seg_base[2]
65536
S:ftb_seg_base[3]         16384     ftb_seg_base[4]
32768
S:ftb_seg_base[5]         131072    ftb_seg_base[6]
49152
asic_err_monitor_period1  300
asic_err_monitor_period2 86400
zone_chk_to_poll_period  25
zone_chk_class2_reject_tov 220
S:
S:c4_phy_cfg
S:-----
-----
S:version = 2.1
S:pt          0x43028014     fab_ptr
0x9a800000
S:fabattr          0x9a8000d4     fab_iop
0x9a800050
S:cfgbm          0xbb8420e4     port_ctrl
0xb6ade198
S:pcap.pcap_bm    0x8d215547     pcap.pcap2_bm
0x588289
S:pcap.pcap3_bm    0x1bea60c
ui_idx          45          S:slot_no
0
is_icl          0          S:sw_usr_ports          400
S:neg_speed      0 0 0 0 0 0
S:my_domain      0x1          port_mode          0x0
S:hw_sn_maxtries 100          sw_sn_maxtries
0
S:hw_link_maxtries 10          sw_link_maxtries    5
S:rx_cyc_tov     28          rttov              300
S:bufrdy_tov    300         busybuf_tov        286
S:mark_tov      300         lksm_tov           3000
S:buf_dealloc_wait 4          hw_wd_tov          3000
S:hw_lk_train_tov 540        hw_lk_test_tov
150
S:syswait_tx_12_lips 1          lip_rx_tov          55
S:al_time_tov    15         lp_tov              2000
S:intr_tries_port 500        intr_mod_debounce
250
S:intr_lsrflt_debounce 500       intr_efifo_debounce 100
S:port_no_fid    3          excess_ptintr_thresh 8
S:port_fault1_thresh 100       port_fault1_spur_thresh 250
S:port_fault1_disc_thresh 500

```

```

port_fault1_disc_spur_thresh      1000
S:port_fault2_thresh      5      losync_tov      100
S:port_sw_link_to      15      en_8g_scramble
    1
frc_hw_sn_mode      0x1
S:enc_poll_thresh      0      fec_enable
    0
S:fec_in_sync_to      50      fec_in_sync_try_max
    4
S:port_be_lto_threshold      100      port_be_lr_threshold
    2
S:be_cr_in_sync_to      5
port_credit_overrun_thresh      10
S:jda_sfp_losig_tov      400
jda_sfp_losig_try_max      30
S:striped_wd_tov      3000
no_sync_debounce      1200
S:
S:      fab_iop
S:=====
S:fab_iop->interop_mode 0x0      fab_iop->lab_mode      0x0
S:fab_iop->fl_bbc      0x0      fab_iop->fl_fan
    0x0
S:fab_iop->fl_cls      0x4      fab_iop->fl_rscn
    0x0
S:fab_iop->domain_id_offset      0x60      fab_iop-
>mcmt_fabric_mode      0x0
S:fab_iop->mcmt_default_zone      0x0      fab_iop-
>mcmt_safe_zone      0x0
S:
S:      port_ctrl
S:=====
S:port_ctrl.port_type      1      port_ctrl.port_grp      2
S:port_ctrl.port_number 45      port_ctrl.vc_mode      1
S:
S:      port_ctrl.lcap
S:=====
S:has_serdes      0      has_media      1
S:topology      1      skip_nego      0
S:skip_pnego      0      skip_init_event      0
S:en_shim      0      speed_neg
    1
S:loop_back      0      num_speeds      5
S:fec_enable      0
S:
S:      port_ctrl.speed_list array
S:=====
S:speed_list[0].auto_neg 1      speed_list[0].lnk_speed 0x0000000a
S:speed_list[1].auto_neg 1      speed_list[1].lnk_speed 0x00000008
S:speed_list[2].auto_neg 0      speed_list[2].lnk_speed 0x00000006
S:speed_list[3].auto_neg 1      speed_list[3].lnk_speed 0x00000005
S:speed_list[4].auto_neg 0      speed_list[4].lnk_speed 0x00000003
S:speed_list[5].auto_neg 0      speed_list[5].lnk_speed 0x00000000
S:

```



```

S:      port_ctrl.cm
S:=====
S:port_ctrl.cm.num_vcs          8
S:port_ctrl.cm.min_bufs        8
S:port_ctrl.cm.cr_shar_bufs    0
S:port_ctrl.vc_alloc
S:port_ctrl.vc_alloc          2 0 1 1 1 1 1 1
S:port_ctrl.vc_alloc          0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.norm_vc_alloc
S:port_ctrl.norm_vc_alloc     4 0 5 5 5 5 1 1
S:port_ctrl.norm_vc_alloc     0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.cm.skip_bb_credit      0
S:port_ctrl.cm.use_shim_based_sublist 0
S:
S:      port_ctrl.serdes_set
S:=====
S:serdes_type          0x8
S:serdes_data_t.ibm_hss_serdes.tx_drive_power      0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b_sign 0x1
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b      0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_a      0x0
S:serdes_data_t.ibm_hss_serdes.rxeq                0x0
S:
S:      cfgbm
S:=====
S:old_distance          0x0          gport_lockdown      0x0
S:tport                 0x1          speed                0x0
S:disable_eport         0x0          fcacc                0x0
S:lport_lockdown        0x0          priv_lport_lockdown
0x0
S:vcxlt_linit           0x0          delay_flogi          0x0
S:isl_interop           0x0          distance              0x0
S:BufStarvFlag          0x0          credit_sharing       0x0
S:lport_halfduplex      0x0          lport_fairness       0x0
S:soft_neg              0x0          asn_frc_hwretry      0x0
S:cr_recov              0x0          fport_buffers        0x0
S:export                0x0          export_mode
0x0
S:csctl_en              0x0          mirror_port          0x0
S:fault_delay           0x0          non_dfe              0x0
S:fec_configured*(0=ENAB) 0          fec_tts
0
S:port_persistently_disabled (permanently) 0 (0)
S:
S:      cfg property
S:=====
S:priv_pcfg_bm          0x00000000    lgcl_pcfg_bm
0xbb842124
S:fport_buffer          0x00000000
S:
S:
S:C4 Discard Cntrs: rxlp_stats = 0xb6add4f0

```

```

S:-----
-----
S:disc_mcast_wka          0x0          disc_inv_did          0x0
S:disc_cl1_cl4           0x0          disc_sid_chk_fail     0x0
S:disc_inv_dom_egid_txpt 0x0          disc_vft_hop_cnt_1
  0x0
S:disc_classf            0x0          disc_fcp_cdb_inv      0x0
S:disc_vfid_trap_enabled 0x0
disc_vfid_hdr_chk_fail  0x0
S:disc_shim_cksum_fail   0x0          disc_fed_edit_cmd_err 0x0
S:disc_shim_cksum_fail   0x0          disc_fed_edit_cmd_err 0x0
S:disc_ftb_vm_mode       0x0          disc_ftb_agnt2_miss   0x0
S:disc_ecb_de_pad_err    0x0          disc_ecb_de_tag_err   0x0
S:disc_ecb_de_seq_err    0x0          disc_ecb_err           0x0
S:disc_ftb_type4_match   0x0          disc_fcp_rsp_ftb_type4 0x0
S:disc_fcp_rsp_ftb_type4 0x0          disc_ftb_type5_match
  0x0
S:disc_ftb_type3_match   0x0          disc_els_ftb_type3    0x0
S:disc_ftb_type1_match   0x0          disc_els_rsp_ex_port   0x0
S:disc_inv_drp_dps       0x0          disc_did_lookup_miss   0x0
S:disc_ftb_type2_match   0x0          disc_trpd_plogi_pdisc  0x0
S:disc_type2_lookup_miss 0x0          disc_ftb_type6_match
  0x0
S:disc_els_rep_ex_port   0x0          disc_els_sid_lkup_bit1 0x0
S:disc_els_sid_lkup_bit0 0x0
disc_bls_frm_trap_bit1  0x0
S:disc_ftb_token_err     0x0          disc_asic_internal_err 0x0
S:disc_hard_zone_miss    0x0          disc_lun_zone_miss     0x0
S:discflt_frame_disc     0x0          discflt_parity_err     0x0
S:disc_frame_marked_du   0x0          disc_frame_marked_to   0x0
E:Connection type: FE
E:Port type: F_port
E:Trunk port: No
E:Configured Speed: AUTO_SPEED_NEGO
E:Max Capable Speed: 32G
E:Current SNSM Speed: UNDEFINED
E:Hardware TX Speed: 32G (0x00000004)
E:Hardware RX Speed: 32G (0x00000040)
E:
E:Interrupts: 0          Link_failure: 0
Loss_of_sync: 0          Loss_of_sig: 0
E:Lli: 0                 Invalid_word: 0
E:trapped_frm: 0         fwd_status_ok: 0
E:fwd_timeout: 0         fwd_tx_unavail: 0
E:fwd_unroutable: 0     fwd_zone_out: 0
E:fwd_other_err: 0       frm_err_discard: 0
E:Fltr listA: 0          Fltr listB: 0
E:Zone trap fwd: 0       Zone trap disc: 0
E:shim_csum: 0           RTE_perr: 0
E:Invalid_crc: 0         Delim_err: 0
E:Protocol_err: 0
E:Lr_in: 0               Lr_out: 0
E:Ols_in: 0              Ols_out: 0

```

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FILTER DATA

Shadow settings:

Filter Enable: 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass: 0x00000000

Real settings:

Enable RAM: 0x00000000, 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000

Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass RAM: 0x00000000

Shadowed filters:

Filter 0: Not Installed (MIRROR1)(LISTA)
c4_fldenable[0] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[0] = 0x00000000,c4_fltr_config[0] = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
c4_fldenable[1] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[1] = 0x00000000,c4_fltr_config[1] = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
c4_fldenable[2] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[2] = 0x00000000,c4_fltr_config[2] = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
c4_fldenable[3] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[3] = 0x00000000,c4_fltr_config[3] = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
c4_fldenable[4] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[4] = 0x00000000,c4_fltr_config[4] = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
c4_fldenable[5] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[5] = 0x00000000,c4_fltr_config[5] = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
c4_fldenable[6] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[6] = 0x00000000,c4_fltr_config[6] = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
c4_fldenable[7] = 0x00000000 0x00000000 0x00000000

```
0x00000000
    c4_fldnegate[7] = 0x00000000,c4_fltr_config[7] = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
    c4_fldenable[8] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[8] = 0x00000000,c4_fltr_config[8] = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
    c4_fldenable[9] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[9] = 0x00000000,c4_fltr_config[9] = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
    c4_fldenable[10] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[10] = 0x00000000,c4_fltr_config[10] =
0x00000000
Filter 11: Not Installed (SIM)(LISTA)
    c4_fldenable[11] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[11] = 0x00000000,c4_fltr_config[11] =
0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
    c4_fldenable[12] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[12] = 0x00000000,c4_fltr_config[12] =
0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
    c4_fldenable[13] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[13] = 0x00000000,c4_fltr_config[13] =
0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
    c4_fldenable[14] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[14] = 0x00000000,c4_fltr_config[14] =
0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
    c4_fldenable[15] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[15] = 0x00000000,c4_fltr_config[15] =
0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
    c4_fldenable[16] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[16] = 0x00000000,c4_fltr_config[16] =
0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
    c4_fldenable[17] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[17] = 0x00000000,c4_fltr_config[17] =
0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
    c4_fldenable[18] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[18] = 0x00000000,c4_fltr_config[18] =
```

```
0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
    c4_fldenable[19] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[19] = 0x00000000,c4_fltr_config[19] =
0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
    c4_fldenable[20] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[20] = 0x00000000,c4_fltr_config[20] =
0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
    c4_fldenable[21] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[21] = 0x00000000,c4_fltr_config[21] =
0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
    c4_fldenable[22] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[22] = 0x00000000,c4_fltr_config[22] =
0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
    c4_fldenable[23] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[23] = 0x00000000,c4_fltr_config[23] =
0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
    c4_fldenable[24] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[24] = 0x00000000,c4_fltr_config[24] =
0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
    c4_fldenable[25] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[25] = 0x00000000,c4_fltr_config[25] =
0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
    c4_fldenable[26] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[26] = 0x00000000,c4_fltr_config[26] =
0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
    c4_fldenable[27] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[27] = 0x00000000,c4_fltr_config[27] =
0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
    c4_fldenable[28] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[28] = 0x00000000,c4_fltr_config[28] =
0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
    c4_fldenable[29] = 0x00000000 0x00000000 0x00000000
0x00000000
```

```
    c4_fldnegate[29] = 0x00000000,c4_fltr_config[29] =
0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    c4_fldenable[30] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[30] = 0x00000000,c4_fltr_config[30] =
0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    c4_fldenable[31] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[31] = 0x00000000,c4_fltr_config[31] =
0x00000000
```

Real filters:

```
Filter 0: Not Installed (MIRROR1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
```

0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 11: Not Installed (SIM)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 23: Not Installed (PERF8)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter dirty indicator: 0x00000000
Performance filters: 0
Port Mirror filters: 0 (0x0)

FIELD DATA

Shadowed fields:

fldoffset[0] = 0x00, fldmask[0] = 0x00, fldvalue_dyna[0]: 0x00 0x00
0x00 0x00
fldcontrol[0].inuse = 0x0 fldcontrol[0].refcnt = 0x00 0x00 0x00
0x00
fldoffset[1] = 0x00, fldmask[1] = 0x00, fldvalue_dyna[1]: 0x00 0x00
0x00 0x00
fldcontrol[1].inuse = 0x0 fldcontrol[1].refcnt = 0x00 0x00 0x00

```
0x00
fldoffset[2] = 0x00, fldmask[2] = 0x00, fldvalue_dyna[2]:0x00 0x00
0x00 0x00
fldcontrol[2].inuse = 0x0 fldcontrol[2].refcnt = 0x00 0x00 0x00
0x00
fldoffset[3] = 0x00, fldmask[3] = 0x00, fldvalue_dyna[3]:0x00 0x00
0x00 0x00
fldcontrol[3].inuse = 0x0 fldcontrol[3].refcnt = 0x00 0x00 0x00
0x00
fldoffset[4] = 0x00, fldmask[4] = 0x00, fldvalue_dyna[4]:0x00 0x00
0x00 0x00
fldcontrol[4].inuse = 0x0 fldcontrol[4].refcnt = 0x00 0x00 0x00
0x00
fldoffset[5] = 0x00, fldmask[5] = 0x00, fldvalue_dyna[5]:0x00 0x00
0x00 0x00
fldcontrol[5].inuse = 0x0 fldcontrol[5].refcnt = 0x00 0x00 0x00
0x00
fldoffset[6] = 0x00, fldmask[6] = 0x00, fldvalue_dyna[6]:0x00 0x00
0x00 0x00
fldcontrol[6].inuse = 0x0 fldcontrol[6].refcnt = 0x00 0x00 0x00
0x00
fldoffset[7] = 0x00, fldmask[7] = 0x00, fldvalue_dyna[7]:0x00 0x00
0x00 0x00
fldcontrol[7].inuse = 0x0 fldcontrol[7].refcnt = 0x00 0x00 0x00
0x00
fldoffset[8] = 0x00, fldmask[8] = 0x00, fldvalue_dyna[8]:0x00 0x00
0x00 0x00
fldcontrol[8].inuse = 0x0 fldcontrol[8].refcnt = 0x00 0x00 0x00
0x00
fldoffset[9] = 0x00, fldmask[9] = 0x00, fldvalue_dyna[9]:0x00 0x00
0x00 0x00
fldcontrol[9].inuse = 0x0 fldcontrol[9].refcnt = 0x00 0x00 0x00
0x00
fldoffset[10] = 0x00, fldmask[10] = 0x00, fldvalue_dyna[10]:0x00 0x00
0x00 0x00
fldcontrol[10].inuse = 0x0 fldcontrol[10].refcnt = 0x00 0x00 0x00
0x00
fldoffset[11] = 0x00, fldmask[11] = 0x00, fldvalue_dyna[11]:0x00 0x00
0x00 0x00
fldcontrol[11].inuse = 0x0 fldcontrol[11].refcnt = 0x00 0x00 0x00
0x00
fldoffset[12] = 0x00, fldmask[12] = 0x00, fldvalue_dyna[12]:0x00 0x00
0x00 0x00
fldcontrol[12].inuse = 0x0 fldcontrol[12].refcnt = 0x00 0x00 0x00
0x00
fldoffset[13] = 0x00, fldmask[13] = 0x00, fldvalue_dyna[13]:0x00 0x00
0x00 0x00
fldcontrol[13].inuse = 0x0 fldcontrol[13].refcnt = 0x00 0x00 0x00
0x00
fldoffset[14] = 0x00, fldmask[14] = 0x00, fldvalue_dyna[14]:0x00 0x00
0x00 0x00
fldcontrol[14].inuse = 0x0 fldcontrol[14].refcnt = 0x00 0x00 0x00
0x00
fldoffset[15] = 0x00, fldmask[15] = 0x00, fldvalue_dyna[15]:0x00 0x00
```

```
0x00 0x00
fldcontrol[15].inuse = 0x0  fldcontrol[15].refcnt = 0x00 0x00 0x00
0x00
fldoffset[16] = 0x00,fldmask[16] = 0x00,fldvalue_dyna[16]:0x00 0x00
0x00 0x00
fldcontrol[16].inuse = 0x0  fldcontrol[16].refcnt = 0x00 0x00 0x00
0x00
fldoffset[17] = 0x00,fldmask[17] = 0x00,fldvalue_dyna[17]:0x00 0x00
0x00 0x00
fldcontrol[17].inuse = 0x0  fldcontrol[17].refcnt = 0x00 0x00 0x00
0x00
fldoffset[18] = 0x00,fldmask[18] = 0x00,fldvalue_dyna[18]:0x00 0x00
0x00 0x00
fldcontrol[18].inuse = 0x0  fldcontrol[18].refcnt = 0x00 0x00 0x00
0x00
fldoffset[19] = 0x00,fldmask[19] = 0x00,fldvalue_dyna[19]:0x00 0x00
0x00 0x00
fldcontrol[19].inuse = 0x0  fldcontrol[19].refcnt = 0x00 0x00 0x00
0x00
```

Real fields:

```
fldoffset RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000
fldmask RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000
fld value4 RAM:
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
Field dirty indicator: 0x00000000
```

```
FDB reference count fdb: 0 [0 0 0 0 ]
FDB reference count fdb: 1 [0 0 0 0 ]
FDB reference count fdb: 2 [0 0 0 0 ]
FDB reference count fdb: 3 [0 0 0 0 ]
FDB reference count fdb: 4 [0 0 0 0 ]
```

FDB reference count fdb: 5 [0 0 0 0]
FDB reference count fdb: 6 [0 0 0 0]
FDB reference count fdb: 7 [0 0 0 0]
FDB reference count fdb: 8 [0 0 0 0]
FDB reference count fdb: 9 [0 0 0 0]
FDB reference count fdb: 10 [0 0 0 0]
FDB reference count fdb: 11 [0 0 0 0]
FDB reference count fdb: 12 [0 0 0 0]
FDB reference count fdb: 13 [0 0 0 0]
FDB reference count fdb: 14 [0 0 0 0]
FDB reference count fdb: 15 [0 0 0 0]
FDB reference count fdb: 16 [0 0 0 0]
FDB reference count fdb: 17 [0 0 0 0]
FDB reference count fdb: 18 [0 0 0 0]
FDB reference count fdb: 19 [0 0 0 0]

Filter counters:

Filter counter 0: 0 (MIRROR1)
Filter counter 1: 0 (MIRROR2)
Filter counter 2: 0 (MIRROR3)
Filter counter 3: 0 (MIRROR4)
Filter counter 4: 0 (AEPORT_NON_MIRR_DROP)
Filter counter 5: 0 (ZONING TRAP)
Filter counter 6: 0 (FCR_EXPORT_DC)
Filter counter 7: 0 (TIN TRAP)
Filter counter 8: 0 (FICON CUP)
Filter counter 9: 0 (FICON CUP DST)
Filter counter 10: 0 (WELL KNOWN ADDR)
Filter counter 11: 0 (SIM)
Filter counter 12: 0 (UNUSED)
Filter counter 13: 0 (UNUSED)
Filter counter 14: 0 (UNUSED)
Filter counter 15: 0 (UNUSED)
Filter counter 16: 0 (PERF1)
Filter counter 17: 0 (PERF2)
Filter counter 18: 0 (PERF3)
Filter counter 19: 0 (PERF4)
Filter counter 20: 0 (PERF5)
Filter counter 21: 0 (PERF6)
Filter counter 22: 0 (PERF7)
Filter counter 23: 0 (PERF8)
Filter counter 24: 0 (PERF9)
Filter counter 25: 0 (PERF10)
Filter counter 26: 0 (PERF11)
Filter counter 27: 0 (PERF12)
Filter counter 28: 0 (OPM1)
Filter counter 29: 0 (OPM2)
Filter counter 30: 0 (IPM1)
Filter counter 31: 0 (IPM2)

ACL DATA

Logical port 20: Hard Zoning disabled, Soft Zoning disabled
Zone type: WWN Zoning

Frames with hard zone miss: 0

*** Please use filterportshow on user port 56 to display ACL hash tables and Mirroring resources of thischip.

***We show this data only for the first physical port which is an external port.

portFcPortCmdShow --slot 0 46 3
doing portFcPortCmdShow: arg1 = 3, arg2 = -2

portshow 46
portDisableReason: None
portCFlags: 0x1
portFlags: 0x1 PRESENT U_PORT
LocalSwcFlags: 0x0
portType: 26.0
POD Port: Port is licensed
portState: 2 Offline
Protocol: FC
portPhys: 4 No_Light portScn: 2 Offline
port generation number: 0
state transition count: 1

portId: 012e00
portIfId: 43020013
portWwn: 20:2e:d8:1f:cc:2c:99:90
portWwn of device(s) connected:
16b Area list:
Distance: normal
portSpeed: N32Gbps

FEC: Inactive
Credit Recovery: Inactive
LE domain: 0
Peer beacon: Off
FC Fastwrite: OFF

| | | | | |
|-------------|---|---------------|---|-------|
| Interrupts: | 0 | Link_failure: | 0 | Frjt: |
| 0 | | | | |
| Unknown: | 0 | Loss_of_sync: | 0 | Fbsy: |
| 0 | | | | |
| Lli: | 0 | Loss_of_sig: | 0 | |
| Proc_rqrd: | 0 | Protocol_err: | 0 | |
| Timed_out: | 0 | Invalid_word: | 0 | |
| Tx_unavail: | 0 | Invalid_crc: | 0 | |
| Delim_err: | 0 | Address_err: | 0 | |
| Lr_in: | 0 | Ols_in: | 0 | |
| Lr_out: | 0 | Ols_out: | 0 | |

portloginshow 46
Type PID World Wide Name credit df_sz cos
=====

portloginshow 46 -history

| Type | PID | World Wide Name | logout time |
|------|-----|-----------------|-------------|
|------|-----|-----------------|-------------|

=====

portregshow 46

LED registers

=====

| | | |
|---------------------------|----------|-------------|
| 0x81c9a000: c4_led_status | 00000000 | 0x81c9a004: |
| c4_led_ctl | 00000000 | |

FPL registers

=====

| | | |
|---------------------------------|----------|-------------|
| 0x81c98200: fpl_port_config | 23298002 | |
| 0x81c9820c: fpl_port_id_ctl | 00000000 | 0x81c98210: |
| fpl_port_id_addr | 00012e00 | |
| 0x81c98214: fpl_port_speed | 00000004 | 0x81c9821c: |
| fpl_lli_ctl | 00000100 | |
| 0x81c98228: fpl_lli_os_ctl | bc94ffff | 0x81c9822c: |
| fpl_lli_send_word | bc95b5b5 | |
| 0x81c98230: fpl_lli_mark_rx | 00000000 | 0x81c98234: |
| fpl_lli_rnd_trip_time | 00000000 | |
| 0x81c98238: fpl_lli_ns_status | 00130007 | 0x81c9823c: |
| fpl_lli_intr_status | 00030007 | |
| 0x81c98244: fpl_lli_def | 00100000 | 0x81c98254: |
| fpl_lli_intr_enable_clr | 001c0000 | |
| 0x81c98258: fpl_err_intr_status | 00000000 | 0x81c98260: |
| fpl_err_intr_enable_clr | 00000000 | |
| 0x81c98268: fpl_err_first_error | 00000000 | 0x81c9826c: |
| fpl_speed_neg_ctl | 00000000 | |
| 0x81c98270: fpl_speed_neg_stat | 00000000 | 0x81c98274: |
| fpl_softasn_ctl | 0000000f | |
| 0x81c98278: fpl_link_init_ctl | 00000000 | 0x81c9827c: |
| fpl_link_init_stat | 00000000 | |
| 0x81c98280: fpl_aec_ctl | 001c1060 | 0x81c98284: |
| fpl_aec_ctl2 | 04009f60 | |
| 0x81c98288: fpl_pcs_ctl | 00000170 | 0x81c9828c: |
| fpl_fec_ctl | 00000424 | |
| 0x81c98290: fpl_fec_cor | 00000000 | 0x81c98294: |
| fpl_fec_uncor | 00000000 | |
| 0x81c98298: fpl_hss_link_ctl | 0031f040 | 0x81c9829c: |
| fpl_afifo_link_ctl | 00000a86 | |
| 0x81c982a0: fpl_echo_lb_ctl | 0000028c | 0x81c982a4: |
| fpl_scratch | 00000121 | |
| 0x81c982a8: fpl_debug | 00060005 | 0x81c982ac: |
| fpl_misc_debug | 00000800 | |
| 0x00000000: SW_shadow_reg | 00000000 | 0x00000000: |
| SW_c4_phyp->cfgptr | 00030003 | |

per-fpg (per octet) registers

=====

| | | |
|------------------------------|----------|-------------|
| 0x8181382c: fpg_serdes_ctla0 | 81a37be7 | 0x81813830: |
| fpg_serdes_ctla1 | 81a37be7 | |

```

0x81813834: fpg_serdes_ctlb0      81a1c3c3    0x81813838:
fpg_serdes_ctlb1      81a1c3c3
0x8181383c: fpg_serdes_xgmii_1ms    00067c28    0x81813840:
fpg_serdes_regtimctl  40e47946
0x81813844: fpg_serdes_asnrsttimctl 00000102

```

HSS PLL registers

=====

```

0x81811400: 00_hssplla_vco_coarse_cal0    00000000    0x81811404:
01_hssplla_vco_coarse_cal1    00000014
0x81811408: 02_hssplla_vco_coarse_cal2    00000000    0x8181140c:
03_hssplla_vco_coarse_cal3    00000000
0x81811410: 04_hssplla_vco_coarse_cal4    00000000    0x81811424:
09_hssplla_power_ctl          00000000
0x81811428: 0A_hssplla_charge_pump_ctl     00000004    0x81811438:
0E_hssplla_pll_misc_ctl      00000000
0x8181143c: 0F_hssplla_pclk_ctl           000000f8    0x81811440:
10_hssplla_eyem_intv_ctl     00000000
0x81811444: 11_hssplla_eyem_intv_lim1     00000000    0x81811448:
12_hssplla_eyem_intv_lim2     00000000
0x8181144c: 13_hssplla_eyem_intv_lim3     00000000    0x81811450:
14_hssplla_eyem_intv_lim4     00000000
0x818114f0: 3C_hssplla_macro_tst_ctl4     00000000    0x818114f4:
3D_hssplla_macro_tst_ctl3     00000000
0x818114f8: 3E_hssplla_macro_tst_ctl2     00000000    0x818114fc:
3F_hssplla_macro_tst_ctl1     00000000
0x81811500: 00_hssppll_vco_coarse_cal0    0000000a    0x81811504:
01_hssppll_vco_coarse_cal1    00000014
0x81811508: 02_hssppll_vco_coarse_cal2    00000000    0x8181150c:
03_hssppll_vco_coarse_cal3    00000000
0x81811510: 04_hssppll_vco_coarse_cal4    00000000    0x81811524:
09_hssppll_power_ctl          00000000
0x81811528: 0A_hssppll_charge_pump_ctl     00000004    0x81811538:
0E_hssppll_pll_misc_ctl      00000000
0x8181153c: 0F_hssppll_pclk_ctl           000000f8    0x81811540:
10_hssppll_eyem_intv_ctl     00000000
0x81811544: 11_hssppll_eyem_intv_lim1     00000000    0x81811548:
12_hssppll_eyem_intv_lim2     00000000
0x8181154c: 13_hssppll_eyem_intv_lim3     00000000    0x81811550:
14_hssppll_eyem_intv_lim4     00000000
0x818115f0: 3C_hssppll_macro_tst_ctl4     00000000    0x818115f4:
3D_hssppll_macro_tst_ctl3     00000000
0x818115f8: 3E_hssppll_macro_tst_ctl2     00000000    0x818115fc:
3F_hssppll_macro_tst_ctl1     00000000

```

HSS TX registers

=====

```

0x81810500: 00_hsstx_cfg_mode_PHY         00009f48    0x81810504:
01_hsstx_test_ctl            00000000
0x81810508: 02_hsstx_coeff_ctl_INV        00000000    0x8181050c:
03_hsstx_drv_mode_ctl        00000000
0x81810510: 04_hsstx_drv_ovrd_ctl         00000010    0x81810514:
05_hsstx_dclk_align_ovrd     00000080
0x81810518: 06_hsstx_imp_cal_ovrd         00000c0c    0x8181051c:

```

| | | | |
|---|----------|-------------|--|
| 07_hsstx_dclk_drift_tol | 00000004 | | |
| 0x81810520: 08_hsstx_tap0_coeff_TUNE | 00000000 | 0x81810524: | |
| 09_hsstx_tap1_coeff_TUNE | 00000003 | | |
| 0x81810528: 0A_hsstx_tap2_coeff_TUNE | 00000019 | 0x8181052c: | |
| 0B_hsstx_tap3_coeff_TUNE | 00000003 | | |
| 0x81810534: 0D_hsstx_pol_INV | 00000004 | 0x81810538: | |
| 0E_hsstx_ae_cmd | 00000000 | | |
| 0x8181053c: 0F_hsstx_ae_stat | 00000000 | 0x81810540: | |
| 10_hsstx_ae_tap0_TUNE | 00000000 | | |
| 0x81810544: 11_hsstx_ae_tap1_TUNE | 00000000 | 0x81810548: | |
| 12_hsstx_ae_tap2_TUNE | 00000028 | | |
| 0x8181054c: 13_hsstx_ae_tap3_TUNE | 00000000 | 0x81810554: | |
| 15_hsstx_app_tune | 0000120e | | |
| 0x81810558: 16_hsstx_analog_diag | 00000000 | 0x81810560: | |
| 18_hsstx_4x_seg_app | 0000aa00 | | |
| 0x81810564: 19_hsstx_2x_seg_app | 000000aa | 0x81810568: | |
| 1A_hsstx_1x_seg_app | 0000f5e4 | | |
| 0x8181056c: 1B_hsstx_seg_4x_term_app | 0000000f | 0x81810570: | |
| 1C_hsstx_seg_2x1x_term_app | 00000001 | | |
| 0x81810574: 1D_hsstx_tap_sign_app | 00000004 | 0x81810578: | |
| 1E_hsstx_ext_addr_data | 00000001 | | |
| 0x8181057c: 1F_hsstx_ext_addr_addr | 00000000 | 0x81810580: | |
| 20_hsstx_pat_buf_bytes_1_0 | 00000000 | | |
| 0x81810584: 21_hsstx_pat_buf_bytes_3_2 | 00000000 | 0x81810588: | |
| 22_hsstx_pat_buf_bytes_5_4 | 00000000 | | |
| 0x8181058c: 23_hsstx_pat_buf_bytes_7_6 | 00000000 | 0x8181059c: | |
| 27_hsstx_8023az_ctl | 00000000 | | |
| 0x818105a0: 28_hsstx_dcc_ctl | 000060c0 | 0x818105a4: | |
| 29_hsstx_dcc_ovrd | 00001000 | | |
| 0x818105a8: 2A_hsstx_dcc_app | 00000106 | 0x818105ac: | |
| 2B_hsstx_dcc_timeout | 0000ffff | | |
| 0x818105c0: 30_hsstx_tap_sign_ovrd | 00000000 | 0x818105c8: | |
| 32_hsstx_seg_4x_ovrd | 00000000 | | |
| 0x818105cc: 33_hsstx_seg_2x_ovrd | 00000000 | 0x818105d0: | |
| 34_hsstx_seg_1x_ovrd | 00000000 | | |
| 0x818105d8: 36_hsstx_tap_seg_4x_term_ovrd | 00000000 | 0x818105dc: | |
| 37_hsstx_tap_seg_2x_term_ovrd | 00000000 | | |
| 0x818105e0: 38_hsstx_tap_seg_1x_term_ovrd | 00000000 | 0x818105ec: | |
| 3B_hsstx_mac_test_ctl5 | 00000000 | | |
| 0x818105f0: 3C_hsstx_mac_test_ctl4 | 00000000 | 0x818105f4: | |
| 3D_hsstx_mac_test_ctl3 | 00000000 | | |
| 0x818105f8: 3E_hsstx_mac_test_ctl2 | 00000000 | 0x818105fc: | |
| 3F_hsstx_mac_test_ctl1 | 000000c6 | | |

HSS RX registers

=====

| | | | |
|---------------------------------------|----------|-------------|--|
| 0x81810700: 00_hssrx_cfg_mode_PHY | 00009e78 | 0x81810704: | |
| 01_hssrx_test_ctl | 00000000 | | |
| 0x81810708: 02_hssrx_phs_rot_ctl | 0000cb80 | 0x8181070c: | |
| 03_hssrx_phs_rot_ofs_ctl | 00004610 | | |
| 0x81810710: 04_hssrx_phs_rot_posn1 | 00001110 | 0x81810714: | |
| 05_hssrx_phs_rot_posn2 | 0000003d | | |
| 0x81810718: 06_hssrx_phs_rot_sta_ofs1 | 00000000 | 0x8181071c: | |
| 07_hssrx_phs_rot_sta_ofs2 | 0000001f | | |

| | | |
|--|----------------|-------------|
| 0x81810720: 08_hssrx_dfe_ctl_PHY | 00002002 | 0x81810724: |
| 09_hssrx_dfe_smpl_snap1 | 00000000 | |
| 0x81810728: 0A_hssrx_dfe_smpl_snap2 | 00008000 | 0x8181072c: |
| 0B_hssrx_vga_ctl1 | 000041fc | |
| 0x81810730: 0C_hssrx_vga_ctl2 | 00007aa0 | 0x81810734: |
| 0D_hssrx_vga_ctl3 | 000009e4 | |
| 0x81810738: 0E_hssrx_pwr_mgmt_ctl | 0000001f | 0x8181073c: |
| 0F_hssrx_iqamp_ctl1 | 0000001a | |
| 0x81810740: 10_hssrx_iqamp_ctl2 | 00000008 | 0x81810744: |
| 11_hssrx_dacap_dacan_sel | 00000003 | |
| 0x81810748: 12_hssrx_dacap_dacan | 0000ffff | 0x8181074c: |
| 13_hssrx_daca_min | 00000000 | |
| 0x81810750: 14_hssrx_adac_ctl | 00000000 | 0x81810754: |
| 15_hssrx_ac_cp_ctl | 000031c3 | |
| 0x81810758: 16_hssrx_ac_cp_val | 00000051 | 0x8181075c: |
| 17_hssrx_dfe_h1h2h3_lcl_off_ch | 00000014 | |
| 0x81810760: 18_hssrx_dfe_h1h2h3_lcl_off_val | 00000000 | 0x81810764: |
| 19_hssrx_peaked_intg | 000000ff | |
| 0x81810768: 1A_hssrx_cdr_analog_sw | 0000ce00 | 0x8181076c: |
| 1B_hssrx_peaking_amp_init_c_PHY | 00000000 | |
| 0x81810770: 1C_hssrx_dac_dpc | 00000040 | 0x81810774: |
| 1D_hssrx_ddc | 00000000 | |
| 0x81810778: 1E_hssrx_int_stat_PHY | 00000c0f | 0x8181077c: |
| 1F_hssrx_dfe_func_ctl1_PHY | 0000ffff | |
| 0x81810780: 20_hssrx_dfe_func_ctl2_INV | 00007ebf | 0x81810784: |
| 21_hssrx_ofs_ch_dcc_qcc_idx | 00002000 | |
| 0x81810788: 22_hssrx_dfe_ofs_val | 00007b7b | 0x8181078c: |
| 23_hssrx_h_coeff_bist | 0000040e | |
| 0x81810790: 24_hssrx_ac_cap_bist | 000000aa | 0x81810794: |
| 25_hssrx_max_gain_path_idx_res | 00007800 | |
| 0x81810798: 26_hssrx_loff_ctl | 00000040 | 0x8181079c: |
| 27_hssrx_sigdet_ctl | 00004280 | |
| 0x818107a0: 28_hssrx_ana_ctl_sw | 00000000 | 0x818107a4: |
| 29_hssrx_intg_dac_ofs | 0000dee0 | |
| 0x818107a8: 2A_hssrx_eye_ctl | 00000000 | 0x818107ac: |
| 2B_hssrx_eye_met | 00000004 | |
| 0x818107b0: 2C_hssrx_eye_met_err_cnt | 00000000 | 0x818107b4: |
| 2D_hssrx_eye_met_pdf_eyec | 00000000 | |
| 0x818107b8: 2E_hssrx_eye_met_pat_len | 0000007f | 0x818107bc: |
| 2F_hssrx_dfe_func_ctl3 | 0000dfff | |
| 0x818107c0: 30_hssrx_dfe_tap_ctl_idx_ptr | 00000008 | 0x818107c4: |
| 31_hssrx_dfe_tap | 00003030 | |
| 0x818107c8: 32_hssrx_lte_ctl_TUNE | 00001601 | 0x818107e4: |
| 39_hssrx_int_stat2 | 0000c1ff | |
| 0x818107e8: 3A_hssrx_ac_cpl_cur_src_adj | 00000042 | 0x818107ec: |
| 3B_hssrx_dcd_ctl | 00007c51 | |
| 0x818107f0: 3C_hssrx_dcc_ctl | 00000d41 | 0x818107f4: |
| 3D_hssrx_qcc_ctl | 00006941 | |
| 0x818107f8: 3E_hssrx_mac_test_ctl2 | 00000000 | 0x818107fc: |
| 3F_hssrx_mac_test_ctl1 | 00000000 | |
| 0x81810748: 12_hssrx_dacap_dacan[02] | 00ff ffff | |
| 0x81810760: 18_hssrx_dfe_h1h2h3_lcl_off_va[00] | 0000 0000 0000 | |
| 0000 0000 0000 0000 0000 | | |
| 0x81810760: 18_hssrx_dfe_h1h2h3_lcl_off_va[08] | 0000 0000 0000 | |

```

0000 0000 0000 0000 0000
0x81810760: 18_hssrx_dfe_h1h2h3_lcl_off_va[16]      0000 0000 0000
0000 0000
0x81810788: 22_hssrx_dfe_ofs_val[00][00]              7b7b 0000 057f
7f00 0909 7f7f
0x81810788: 22_hssrx_dfe_ofs_val[03][00]              0403 7f00 7e01
007f 050b 7f7f
0x81810788: 22_hssrx_dfe_ofs_val[06][00]              037f 0000 077b
7f00 7f7d 7f00
0x81810788: 22_hssrx_dfe_ofs_val[09][00]              7b79 0000 087d
7f00 067f 7f00
0x81810788: 22_hssrx_dfe_ofs_val[12][00]             0b79 7f00 7d09
007f 7e7d 0000
0x81810788: 22_hssrx_dfe_ofs_val[15][00]             7e7f 0000 067b
7f00 0301 7f00
0x81810788: 22_hssrx_dfe_ofs_val[18][00]             7d7f 0000 017b
0000 007d 0000
0x81810788: 22_hssrx_dfe_ofs_val[21][00]             007d 0000 007d
0000 007d 0000
0x81810788: 22_hssrx_dfe_ofs_val[24][00]             0706 0000 047f
0000 7c7c 0000
0x81810794: 25_hssrx_max_gain_path_idx_res[00]       0060 0853 110c
1894 20c0 28a0 308b 3800
0x81810794: 25_hssrx_max_gain_path_idx_res[08]       4090 4875 5070
5801 6040 6800 70ff 7800
0x818107c4: 31_hssrx_dfe_tap[00]                          fffe 8181 0000
0000 0030 0030 3030 3030
0x818107c4: 31_hssrx_dfe_tap[08]                          3030 3030 3030
0000
0x818107e8: 3A_hssrx_ac_cpl_cur_src_adj[00]              0042 0042 0042
0042
0x818107ec: 3B_hssrx_dcd_ctl[00]                          7c51 5c00 7c00
5c00 7c00
0x818107f0: 3C_hssrx_dcc_ctl[00]                          0d41 0d44 0d81
0d85
0x818107f4: 3D_hssrx_qcc_ctl[00]                          698b 6941

```

xfipcs, fec, aec, & aet registers

=====

```

0x81c98400: xfipcs_reg [00] 00002040 00000080 00000000
00000000 00000001 00000008 00000000 00000000
0x81c98420: xfipcs_reg [08] 00008401 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c98440: xfipcs_reg [16] 00000000 00000000 00000000
00000000 00000040 00000000 00000000 00000000
0x81c98460: xfipcs_reg [24] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c98480: xfipcs_reg [32] 00000004 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c98620: fec_32g_128g_reg [08] 00000000 00008003 00000000
00000000 00000000 00000000 00000000
0x81c98648: fec_32g_128g_reg [18] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c98a00: aec_reg [00] 00000000 00000000 00000000

```

```

00000000 00000040 00000000 00000000 00002490
0x81c98c00: aet_reg [00] 000000b0 00007000 000008c4
00000000 00000000

```

bbc registers

=====

```

0x81c99800: bbc_trc 0 0 0 0 0 0 0
0
0x81c99840: bbc_trc 0 0 0 0 0 0 0
0
0x81c99880: bbc_trc 0 0 0 0 0 0 0
0
0x81c998c0: bbc_trc 0 0 0 0 0 0 0
0
0x81c99900: bbc_trc 0 0 0 0 0 0 0
0
0x81c99804: bbc_mbc 0 0 0 0 0 0 0
0
0x81c99844: bbc_mbc 0 0 0 0 0 0 0
0
0x81c99884: bbc_mbc 0 0 0 0 0 0 0
0
0x81c998c4: bbc_mbc 0 0 0 0 0 0 0
0
0x81c99904: bbc_mbc 0 0 0 0 0 0 0
0
0x81c99a00: bbc_rcc 0 0 0 0 0 0 0
0
0x81c99a20: bbc_rcc 0 0 0 0 0 0 0
0
0x81c99a40: bbc_rcc 0 0 0 0 0 0 0
0
0x81c99a60: bbc_rcc 0 0 0 0 0 0 0
0
0x81c99a80: bbc_rcc 0 0 0 0 0 0 0
0
0x81c99c00: bbc_rqc 0 0 0 0 0 0 0
0
0x81c99c20: bbc_rqc 0 0 0 0 0 0 0
0
0x81c99c40: bbc_rqc 0 0 0 0 0 0 0
0
0x81c99c60: bbc_rqc 0 0 0 0 0 0 0
0
0x81c99c80: bbc_rqc 0 0 0 0 0 0 0
0
0x81c99d00: bbc_fbpc 00000000 0x81c99d04: bbc_csc
00000000
0x81c99d08: bbc_rcc_inc 00000000 0x81c99d0c:
bbc_rqc_inc 00000000
0x81c99d10: bbc_fbpc_inc 00000000 0x81c99d14:
bbc_tmc_inc 00000000
0x81c99d18: bbc_threshold 00080100 0x81c99d1c:
bbc_counter_clr 00000000

```

| | | |
|-------------------------------------|----------|----------------------|
| 0x81c99d20: bbc_debug_en | 00000000 | 0x81c99d24: bbc_ctrl |
| 00200120 | | |
| 0x81c99d28: bbc_rqc_rcc_thresh | 00000055 | 0x81c99d34: |
| bbc_bb_sc_n | 00000000 | |
| 0x81c99d38: bbc_crd_reco_debug | 00000000 | 0x81c99d3c: |
| bbc_crd_reco_debug_data | 00000000 | |
| 0x81c99d40: bbc_multi_frm_loss_cnt | 00000000 | 0x81c99d44: |
| bbc_multi_rdy_loss_cnt | 00000000 | |
| 0x81c99d48: bbc_1frm_loss_recov_cnt | 00000000 | 0x81c99d4c: |
| bbc_1rdy_loss_recov_cnt | 00000000 | |
| 0x81c99d58: bbc_int_status | 00000000 | 0x81c99d5c: |
| bbc_int_set | 00000000 | |
| 0x81c99d60: bbc_int_first | 00000000 | 0x81c99d64: |
| bbc_frm_rdy_rx_err_addr | 00000000 | |
| 0x81c99d68: bbc_frm_rdy_tx_err_addr | 00000000 | 0x81c99d6c: |
| bbc_trc_mbc_err_addr | 00000000 | |
| 0x81c99d70: bbc_frm_rdy_rx_dbl_ecc | 00000000 | 0x81c99d74: |
| bbc_frm_rdy_tx_dbl_ecc | 00000000 | |
| 0x81c99d78: bbc_trc_mbc_dbl_ecc | 00000000 | |
| 0x81c99d7c: bbc_fsm_status | 00001011 | 0x81c99d80: |
| bbc_force_err | 00000000 | |
| 0x81c99d84: bbc_crdt_avail0 | 00000000 | 0x81c99d88: |
| bbc_crdt_avail1 | 00000000 | |
| 0x81c99d8c: bbc_scratch | 00000000 | |

FPS registers

=====

| | | |
|--------------------------------|----------|-------------|
| 0x81c98004: fps_er_enc_in | 00000000 | 0x81c98008: |
| fps_er_crc | 00000000 | |
| 0x81c9800c: fps_er_trunc | 00000000 | 0x81c98010: |
| fps_er_toolong | 00000000 | |
| 0x81c98014: fps_er_bad_eof | 00000000 | 0x81c98018: |
| fps_er_enc_out | 00000000 | |
| 0x81c9801c: fps_er_bad_os | 00000000 | 0x81c98020: |
| fps_er_flush | 00000000 | |
| 0x81c98024: fps_er_ifg | 00000000 | 0x81c98038: |
| fps_er_crc_good_eof | 00000000 | |
| 0x81c9803c: fps_inv_arb | 00000000 | 0x81c98040: |
| fps_slow_sts_status | 00000000 | |
| 0x81c98044: fps_tx_frm_cnt | 00000000 | 0x81c98048: |
| fps_rx_frm_cnt | 00000000 | |
| 0x81c98050: fps_tx_word_cnt_hi | 00000000 | 0x81c9804c: |
| fps_tx_word_cnt_lo | 00000000 | |
| 0x81c98058: fps_rx_word_cnt_hi | 00000000 | 0x81c98054: |
| fps_rx_word_cnt_lo | 00000000 | |

BAL registers

=====

| | | |
|---------------------------------|----------|-------------|
| 0x81c9f000: bal_desired_buf | 00000000 | 0x81c9f004: |
| bal_alloc_buf | 00000000 | |
| 0x81c9f008: bal_busy_buf | 00000000 | 0x81c9f00c: |
| bal_usable_buf | 00000000 | |
| 0x81c9f010: bal_max_bor_buf | 00000000 | |
| 0x81c9f014: bal_busy_buf_thresh | 00000002 | |

TXQ registers

=====

| | | | |
|-------------|-------------------------|----------|-------------------|
| 0x81c9b004: | txq_phys_port_ctl | 00430000 | |
| 0x81c9b050: | txq_link_skew | 00000000 | |
| 0x81c9b068: | txq_cr_lk_dttm_intr_sts | [00] | 00000000 00000000 |
| 0x81c9b070: | txq_cr_lk_dttm_intr_en | [00] | 00000000 00000000 |
| 0x81c9b024: | txq_disc_frm_trap_cnt | 00000014 | |

FDS registers

=====

| | | | |
|-------------|--------------------------|----------|-------------|
| 0x81c9c000: | fds_rxf_ctl | 00000002 | 0x81c9c004: |
| | fds_rxf_wait_thresh | 00000909 | |
| 0x81c9c018: | fds_rxf_first_error | 00000000 | 0x81c9c01c: |
| | fds_rxf_first_error_info | 00000000 | |
| 0x81c9c020: | fds_rxf_inout_pkt_cnt | 00000000 | |
| 0x81c9c008: | fds_rxf_err_int_status | 00000000 | 0x81c9c024: |
| | fds_rxf_fifo_status | 00888888 | |
| 0x81c9d000: | fds_txf_ctl | 0000003a | 0x81c9d004: |
| | fds_txf_wait_ifg_thresh | 00a00106 | |
| 0x81c9d008: | fds_txf_err_int_status | 00000000 | 0x81c9d024: |
| | fds_txf_fifo_status | 00088888 | |
| 0x81c9d02c: | fds_txf_bbc_scs | 00000000 | |

Logical TXQ registers

=====

| | | | |
|-------------|------------------------|----------|----------------------------|
| 0x81c9b000: | txq_log_port_ctl | 00000002 | 0x81c9b008: |
| | txq_port_status | 00000000 | |
| 0x81c9b00c: | txq_todo_flags | [00] | 00000000 00000000 |
| 0x81c9b014: | txq_spd_match_desc | [00] | 00000000 00000000 00000000 |
| | | | 00000000 |
| 0x81c9b024: | txq_spd_match_desc | [04] | 00000014 |
| 0x81c9b028: | txq_vc_weight | [00] | 01010101 01010101 01010101 |
| | | | 01010101 |
| 0x81c9b038: | txq_vc_weight | [04] | 01010101 01010101 01010101 |
| | | | 01010101 |
| 0x81c9b048: | txq_vc_weight | [08] | 01010101 00010101 |
| 0x81c9b054: | txq_cong_dttm_ctrl | 00000106 | |
| 0x81c9b058: | txq_cong_dttm_intr_sts | [00] | 00000000 00000000 |
| 0x81c9b060: | txq_cong_dttm_intr_en | [00] | 00000000 00000000 |
| 0x81c9b078: | txq_bw_limit_en_reg | [00] | 00000000 00000000 |
| 0x81c9b080: | txq_bw_gua_en_reg | [00] | 00000000 00000000 |
| 0x81c9b088: | txq_vc_group | [00] | 03030300 03030303 03030303 |
| | | | 03030303 |
| 0x81c9b098: | txq_vc_group | [04] | 03030303 03030303 03030303 |
| | | | 03030303 |
| 0x81c9b0a8: | txq_vc_group | [08] | 03030303 03030303 00000000 |
| | | | 00000000 |
| 0x81c9b0b0: | txq_bw_thresh_group | [00] | 00000000 00000000 00000000 |
| | | | 00000000 |
| 0x81c9b0c0: | txq_bw_thresh_group | [04] | 00000000 00000000 00000000 |
| | | | 00000000 |
| 0x81c9b0d0: | txq_bw_thresh_group | [08] | 00000000 00000000 00000000 |
| | | | 00000000 |

| | | | | |
|---------------------------------|------|----------|----------|----------|
| 0x81c9b0e0: txq_bw_thresh_group | [12] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c9b0f0: txq_bw_thresh_group | [16] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c9b100: txq_bw_thresh_group | [20] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c9b110: txq_bw_thresh_group | [24] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c9b120: txq_bw_thresh_group | [28] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c9b130: txq_bw_thresh_group | [32] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c9b140: txq_bw_thresh_group | [36] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |

txq Congestion detection Statistics RAM

=====

| | | |
|--------------------|----------|--------------------|
| 0x81090be0: vc[0] | 00000000 | 0x81090be4: vc[1] |
| 00000000 | | |
| 0x81090be8: vc[2] | 00000000 | 0x81090bec: vc[3] |
| 00000000 | | |
| 0x81090bf0: vc[4] | 00000000 | 0x81090bf4: vc[5] |
| 00000000 | | |
| 0x81090bf8: vc[6] | 00000000 | 0x81090bfc: vc[7] |
| 00000000 | | |
| 0x81090c00: vc[8] | 00000000 | 0x81090c04: vc[9] |
| 00000000 | | |
| 0x81090c08: vc[10] | 00000000 | 0x81090c0c: vc[11] |
| 00000000 | | |
| 0x81090c10: vc[12] | 00000000 | 0x81090c14: vc[13] |
| 00000000 | | |
| 0x81090c18: vc[14] | 00000000 | 0x81090c1c: vc[15] |
| 00000000 | | |
| 0x81090c20: vc[16] | 00000000 | 0x81090c24: vc[17] |
| 00000000 | | |
| 0x81090c28: vc[18] | 00000000 | 0x81090c2c: vc[19] |
| 00000000 | | |
| 0x81090c30: vc[20] | 00000000 | 0x81090c34: vc[21] |
| 00000000 | | |
| 0x81090c38: vc[22] | 00000000 | 0x81090c3c: vc[23] |
| 00000000 | | |
| 0x81090c40: vc[24] | 00000000 | 0x81090c44: vc[25] |
| 00000000 | | |
| 0x81090c48: vc[26] | 00000000 | 0x81090c4c: vc[27] |
| 00000000 | | |
| 0x81090c50: vc[28] | 00000000 | 0x81090c54: vc[29] |
| 00000000 | | |
| 0x81090c58: vc[30] | 00000000 | 0x81090c5c: vc[31] |
| 00000000 | | |
| 0x81090c60: vc[32] | 00000000 | 0x81090c64: vc[33] |
| 00000000 | | |
| 0x81090c68: vc[34] | 00000000 | 0x81090c6c: vc[35] |
| 00000000 | | |
| 0x81090c70: vc[36] | 00000000 | 0x81090c74: vc[37] |

00000000
0x81090c78: vc[38] 00000000 0x81090c7c: vc[39]
00000000

Logical STS registers

=====
0x81584ec4: sts_ftb_type1_miss 00000000
0x81584ec8: sts_ftb_type2_miss 00000000
0x81584ecc: sts_ftb_type6_miss 00000000
0x81584ed0: sts_hard_zoning_miss 00000000
0x81584ed4: sts_lun_zoning_miss 00000000
0x81584edc: sts_unroutable 00000000
0x81581ef4: sts_rte_cl2 00000000 0x81581ef8:
sts_rte_cl3 00000000 0x81581efc: sts_rte_link_ctl
00000000 0x81584ee8: sts_tx_timeout 00000000

Logical STS filter registers

=====
0x81584e40: stsflt_trig [00] 00000000 00000000 00000000
00000000
0x81584e50: stsflt_trig [04] 00000000 00000000 00000000
00000000
0x81584e60: stsflt_trig [08] 00000000 00000000 00000000
00000000
0x81584e70: stsflt_trig [12] 00000000 00000000 00000000
00000000
0x81584e80: stsflt_trig [16] 00000000 00000000 00000000
00000000
0x81584e90: stsflt_trig [20] 00000000 00000000 00000000
00000000
0x81584ea0: stsflt_trig [24] 00000000 00000000 00000000
00000000
0x81584eb0: stsflt_trig [28] 00000000 00000000 00000000
00000000
0x81584ec0: stsflt_trig [32]

Logical STS discard registers

=====
0x81582b9c: disc_mcast_wka 00000000 0x81582ba0:
disc_inv_did 00000000
0x81582ba4: disc_cl1_cl4 00000000 0x81582ba8:
disc_sid_chk_fail 00000000
0x81582bac: disc_inv_dom_egid_txpt 00000000 0x81582bb0:
disc_vft_hop_cnt_1 00000000
0x81582bb4: disc_classf 00000000 0x81582bb8:
disc_fcp_cdb_inv 00000000
0x81582bbc: disc_vfid_trap_enabled 00000000 0x81582bc0:
disc_vfid_hdr_chk_fail 00000000
0x81582bc4: disc_shim_cksum_fail 00000000 0x81582bc8:
disc_fed_edit_cmd_err 00000000
0x81582bcc: disc_ftb_vm_mode 00000000 0x81582bd0:
disc_ftb_agnt2_miss 00000000
0x81582bd4: disc_ecb_reserved 00000000 0x81582bd8:

```

disc_ecb_de_pad_err      00000000
0x81582bdc: disc_ecb_de_tag_err      00000000      0x81582be0:
disc_ecb_de_seq_err      00000000
0x81582be4: disc_ecb_err      00000000      0x81582be8:
disc_ftb_type4_match      00000000
0x81582bec: disc_fcp_rsp_ftb_type4      00000000      0x81582bf0:
disc_ftb_type5_match      00000000
0x81582bf4: disc_ftb_type3_match      00000000      0x81582bf8:
disc_els_ftb_type3      00000000
0x81582bfc: disc_ftb_type1_match      00000000      0x81582c00:
disc_els_rsp_ex_port      00000000
0x81582c04: disc_inv_drp_dps      00000000      0x81582c08:
disc_did_lookup_miss      00000000
0x81582c0c: disc_ftb_type2_match      00000000      0x81582c10:
disc_trpd_plogi_pdisc      00000000
0x81582c14: disc_type2_lookup_miss      00000000      0x81582c18:
disc_ftb_type6_match      00000000
0x81582c1c: disc_els_rep_ex_port      00000000      0x81582c20:
disc_els_sid_lkup_bit1      00000000
0x81582c24: disc_els_sid_lkup_bit0      00000000      0x81582c28:
disc_bls_frm_trap_bit1      00000000
0x81582c2c: disc_ftb_token_err      00000000      0x81582c30:
disc_asic_internal_err      00000000
0x81582c34: disc_hard_zone_miss      00000000      0x81582c38:
disc_lun_zone_miss      00000000
0x81582c3c: discflt_frame_disc      00000000      0x81582c40:
discflt_parity_err      00000000
0x81582c44: disc_frame_marked_du      00000000      0x81582c48:
disc_frame_marked_to      00000000
0x81582c4c: disc_lkup_rte_prty_err      00000000

```

portstatsshow 46

```

stat_wtx      0      4-byte words transmitted
stat_wrx      0      4-byte words received
stat_ftx      0      Frames transmitted
stat_frx      0      Frames received
stat_c2_frx      0      Class 2 frames received
stat_c3_frx      0      Class 3 frames received
stat_lc_rx      0      Link control frames
received
stat_mc_rx      0      Multicast frames
received
stat_mc_to      0      Multicast timeouts
stat_mc_tx      0      Multicast frames
transmitted
tim_txcrd_z      0      Time TX Credit Zero
(2.5Us ticks)
tim_txcrd_z_vc 0- 3: 0      0      0      0
tim_txcrd_z_vc 4- 7: 0      0      0      0
tim_txcrd_z_vc 8-11: 0      0      0      0
tim_txcrd_z_vc 12-15: 0      0      0      0
lat_tot_pkt_vc 0- 3: 1      1      1      1
lat_tot_pkt_vc 4- 7: 1      1      1      1

```


| | | | | | |
|------------------------------|-----------------------------|-------------------------|---|---|-----|
| lat_tot_pkt_vc | 8-11: | 1 | 1 | 1 | 1 |
| lat_tot_pkt_vc | 12-15: | 1 | 1 | 1 | 1 |
| lat_hi_time_vc | 0- 3: | 0 | 0 | 0 | 0 |
| lat_hi_time_vc | 4- 7: | 0 | 0 | 0 | 0 |
| lat_hi_time_vc | 8-11: | 0 | 0 | 0 | 0 |
| lat_hi_time_vc | 12-15: | 0 | 0 | 0 | 0 |
| lat_lo_time_vc | 0- 3: | 1 | 1 | 1 | 1 |
| lat_lo_time_vc | 4- 7: | 1 | 1 | 1 | 1 |
| lat_lo_time_vc | 8-11: | 1 | 1 | 1 | 1 |
| lat_lo_time_vc | 12-15: | 1 | 1 | 1 | 1 |
| max_latency_vc | 0- 3: | 1 | 1 | 1 | 1 |
| max_latency_vc | 4- 7: | 1 | 1 | 1 | 1 |
| max_latency_vc | 8-11: | 1 | 1 | 1 | 1 |
| max_latency_vc | 12-15: | 1 | 1 | 1 | 1 |
| latency_dma_ts | 09-09-2024 UTC Mon 08:47:25 | | | | TXQ |
| Latency DMA TimeStamp | | | | | |
| fec_cor_detected | 0 | Count of blocks that | | | |
| were corrected by FEC | | | | | |
| fec_uncor_detected | 0 | Count of blocks that | | | |
| were left uncorrected by FEC | | | | | |
| er_enc_in | 0 | Encoding errors inside | | | |
| of frames | | | | | |
| er_crc | 0 | Frames with CRC errors | | | |
| er_trunc | 0 | Frames shorter than | | | |
| minimum | | | | | |
| er_toolong | 0 | Frames longer than | | | |
| maximum | | | | | |
| er_bad_eof | 0 | Frames with bad end-of- | | | |
| frame | | | | | |
| er_enc_out | 0 | Encoding error outside | | | |
| of frames | | | | | |
| er_bad_os | 0 | Invalid ordered set | | | |
| er_pcs_blk | 0 | PCS block errors | | | |
| er_rx_c3_timeout | 0 | Class 3 receive frames | | | |
| discarded due to timeout | | | | | |
| er_tx_c3_timeout | 0 | Class 3 transmit frames | | | |
| discarded due to timeout | | | | | |
| er_unroutable | 0 | Frames that are | | | |
| unroutable | | | | | |
| er_unreachable | 0 | Frame with unreachable | | | |
| destination | | | | | |
| er_other_discard | 0 | Other discards | | | |
| er_type1_miss | 0 | frames with FTB type 1 | | | |
| miss | | | | | |
| er_type2_miss | 0 | frames with FTB type 2 | | | |
| miss | | | | | |
| er_type6_miss | 0 | frames with FTB type 6 | | | |
| miss | | | | | |
| er_zone_miss | 0 | frames with hard zoning | | | |
| miss | | | | | |
| er_lun_zone_miss | 0 | frames with LUN zoning | | | |
| miss | | | | | |
| er_crc_good_eof | 0 | Crc error with good eof | | | |
| er_inv_arb | 0 | Invalid ARB | | | |

| | | |
|-----------------------|-----------------------------|--------------------------|
| er_single_credit_loss | 0 | Single vcrdy/frame loss |
| on link | | |
| er_multi_credit_loss | 0 | Multiple vcrdy/frame |
| loss on link | | |
| other_credit_loss | 0 | Link timeout/complete |
| credit loss | | |
| phy_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | Timestamp of |
| phy_port stats clear | | |
| lgc_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | Timestamp of |
| lgc_port stats clear | | |
| fec_corrected_rate | 0 | FEC Corrected blocks per |
| second | | |

portstats64show 46

| | | |
|---------------|---|--|
| stat64_wtx | 0 | top_int : 4-byte words transmitted |
| | 0 | bottom_int : 4-byte words transmitted |
| stat64_wrx | 0 | top_int : 4-byte words received |
| | 0 | bottom_int : 4-byte words received |
| stat64_ftx | 0 | top_int : Frames transmitted |
| | 0 | bottom_int : Frames transmitted |
| stat64_frx | 0 | top_int : Frames received |
| | 0 | bottom_int : Frames received |
| stat64_c2_frx | 0 | top_int : Class 2 frames received |
| | 0 | bottom_int : Class 2 frames received |
| stat64_c3_frx | 0 | top_int : Class 3 frames received |
| | 0 | bottom_int : Class 3 frames received |
| stat64_lc_rx | 0 | top_int : Link control frames received |
| | 0 | bottom_int : Link control frames |
| received | | |
| stat64_mc_rx | 0 | top_int : Multicast frames received |
| | 0 | bottom_int : Multicast frames received |
| stat64_mc_to | 0 | top_int : Multicast timeouts |
| | 0 | bottom_int : Multicast timeouts |
| stat64_mc_tx | 0 | top_int : Multicast frames transmitted |
| | 0 | bottom_int : Multicast frames |
| transmitted | | |
| tim64_rdy_pri | 0 | top_int : Time R_RDY high priority |
| | 0 | bottom_int : Time R_RDY high priority |
| tim64_txcrd_z | 0 | top_int : Time BB_credit zero |
| | 0 | bottom_int : Time BB_credit zero |
| er64_enc_in | 0 | top_int : Encoding errors inside of |
| frames | | |
| | 0 | bottom_int : Encoding errors inside of |
| frames | | |
| er64_crc | 0 | top_int : Frames with CRC errors |
| | 0 | bottom_int : Frames with CRC errors |
| er64_trunc | 0 | top_int : Frames shorter than minimum |
| | 0 | bottom_int : Frames shorter than minimum |
| er64_toolong | 0 | top_int : Frames longer than maximum |
| | 0 | bottom_int : Frames longer than maximum |
| er64_bad_eof | 0 | top_int : Frames with bad end-of-frame |
| | 0 | bottom_int : Frames with bad end-of- |
| frame | | |
| er64_enc_out | 0 | top_int : Encoding error outside of |

| | | |
|---|---|--|
| frames | 0 | bottom_int : Encoding error outside of |
| frames | | |
| er64_disc_c3 | 0 | top_int : Class 3 frames discarded |
| | 0 | bottom_int : Class 3 frames discarded |
| er64_pcs_blk | 0 | top_int : PCS block errors |
| | 0 | bottom_int : PCS block errors |
| stat64_rateTxFrame | 0 | Tx frame rate (fr/sec) |
| stat64_rateRxFrame | 0 | Rx frame rate (fr/sec) |
| stat64_rateTxPeakFrame | 0 | Tx peak frame rate (fr/sec) |
| stat64_rateRxPeakFrame | 0 | Rx peak frame rate (fr/sec) |
| stat64_rateTxWord | 0 | Tx Word rate (words/sec) |
| stat64_rateRxWord | 0 | Rx Word rate (words/sec) |
| stat64_rateTxPeakWord | 0 | Tx peak Word rate (words/sec) |
| stat64_rateRxPeakWord | 0 | Rx peak Word rate (words/sec) |
| stat64_PRJTFrames | 0 | top_int : Number of PRJT frames |
| returned to this port | | |
| | 0 | bottom_int : Number of PRJT |
| frames returned to this port | | |
| stat64_PBSYFrames | 0 | top_int : Number of PBSY frames |
| returned to this port | | |
| | 0 | bottom_int : Number of PBSY |
| frames returned to this port | | |
| stat64_inputBuffersFull | 0 | top_int : Number of occurrences |
| when all input buffers full | | |
| | 0 | bottom_int : Number of |
| occurrences when all input buffers full | | |
| stat64_rxClass1Frames | 0 | top_int : Number of class 1 |
| frames received | | |
| | 0 | bottom_int : Number of class 1 |
| frames received | | |
| stat64_aveTxFrameSize | 0 | Average Tx Frame size |
| stat64_aveRxFrameSize | 0 | Average Rx Frame size |
| Lr_in | 0 | top_int |
| | 0 | bottom_int |
| Ols_in | 0 | top_int |
| | 0 | bottom_int |
| Lr_out | 0 | top_int |
| | 0 | bottom_int |
| Ols_out | 0 | top_int |
| | 0 | bottom_int |
| Link_failure | 0 | top_int |
| | 0 | bottom_int |
| Invalid_CRC | 0 | top_int |
| | 0 | bottom_int |
| Invalid_word | 0 | top_int |
| | 0 | bottom_int |
| Protocol_err | 0 | top_int |
| | 0 | bottom_int |
| Loss_of_sig | 0 | top_int |
| | 0 | bottom_int |
| Loss_of_sync | 0 | top_int |
| | 0 | bottom_int |
| er_bad_os | 0 | top_int : Invalid ordered set |

0 bottom_int: Invalid ordered set

portrouteshow 46
port address ID: 0x012e00
external unicast routing table:
0: Embedded
255: Embedded
internal unicast routing table:
0: Embedded

portcamshow 46

```
-----  
Port  SID used  DID used  SID entries  DID entries  
46    0         0        000000      000000  
-----
```

ptbufshow, ptcridtshow, ptdatashow, ptstatsshow 46

```
S:  
S:VF Enable:          1  
S:  
S:C4 Global Variable:  
S:-----  
-----  
S:trace_stop:        0  
S:  
S:C4 Phy Data Pointers: c4_phyp = 0xb6adb0c0  
S:-----  
-----  
S:tnodep              0xbb841000      pt  
      0x43028013  
S:proto_phyp          0xb8809a20      phy_cfg  
0xb6adc100  
S:c4_chp              0x97e28000      c4_lgcp  
0x97f94000  
S:c4_phy_regp         0x81c98000      proc_dir  
0xb851a320  
S:-----  
-----  
S:magic_id            0xc4345678      num_port_timer    12  
S:prev_if_id          0x43020013      S:ftx              0  
      tov          0  
S:initialized         1                port_idx           19  
S:ui_idx              46                slot_no  
      0  
S:blade_idx           19                sw_usr_ports       400  
S:unused              0                intr_debounced  
      0  
S:aec_status          0x0              reason_code  
      0  
S:debug               0x00000004      debug_trc_line     0  
S:rxbuf_list_head     0xffffffff      rxbuf_list_tail  
0xffffffff  
S:isAePort            0                port_misc_data
```

| | | | |
|------------------------------|------------|-----------------------|-----|
| | 0 | | |
| S:num_fault1_rx_disc | 0 | num_fault2_rx_disc | 0 |
| S:p_lli_cause0 | 0 | p_sig_regained | 0 |
| S:p_sync_regained | 0 | enc_out | |
| | 0x0 | | |
| S:cached_fps_status | 0 | cached_sts_status | 0 |
| S:cached_er_crc_good_eof | 0 | cached_er_too_long | 0 |
| S:cached_er_bad_os | 0 | | |
| S:cached_er_trunc | 0 | | |
| cached_tot_er_crc_good_eof | 0 | | |
| S:num_pt_excess_intr | 0 | num_no_fid | 0 |
| S:num_fault1_cnt | 0 | num_fault2_cnt | |
| | 0 | | |
| S:num_fault_lip | 0 | num_fault_lli | 0 |
| S:num_fault_rx_fifo | 0 | num_fault_hss | 0 |
| S:num_fault_bwait | 0 | lli_intr_prim | |
| | 0 | | |
| S:num_sw_link_to | 0 | | |
| be_link_err_mon_count | 0 | | |
| S:ecb_enc_enabled | 0 | ecb_comp_enabled | |
| | 0 | | |
| S:ecb_rsv_enc | 0 | ecb_rsv_comp | 0 |
| S:ecb_enc_bm | 0x0 | ecb_key_index | |
| 0xffffffff | | | |
| S:fab_idx | 0 | | |
| S:num_be_lto | 0 | lto_count_reset_intvl | |
| | 0 | | |
| S:lr_count_reset_intvl | 0 | num_be_lr | |
| | 0 | | |
| S:num_fault_qsf | 0 | check_lto | |
| | 0 | | |
| S:credit_loaded | 0 | num_credit_overrun | |
| | 0 | | |
| S:fec_enabled | 0x0 | fec_los_to_flag | 0x0 |
| S:phy_stats_clear_ts | 1725611419 | pcs_err_online | |
| | 0 | | |
| S:pcs_err_light_det | 0 | pcs_err_ignore | |
| | 0 | | |
| S:pcs_blk_err | 0 | pcs_hiber | 0 |
| S:phy_port_status | 0 | ecb_enc_lr_count | |
| | 0 | | |
| S:dport_mode | 0 | avoid_lto_det | 0 |
| S:sn_debounced | 0x0 | sn_started_kr_reqd | 0 |
| S:major_timer_started | 0x0 | ready_bm | 0x0 |
| S:parln_1_bm | 0x0 | parln_0_bm | 0x0 |
| S:be_los_of_sync_event_intvl | | 0 | |
| be_los_of_sync_event | 0 | | |
| S:errataPtenable_cntr | 0 | errataPoll_cntr | |
| | 0 | | |
| S:jda_rx_sig_loss_det | 0 | jda_rx_sig_loss_cnt | |
| | 0 | | |
| S:encrypt_blk_error | 0 | | |
| S: | | | |
| S: c4_trunk | | | |

```

S:=====
S:mark_ts          0x0          deskew          0x0
S:master_phyp     0x0
S:
S:adelay[00]: 0x00000000 0x00000000 0x00000000 0x00000000
S:adelay[04]: 0x00000000 0x00000000 0x00000000 0x00000000
S:
S:      c4_buf
S:=====
S:tx_csc          0          rx_csc
      0
S:ld_vc_credits  0          tx_flag          0x0
S:alloc_buffers  0          req_buffers          0
S:est_buffers    20          ld_use_est          0
S:bb_sc_n        0          rx_bb_sc_n
      0
S:data_cr        5          nondata_cr
      6
S:cr_enable      0
S:ld_nondata_cr  6          tnodep
0xbb8410e0
S:tx_credits[0]  0  0  0  0  0  0  0  0
S:tx_credits[8]  0  0  0  0  0  0  0  0
S:tx_credits[16] 0  0  0  0  0  0  0  0  0
S:tx_credits[24] 0  0  0  0  0  0  0  0  0
S:tx_credits[32] 0  0  0  0  0  0  0  0  0
S:rx_credits[0]  0  0  0  0  0  0  0  0
S:rx_credits[8]  0  0  0  0  0  0  0  0
S:rx_credits[16] 0  0  0  0  0  0  0  0  0
S:rx_credits[24] 0  0  0  0  0  0  0  0  0
S:rx_credits[32] 0  0  0  0  0  0  0  0  0
S:tx_mbc[0]      0  0  0  0  0  0  0  0
S:tx_mbc[8]      0  0  0  0  0  0  0  0
S:tx_mbc[16]     0  0  0  0  0  0  0  0
S:tx_mbc[24]     0  0  0  0  0  0  0  0
S:tx_mbc[32]     0  0  0  0  0  0  0  0
S:rx_mbc[0]      0  0  0  0  0  0  0  0
S:rx_mbc[8]      0  0  0  0  0  0  0  0
S:rx_mbc[16]     0  0  0  0  0  0  0  0
S:rx_mbc[24]     0  0  0  0  0  0  0  0
S:rx_mbc[32]     0  0  0  0  0  0  0  0
S:
S:C4 Chip Variables: c4_phyp->c4_chp = 0x97e28000
S:-----
S:version = 2.1
S:magic_id        0xc4234567  init_state          0x8
S:reset_reg_mem  0x1
S:ch_int0_en_bm  0x0          intr0_cause          0x0
S:ch_int1_en_bm  0x0          intr1_cause          0x0
S:ch_int2_en_bm  0x0          intr2_cause          0x0
S:ch              0x43010080  ch_cfg
0xb7013ba0
S:raslog_hndl.hndl 0x0          obj_halted          0x0

```

| | | | |
|---------------------------|-----------------------|-------------------------|-----|
| S:c4_chip_regp | 0x80000000 | c4_fpg_regp | |
| 0x81800000 | | | |
| S:num_chip_timer | 0x5 | | |
| S:hi_task_bm | 0x0 | lo_task_bm | 0x0 |
| S:c4_deferq.q_head | 0x0 | c4_deferq.q_tail | 0x0 |
| S:c4_tmrq.q_head | 0x0 | c4_tmrq.q_tail | 0x0 |
| slot_no | 0 | | |
| S:chip_inst | 0 | chip_idx | 0 |
| S:pll_initialized | 1 | | |
| pll_serdes_initialized | 1 | | |
| S:init_tries | 0 | init_ptEnableBM | |
| 0xba01b488 | | | |
| S:tick_polling | 0xb980c9c0 | sec_polling | |
| 0xb980c960 | | | |
| S:bb_fid | 129 | | |
| S:ecb_key_bm[0] | 0x0 | ecb_key_bm[1] | 0x0 |
| S:ecb_key_bm[2] | 0x0 | ecb_key_bm[3] | 0x0 |
| S:is_chip_enc_enabled | | 0 | |
| is_chip_comp_enabled | 0x0 | | |
| S:ftb_rsrcp->ftb_flags | 0x0 | act_rsrcp->act_flag | 0x1 |
| S:lue_rsrcp->lue_flags[0] | 0x0 | lue_rsrcp->lue_flags[1] | 0x0 |
| S:c4_phyp[00]: | 0xb6ab0000 0xb6ab2080 | 0xb6ab4100 0xb6ab6180 | |
| S:c4_phyp[04]: | 0xb6ab9040 0xb6abb0c0 | 0xb6abd140 0xb6ac0000 | |
| S:c4_phyp[08]: | 0xb6ac2080 0xb6ac4100 | 0xb6ac6180 0xb6ac9040 | |
| S:c4_phyp[12]: | 0xb6acb0c0 0xb6acd140 | 0xb6ad0000 0xb6ad2080 | |
| S:c4_phyp[16]: | 0xb6ad4100 0xb6ad6180 | 0xb6ad9040 0xb6adb0c0 | |
| S:c4_phyp[20]: | 0xb6add140 0xb6ae0000 | 0xb6ae2080 0xb6ae4100 | |
| S:c4_phyp[24]: | 0xb6ae6180 0xb6ae9040 | 0xb6aeb0c0 0xb6aed140 | |
| S:c4_phyp[28]: | 0xb6af0000 0xb6af2080 | 0xb6af4100 0xb6af6180 | |
| S:c4_phyp[32]: | 0xb6af9040 0xb6afb0c0 | 0xb6afd140 0xb6b00000 | |
| S:c4_phyp[36]: | 0xb6b02080 0xb6b04100 | 0xb6b06180 0xb6b09040 | |
| S:c4_phyp[40]: | 0xb6b0b0c0 0xb6b0d140 | 0xb6b10000 0xb6b12080 | |
| S:c4_phyp[44]: | 0xb6b14100 0xb6b16180 | 0xb6b19040 0xb6b1b0c0 | |
| S:c4_phyp[48]: | 0xb6b1d140 0xb6b20000 | 0xb6b22080 0xb6b24100 | |
| S:c4_phyp[52]: | 0xb6b26180 0xb6b29040 | 0xb6b2b0c0 0xb6b2d140 | |
| S:c4_phyp[56]: | 0xb6b30000 0xb6b32080 | 0xb6b34100 0xb6b36180 | |
| S:c4_phyp[60]: | 0xb6b39040 0xb6b3b0c0 | 0xb6b3d140 0xb6b40000 | |
| S:c4_lgcp[00]: | 0x97f48000 0x97f4c000 | 0x97f50000 0x97f54000 | |
| S:c4_lgcp[04]: | 0x97f58000 0x97f5c000 | 0x97f60000 0x97f64000 | |
| S:c4_lgcp[08]: | 0x97f68000 0x97f6c000 | 0x97f70000 0x97f74000 | |
| S:c4_lgcp[12]: | 0x97f78000 0x97f7c000 | 0x97f80000 0x97f84000 | |
| S:c4_lgcp[16]: | 0x97f88000 0x97f8c000 | 0x97f90000 0x97f94000 | |
| S:c4_lgcp[20]: | 0x97f98000 0x97f9c000 | 0x97fa0000 0x97fa4000 | |
| S:c4_lgcp[24]: | 0x97fa8000 0x97fac000 | 0x97fb0000 0x97fb4000 | |
| S:c4_lgcp[28]: | 0x97fb8000 0x97fbc000 | 0x97fc0000 0x97fc4000 | |
| S:c4_lgcp[32]: | 0x97fc8000 0x97fcc000 | 0x97fd0000 0x97fd4000 | |
| S:c4_lgcp[36]: | 0x97fd8000 0x97fdc000 | 0x97fe0000 0x97fe4000 | |
| S:c4_lgcp[40]: | 0x97fe8000 0x97fec000 | 0x97ff0000 0x97ff4000 | |
| S:c4_lgcp[44]: | 0x97ff8000 0x97ffc000 | 0x8e000000 0x8e004000 | |
| S:c4_lgcp[48]: | 0x8e008000 0x8e00c000 | 0x8e010000 0x8e014000 | |
| S:c4_lgcp[52]: | 0x8e018000 0x8e01c000 | 0x8e020000 0x8e024000 | |
| S:c4_lgcp[56]: | 0x8e028000 0x8e02c000 | 0x8e030000 0x8e034000 | |
| S:c4_lgcp[60]: | 0x8e038000 0x8e03c000 | 0x8e040000 0x8e044000 | |

```

S:chip_timers[00]: 0xb980c720 0xb980c780 0xb980c7e0 0xb980c840
S:chip_timers[04]: 0xb980c8a0 0xb980c900
S:disc_trap_enable_required      0x0          rxlp_disc_log_stop
      0x0
S:curr_rxlp_frm_cnt      0x0          curr_rxlp_disc_frm_cnt  0x0
S:sw_disc_frm_cnt      0x0          last_disc_frm_cnt      0x0
S:txq_nopop_pr_cnt      0x0          pollErrataDfe_ptBM
0xba01b4b0
S:ftb_rsrpc->chip_ref[FTB_REF_CHP_EC][0]      0x0
ftb_rsrpc->chip_ref[FTB_REF_CHP_EC][1] 0x0
S:ftb_rsrpc->chip_ref[FTB_REF_CHP_EC][2]      0x0
ftb_rsrpc->chip_ref[FTB_REF_CHP_NRC][0] 0x0
S:ftb_rsrpc->chip_ref[FTB_REF_CHP_NRC][1]      0x0
ftb_rsrpc->chip_ref[FTB_REF_CHP_NRC][2] 0x0

```

S:
S:C4 Logical Port Variables

S:-----

```

S:c4_lgc_regp      0x81c98000
S:c4_phyp:
S:      0xb6adb0c0      0x0          0x0          0x0

S:      0x0          0x0          0x0          0x0

S:master_phyp      0xb6adb0c0      if_id
0x43020013
S:min_phyp      0x0          max_phyp      0x0
S:num_phy_ports      1          lgc_num      19
S:num_iu_to      0          sw_txq_bm
      0
S:port_fid      128          unused      0
S:port_group      2          lgc_stats_clear_ts
      1725611419
S:domain_tbl_sel      0          area_tbl_sel
      0
S:egid_tbl_sel      0
S:serv_lo_bm      0x0

```

S:
S:Proto Phy Variables:

S:-----

```

S:magic_id      0xc4123456      asic_phyp
0xb6adb0c0
S:port_id      0x43028013      phy_cfg
      0xb6adc100
S:upsm_hdl      0xb8015b40      physm_hdl
0xb80158c0
S:ov_sns_hdl      0xb8015780      sw_sns_hdl
0xb8015820
S:ov_lks_hdl      0xb8015960      sw_lks_hdl
0xb8015a00
S:trks_hdl      0xb8015aa0      lr_flag      0x0
S:lr_active      0x0          qsfpxrx_rate_sel
      0x0

```



```

S:
S:UPSM      UP00: UPST_PORT_DISABLED    --> UP01:
UPST_START_PORT_INIT
S:SNSM(OV)  SN00: 0V_SNST_STOPPED           --> SN00: 0V_SNST_STOPPED
S:SNSM(SW)  SW00: SW_SNST_STAGE_WS      --> SW00: SW_SNST_STAGE_WS
S:PHYSM     UNKNOWN    --> PP03: PHYST_NO_SIGNAL
S:LKSM(OV)  LK00: 0V_LKST_INACTIVE      --> LK00: 0V_LKST_INACTIVE
S:LKSM(SW)  SW13: INACTIVE              --> SW13: INACTIVE
S:TRKSM     TRK0: TRKST_INIT            --> TRK0: TRKST_INIT

```

```

S:
S:physm variables:

```

```

S:-----
-----
S:proto_phyp      0xb8809a20      physm_hdl
0xb80158c0
S:force_offline   0              copper              0
S:fault_reason    0: UNKNOWN
S:phy_media_present      1
S:

```

```

S:sns variables:

```

```

S:-----
-----
S:speed           0xff           proto_phyp
0xb8809a20
S:hw_sn_tries_left      0x0           sw_sn_tries_left      0x0
S:curr_txsp_count      0x0
S:tx_max             0x0           curr_tx_indx
      0x0
S:curr_tx            0x0           curr_rxsp_count
      0x0
S:rx_max             0x0           curr_rx_indx
      0x0
S:curr_rx            0x0           rx_mem
      0x0
S:rxsp_rec_count      0x0
S:nc_start           0x0           tx_start              0x0
S:sync_start         0x0           sync_present          0x0
S:diag_auto          0x0           diag_speed            0xff
S:striped_wd_tov     3000           hw_wd_tov
      3000
S:step              0x0           qsfp28_speed_mode
      0x0
S:qsfp_mode0_hw_sn_tries_left      0x0
S:qsfp_mode1_hw_sn_tries_left      0x0
S:

```

```

S:lksm variables:

```

```

S:-----
-----
S:proto_phyp      0xb8809a20      ov_lksm_hdl
0xb8015960
sw_lksm_hdl      0xb8015a00
num_lf1          0
S:hw_link_tries_left  0              sw_link_tries_left    0
S:buf_ptype       0x0           stored_entry_state     0x6

```

```

S:handshake_owner          0x0          mark_unsent
   0x0
S:busybuf_stuck           0x0          lr_wait          0x0
S:
S:trksm variables:
S:-----
-----
S:Not a trunk port
S:
S:upsm variables:
S:-----
-----
S:proto_phyph             0xb8809a20      upsm_hdl
0xb8015b40
S:bb_credits              0              port_beacon      0
S:port_diag_flag         0              force_offline
0
S:port_fault_rsn         0: PORT_NO_FAULT
S:retry_init_rsn         0: UNKNOWN
S:limit_reason           0              limit_result     0
S:ie_fctl_mode           0              fec_in_sync_tries_left 0
S:retry_sn_fail_init     0
retry_link_fail_init     0
S:excess_lr_count        0
S:
S:c4_ch_cfg
S:-----
-----
S:c4_desc_ring_size      256          292          256          256          292
292          2          292          292
S:thresh_def             0              16            1            0
S:intr_tries             500          cmem_pattern
0xdeadbeef
S:cmem_pattern_upwd      2              cmem_init_time  16
S:cmem_init_tries        5
S:ctrl_par_thresh        2              data_par_thresh
4
S:cam_par_thresh         4              buf_loss_thresh
12
S:crit_par_thresh        2              non_crit_par_thresh
6
S:pci_abort_thresh       10            pci_err_thresh  5
S:excess_chintr_thresh  8              sw_err_thresh   20
S:err_sample_period      300          intr_sleep
20000
S:frame_timeout          2500          proxy_dev        16384
S:vf_route               81920         qos              2048
S:stats 2048             f_redirect     2048
S:rsp_trap               2048          lun_zoning       20480
S:area_mode              0              ftb_max_loop[0] 0
S:ftb_max_loop[1]        6              ftb_max_loop[2] 9
S:ftb_max_loop[3]        10            ftb_max_loop[4] 10
S:ftb_max_loop[5]        5              ftb_max_loop[6] 6
S:ftb_seg_size[0]        0              ftb_seg_size[1]

```

```

16384
S:ftb_seg_size[2]      65536      ftb_seg_size[3]
16384
S:ftb_seg_size[4]      16384      ftb_seg_size[5]
65536
S:ftb_seg_size[6]      16384      ftb_seg_base[0]      0
S:ftb_seg_base[1]      0          ftb_seg_base[2]
65536
S:ftb_seg_base[3]      16384      ftb_seg_base[4]
32768
S:ftb_seg_base[5]      131072     ftb_seg_base[6]
49152
asic_err_monitor_period1      300
asic_err_monitor_period2      86400
zone_chk_to_poll_period 25
zone_chk_class2_reject_tov    220
S:
S:c4_phy_cfg
S:-----
-----
S:version = 2.1
S:pt      0x43028013      fab_ptr
0x9a800000
S:fabattr      0x9a8000d4      fab_iop
      0x9a800050
S:cfgbm      0xbb840e04      port_ctrl
0xb6adc118
S:pcap.pcap_bm      0x8d215547      pcap.pcap2_bm
0x588289
S:pcap.pcap3_bm      0x1bea60c
ui_idx      46      S:slot_no
      0
is_icl      0      S:sw_usr_ports      400
S:neg_speed      0 0 0 0 0 0
S:my_domain      0x1      port_mode      0x0
S:hw_sn_maxtries      100      sw_sn_maxtries
      0
S:hw_link_maxtries      10      sw_link_maxtries      5
S:rx_cyc_tov      28      rttov      300
S:bufrdy_tov      300      busybuf_tov      286
S:mark_tov      300      lksm_tov      3000
S:buf_dealloc_wait      4      hw_wd_tov      3000
S:hw_lk_train_tov      540      hw_lk_test_tov
      150
S:syswait_tx_12_lips      1      lip_rx_tov      55
S:al_time_tov      15      lp_tov      2000
S:intr_tries_port      500      intr_mod_debounce
      250
S:intr_lsrflt_debounce      500      intr_efifo_debounce      100
S:port_no_fid      3      excess_ptintr_thresh      8
S:port_fault1_thresh      100      port_fault1_spur_thresh      250
S:port_fault1_disc_thresh      500
port_fault1_disc_spur_thresh      1000
S:port_fault2_thresh      5      losync_tov      100

```

```

S:port_sw_link_to          15          en_8g_scramble
   1
frc_hw_sn_mode             0x1
S:enc_poll_thresh         0          fec_enable
   0
S:fec_in_sync_to          50          fec_in_sync_try_max
   4
S:port_be_lto_threshold    100         port_be_lr_threshold
   2
S:be_cr_in_sync_to        5
port_credit_overrun_thresh 10
S:jda_sfp_losig_tov       400
jda_sfp_losig_try_max     30
S:striped_wd_tov          3000
no_sync_debounce          1200
S:
S:      fab_iop
S:=====
S:fab_iop->interop_mode 0x0          fab_iop->lab_mode      0x0
S:fab_iop->fl_bbc        0x0          fab_iop->fl_fan
   0x0
S:fab_iop->fl_cls        0x4          fab_iop->fl_rscn
   0x0
S:fab_iop->domain_id_offset 0x60         fab_iop-
>mcmt_fabric_mode      0x0
S:fab_iop->mcmt_default_zone 0x0          fab_iop-
>mcmt_safe_zone        0x0
S:
S:      port_ctrl
S:=====
S:port_ctrl.port_type    1          port_ctrl.port_grp    2
S:port_ctrl.port_number 46          port_ctrl.vc_mode      1
S:
S:      port_ctrl.lcap
S:=====
S:has_serdes             0          has_media              1
S:topology               1          skip_nego              0
S:skip_pnego             0          skip_init_event        0
S:en_shim                 0          speed_neg
   1
S:loop_back              0          num_speeds             5
S:fec_enable              0
S:
S:      port_ctrl.speed_list array
S:=====
S:speed_list[0].auto_neg 1          speed_list[0].lnk_speed 0x0000000a
S:speed_list[1].auto_neg 1          speed_list[1].lnk_speed 0x00000008
S:speed_list[2].auto_neg 0          speed_list[2].lnk_speed 0x00000006
S:speed_list[3].auto_neg 1          speed_list[3].lnk_speed 0x00000005
S:speed_list[4].auto_neg 0          speed_list[4].lnk_speed 0x00000003
S:speed_list[5].auto_neg 0          speed_list[5].lnk_speed 0x00000000
S:
S:      port_ctrl.cm
S:=====

```

```

S:port_ctrl.cm.num_vcs          8
S:port_ctrl.cm.min_bufs        8
S:port_ctrl.cm.cr_shar_bufs    0
S:port_ctrl.vc_alloc
S:port_ctrl.vc_alloc          2 0 1 1 1 1 1 1
S:port_ctrl.vc_alloc          0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.norm_vc_alloc
S:port_ctrl.norm_vc_alloc      4 0 5 5 5 5 1 1
S:port_ctrl.norm_vc_alloc      0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.cm.skip_bb_credit  0
S:port_ctrl.cm.use_shim_based_sublist 0
S:
S:      port_ctrl.serdes_set
S:=====
S:serdes_type                  0x8
S:serdes_data_t.ibm_hss_serdes.tx_drive_power      0x1
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b_sign 0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b      0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_a      0x0
S:serdes_data_t.ibm_hss_serdes.rxeq                0x0
S:
S:      cfgbm
S:=====
S:old_distance                  0x0          gport_lockdown      0x0
S:tport                        0x1          speed                0x0
S:disable_eport                0x0          fcacc                0x0
S:lport_lockdown               0x0          priv_lport_lockdown
0x0
S:vcxlt_linit                  0x0          delay_flogi         0x0
S:isl_interop                  0x0          distance             0x0
S:BufStarvFlag                 0x0          credit_sharing      0x0
S:lport_halfduplex             0x0          lport_fairness      0x0
S:soft_neg                     0x0          asn_frc_hwretry     0x0
S:cr_recov                     0x0          fport_buffers       0x0
S:export                        0x0          export_mode
0x0
S:csctl_en                     0x0          mirror_port         0x0
S:fault_delay                  0x0          non_dfe              0x0
S:fec_configured*(0=ENAB)      0          fec_tts
0
S:port_persistently_disabled (permanently) 0 (0)
S:
S:      cfg property
S:=====
S:priv_pcfg_bm                  0x00000000      lgcl_pcfg_bm
0xbb840e44
S:fport_buffer                  0x00000000
S:
S:
S:C4 Discard Cntrs: rxlp_stats = 0xb6adb470
S:-----
-----

```

```

S:disc_mcast_wka          0x0          disc_inv_did          0x0
S:disc_cl1_cl4           0x0          disc_sid_chk_fail    0x0
S:disc_inv_dom_egid_txpt 0x0          disc_vft_hop_cnt_1
    0x0
S:disc_classf            0x0          disc_fcp_cdb_inv     0x0
S:disc_vfid_trap_enabled 0x0
disc_vfid_hdr_chk_fail 0x0
S:disc_shim_cksum_fail   0x0          disc_fed_edit_cmd_err 0x0
S:disc_shim_cksum_fail   0x0          disc_fed_edit_cmd_err 0x0
S:disc_ftb_vm_mode       0x0          disc_ftb_agn_t2_miss 0x0
S:disc_ecb_de_pad_err    0x0          disc_ecb_de_tag_err   0x0
S:disc_ecb_de_seq_err    0x0          disc_ecb_err          0x0
S:disc_ftb_type4_match   0x0          disc_fcp_rsp_ftb_type4 0x0
S:disc_fcp_rsp_ftb_type4 0x0          disc_ftb_type5_match
    0x0
S:disc_ftb_type3_match   0x0          disc_els_ftb_type3   0x0
S:disc_ftb_type1_match   0x0          disc_els_rsp_ex_port  0x0
S:disc_inv_drp_dps       0x0          disc_did_lookup_miss  0x0
S:disc_ftb_type2_match   0x0          disc_trpd_plogi_pdisc 0x0
S:disc_type2_lookup_miss 0x0          disc_ftb_type6_match
    0x0
S:disc_els_rep_ex_port   0x0          disc_els_sid_lkup_bit1 0x0
S:disc_els_sid_lkup_bit0 0x0
disc_bls_frm_trap_bit1 0x0
S:disc_ftb_token_err     0x0          disc_asic_internal_err 0x0
S:disc_hard_zone_miss    0x0          disc_lun_zone_miss    0x0
S:discflt_frame_disc     0x0          discflt_parity_err    0x0
S:disc_frame_marked_du   0x0          disc_frame_marked_to  0x0
E:Connection type: FE
E:Port type: F_port
E:Trunk port: No
E:Configured Speed: AUTO_SPEED_NEGO
E:Max Capable Speed: 32G
E:Current SNSM Speed: UNDEFINED
E:Hardware TX Speed: 32G (0x00000004)
E:Hardware RX Speed: 32G (0x00000040)
E:
E:Interrupts: 0          Link_failure: 0
Loss_of_sync: 0          Loss_of_sig: 0
E:Lli: 0                Invalid_word: 0
E:trapped_frm: 0          fwd_status_ok: 0
E:fwd_timeout: 0          fwd_tx_unavail: 0
E:fwd_unroutable: 0          fwd_zone_out: 0
E:fwd_other_err: 0          frm_err_discard: 0
E:Fltr listA: 0          Fltr listB: 0
E:Zone trap fwd: 0          Zone trap disc: 0
E:shim_csum: 0           RTE_perr: 0
E:Invalid_crc: 0          Delim_err: 0
E:Protocol_err: 0
E:Lr_in: 0               Lr_out: 0
E:Ols_in: 0              Ols_out: 0

```

filterportshow 46

FILTER DATA

Shadow settings:

Filter Enable: 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass: 0x00000000

Real settings:

Enable RAM: 0x00000000, 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000

Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass RAM: 0x00000000

Shadowed filters:

Filter 0: Not Installed (MIRROR1)(LISTA)
c4_fldenable[0] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[0] = 0x00000000,c4_fltr_config[0] = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
c4_fldenable[1] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[1] = 0x00000000,c4_fltr_config[1] = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
c4_fldenable[2] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[2] = 0x00000000,c4_fltr_config[2] = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
c4_fldenable[3] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[3] = 0x00000000,c4_fltr_config[3] = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
c4_fldenable[4] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[4] = 0x00000000,c4_fltr_config[4] = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
c4_fldenable[5] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[5] = 0x00000000,c4_fltr_config[5] = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
c4_fldenable[6] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[6] = 0x00000000,c4_fltr_config[6] = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
c4_fldenable[7] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[7] = 0x00000000,c4_fltr_config[7] = 0x00000000

Filter 8: Not Installed (FICON CUP)(LISTA)
c4_fldenable[8] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[8] = 0x00000000,c4_fltr_config[8] = 0x00000000

Filter 9: Not Installed (FICON CUP DST)(LISTA)
c4_fldenable[9] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[9] = 0x00000000,c4_fltr_config[9] = 0x00000000

Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
c4_fldenable[10] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[10] = 0x00000000,c4_fltr_config[10] =
0x00000000

Filter 11: Not Installed (SIM)(LISTA)
c4_fldenable[11] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[11] = 0x00000000,c4_fltr_config[11] =
0x00000000

Filter 12: Not Installed (UNUSED)(LISTA)
c4_fldenable[12] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[12] = 0x00000000,c4_fltr_config[12] =
0x00000000

Filter 13: Not Installed (UNUSED)(LISTA)
c4_fldenable[13] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[13] = 0x00000000,c4_fltr_config[13] =
0x00000000

Filter 14: Not Installed (UNUSED)(LISTA)
c4_fldenable[14] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[14] = 0x00000000,c4_fltr_config[14] =
0x00000000

Filter 15: Not Installed (UNUSED)(LISTA)
c4_fldenable[15] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[15] = 0x00000000,c4_fltr_config[15] =
0x00000000

Filter 16: Not Installed (PERF1)(LISTA)
c4_fldenable[16] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[16] = 0x00000000,c4_fltr_config[16] =
0x00000000

Filter 17: Not Installed (PERF2)(LISTA)
c4_fldenable[17] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[17] = 0x00000000,c4_fltr_config[17] =
0x00000000

Filter 18: Not Installed (PERF3)(LISTA)
c4_fldenable[18] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[18] = 0x00000000,c4_fltr_config[18] =
0x00000000

Filter 19: Not Installed (PERF4)(LISTA)

```
    c4_fldenable[19] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[19] = 0x00000000,c4_fltr_config[19] =
0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
    c4_fldenable[20] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[20] = 0x00000000,c4_fltr_config[20] =
0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
    c4_fldenable[21] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[21] = 0x00000000,c4_fltr_config[21] =
0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
    c4_fldenable[22] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[22] = 0x00000000,c4_fltr_config[22] =
0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
    c4_fldenable[23] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[23] = 0x00000000,c4_fltr_config[23] =
0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
    c4_fldenable[24] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[24] = 0x00000000,c4_fltr_config[24] =
0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
    c4_fldenable[25] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[25] = 0x00000000,c4_fltr_config[25] =
0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
    c4_fldenable[26] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[26] = 0x00000000,c4_fltr_config[26] =
0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
    c4_fldenable[27] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[27] = 0x00000000,c4_fltr_config[27] =
0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
    c4_fldenable[28] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[28] = 0x00000000,c4_fltr_config[28] =
0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
    c4_fldenable[29] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[29] = 0x00000000,c4_fltr_config[29] =
0x00000000
```

Filter 30: Not Installed (IPM1)(LISTA)
c4_fldenable[30] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[30] = 0x00000000,c4_fltr_config[30] =
0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
c4_fldenable[31] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[31] = 0x00000000,c4_fltr_config[31] =
0x00000000

Real filters:

Filter 0: Not Installed (MIRROR1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 11: Not Installed (SIM)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 12: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 13: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 14: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 15: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 16: Not Installed (PERF1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 17: Not Installed (PERF2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 18: Not Installed (PERF3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 19: Not Installed (PERF4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 20: Not Installed (PERF5)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 21: Not Installed (PERF6)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 22: Not Installed (PERF7)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 23: Not Installed (PERF8)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,

```

0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter dirty indicator: 0x00000000
Performance filters: 0
Port Mirror filters: 0 (0x0)

```

FIELD DATA

Shadowed fields:

```

fldoffset[0] = 0x00, fldmask[0] = 0x00, fldvalue_dyna[0]: 0x00 0x00
0x00 0x00
fldcontrol[0].inuse = 0x0  fldcontrol[0].refcnt = 0x00 0x00 0x00
0x00
fldoffset[1] = 0x00, fldmask[1] = 0x00, fldvalue_dyna[1]: 0x00 0x00
0x00 0x00
fldcontrol[1].inuse = 0x0  fldcontrol[1].refcnt = 0x00 0x00 0x00
0x00
fldoffset[2] = 0x00, fldmask[2] = 0x00, fldvalue_dyna[2]: 0x00 0x00

```

```
0x00 0x00
fldcontrol[2].inuse = 0x0  fldcontrol[2].refcnt = 0x00 0x00 0x00
0x00
fldoffset[3] = 0x00, fldmask[3] = 0x00, fldvalue_dyna[3]:0x00 0x00
0x00 0x00
fldcontrol[3].inuse = 0x0  fldcontrol[3].refcnt = 0x00 0x00 0x00
0x00
fldoffset[4] = 0x00, fldmask[4] = 0x00, fldvalue_dyna[4]:0x00 0x00
0x00 0x00
fldcontrol[4].inuse = 0x0  fldcontrol[4].refcnt = 0x00 0x00 0x00
0x00
fldoffset[5] = 0x00, fldmask[5] = 0x00, fldvalue_dyna[5]:0x00 0x00
0x00 0x00
fldcontrol[5].inuse = 0x0  fldcontrol[5].refcnt = 0x00 0x00 0x00
0x00
fldoffset[6] = 0x00, fldmask[6] = 0x00, fldvalue_dyna[6]:0x00 0x00
0x00 0x00
fldcontrol[6].inuse = 0x0  fldcontrol[6].refcnt = 0x00 0x00 0x00
0x00
fldoffset[7] = 0x00, fldmask[7] = 0x00, fldvalue_dyna[7]:0x00 0x00
0x00 0x00
fldcontrol[7].inuse = 0x0  fldcontrol[7].refcnt = 0x00 0x00 0x00
0x00
fldoffset[8] = 0x00, fldmask[8] = 0x00, fldvalue_dyna[8]:0x00 0x00
0x00 0x00
fldcontrol[8].inuse = 0x0  fldcontrol[8].refcnt = 0x00 0x00 0x00
0x00
fldoffset[9] = 0x00, fldmask[9] = 0x00, fldvalue_dyna[9]:0x00 0x00
0x00 0x00
fldcontrol[9].inuse = 0x0  fldcontrol[9].refcnt = 0x00 0x00 0x00
0x00
fldoffset[10] = 0x00, fldmask[10] = 0x00, fldvalue_dyna[10]:0x00 0x00
0x00 0x00
fldcontrol[10].inuse = 0x0  fldcontrol[10].refcnt = 0x00 0x00 0x00
0x00
fldoffset[11] = 0x00, fldmask[11] = 0x00, fldvalue_dyna[11]:0x00 0x00
0x00 0x00
fldcontrol[11].inuse = 0x0  fldcontrol[11].refcnt = 0x00 0x00 0x00
0x00
fldoffset[12] = 0x00, fldmask[12] = 0x00, fldvalue_dyna[12]:0x00 0x00
0x00 0x00
fldcontrol[12].inuse = 0x0  fldcontrol[12].refcnt = 0x00 0x00 0x00
0x00
fldoffset[13] = 0x00, fldmask[13] = 0x00, fldvalue_dyna[13]:0x00 0x00
0x00 0x00
fldcontrol[13].inuse = 0x0  fldcontrol[13].refcnt = 0x00 0x00 0x00
0x00
fldoffset[14] = 0x00, fldmask[14] = 0x00, fldvalue_dyna[14]:0x00 0x00
0x00 0x00
fldcontrol[14].inuse = 0x0  fldcontrol[14].refcnt = 0x00 0x00 0x00
0x00
fldoffset[15] = 0x00, fldmask[15] = 0x00, fldvalue_dyna[15]:0x00 0x00
0x00 0x00
fldcontrol[15].inuse = 0x0  fldcontrol[15].refcnt = 0x00 0x00 0x00
```

```
0x00
fldoffset[16] = 0x00, fldmask[16] = 0x00, fldvalue_dyna[16]: 0x00 0x00
0x00 0x00
fldcontrol[16].inuse = 0x0 fldcontrol[16].refcnt = 0x00 0x00 0x00
0x00
fldoffset[17] = 0x00, fldmask[17] = 0x00, fldvalue_dyna[17]: 0x00 0x00
0x00 0x00
fldcontrol[17].inuse = 0x0 fldcontrol[17].refcnt = 0x00 0x00 0x00
0x00
fldoffset[18] = 0x00, fldmask[18] = 0x00, fldvalue_dyna[18]: 0x00 0x00
0x00 0x00
fldcontrol[18].inuse = 0x0 fldcontrol[18].refcnt = 0x00 0x00 0x00
0x00
fldoffset[19] = 0x00, fldmask[19] = 0x00, fldvalue_dyna[19]: 0x00 0x00
0x00 0x00
fldcontrol[19].inuse = 0x0 fldcontrol[19].refcnt = 0x00 0x00 0x00
0x00
```

Real fields:

```
fldoffset RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000
fldmask RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000
fld value4 RAM:
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
Field dirty indicator: 0x00000000
```

```
FDB reference count fdb: 0 [0 0 0 0 ]
FDB reference count fdb: 1 [0 0 0 0 ]
FDB reference count fdb: 2 [0 0 0 0 ]
FDB reference count fdb: 3 [0 0 0 0 ]
FDB reference count fdb: 4 [0 0 0 0 ]
FDB reference count fdb: 5 [0 0 0 0 ]
FDB reference count fdb: 6 [0 0 0 0 ]
```

FDB reference count fdb: 7 [0 0 0 0]
FDB reference count fdb: 8 [0 0 0 0]
FDB reference count fdb: 9 [0 0 0 0]
FDB reference count fdb: 10 [0 0 0 0]
FDB reference count fdb: 11 [0 0 0 0]
FDB reference count fdb: 12 [0 0 0 0]
FDB reference count fdb: 13 [0 0 0 0]
FDB reference count fdb: 14 [0 0 0 0]
FDB reference count fdb: 15 [0 0 0 0]
FDB reference count fdb: 16 [0 0 0 0]
FDB reference count fdb: 17 [0 0 0 0]
FDB reference count fdb: 18 [0 0 0 0]
FDB reference count fdb: 19 [0 0 0 0]

Filter counters:

Filter counter 0: 0 (MIRROR1)
Filter counter 1: 0 (MIRROR2)
Filter counter 2: 0 (MIRROR3)
Filter counter 3: 0 (MIRROR4)
Filter counter 4: 0 (AEPORT_NON_MIRR_DROP)
Filter counter 5: 0 (ZONING TRAP)
Filter counter 6: 0 (FCR_EXPORT_DC)
Filter counter 7: 0 (TIN TRAP)
Filter counter 8: 0 (FICON CUP)
Filter counter 9: 0 (FICON CUP DST)
Filter counter 10: 0 (WELL KNOWN ADDR)
Filter counter 11: 0 (SIM)
Filter counter 12: 0 (UNUSED)
Filter counter 13: 0 (UNUSED)
Filter counter 14: 0 (UNUSED)
Filter counter 15: 0 (UNUSED)
Filter counter 16: 0 (PERF1)
Filter counter 17: 0 (PERF2)
Filter counter 18: 0 (PERF3)
Filter counter 19: 0 (PERF4)
Filter counter 20: 0 (PERF5)
Filter counter 21: 0 (PERF6)
Filter counter 22: 0 (PERF7)
Filter counter 23: 0 (PERF8)
Filter counter 24: 0 (PERF9)
Filter counter 25: 0 (PERF10)
Filter counter 26: 0 (PERF11)
Filter counter 27: 0 (PERF12)
Filter counter 28: 0 (OPM1)
Filter counter 29: 0 (OPM2)
Filter counter 30: 0 (IPM1)
Filter counter 31: 0 (IPM2)

ACL DATA

Logical port 19: Hard Zoning disabled, Soft Zoning disabled
Zone type: WWN Zoning
Frames with hard zone miss: 0

*** Please use filterportshow on user port 56 to display ACL hash tables and Mirroring resources of thischip.
***We show this data only for the first physical port which is an external port.

portFcPortCmdShow --slot 0 47 3
doing portFcPortCmdShow: arg1 = 3, arg2 = -2

portshow 47
portDisableReason: None
portCFlags: 0x1
portFlags: 0x1 PRESENT U_PORT
LocalSwcFlags: 0x0
portType: 26.0
POD Port: Port is licensed
portState: 2 Offline
Protocol: FC
portPhys: 4 No_Light portScn: 2 Offline
port generation number: 0
state transition count: 1

portId: 012f00
portIfId: 43020010
portWwn: 20:2f:d8:1f:cc:2c:99:90
portWwn of device(s) connected:
16b Area list:
Distance: normal
portSpeed: N32Gbps

FEC: Inactive
Credit Recovery: Inactive
LE domain: 0
Peer beacon: Off
FC Fastwrite: OFF

| | | | | |
|-------------|---|---------------|---|-------|
| Interrupts: | 0 | Link_failure: | 0 | Frjt: |
| 0 | | | | |
| Unknown: | 0 | Loss_of_sync: | 0 | Fbsy: |
| 0 | | | | |
| Lli: | 0 | Loss_of_sig: | 0 | |
| Proc_rqrd: | 0 | Protocol_err: | 0 | |
| Timed_out: | 0 | Invalid_word: | 0 | |
| Tx_unavail: | 0 | Invalid_crc: | 0 | |
| Delim_err: | 0 | Address_err: | 0 | |
| Lr_in: | 0 | Ols_in: | 0 | |
| Lr_out: | 0 | Ols_out: | 0 | |

portloginshow 47
Type PID World Wide Name credit df_sz cos
=====

portloginshow 47 -history
Type PID World Wide Name logout time

=====
portregshow 47

LED registers

=====

| | | |
|---------------------------|----------|-------------|
| 0x81c82000: c4_led_status | 00000000 | 0x81c82004: |
| c4_led_ctl | 00000000 | |

FPL registers

=====

| | | |
|---------------------------------|----------|-------------|
| 0x81c80200: fpl_port_config | 23298002 | |
| 0x81c8020c: fpl_port_id_ctl | 00000000 | 0x81c80210: |
| fpl_port_id_addr | 00012f00 | |
| 0x81c80214: fpl_port_speed | 00000004 | 0x81c8021c: |
| fpl_lli_ctl | 00000100 | |
| 0x81c80228: fpl_lli_os_ctl | bc94ffff | 0x81c8022c: |
| fpl_lli_send_word | bc95b5b5 | |
| 0x81c80230: fpl_lli_mark_rx | 00000000 | 0x81c80234: |
| fpl_lli_rnd_trip_time | 00000000 | |
| 0x81c80238: fpl_lli_ns_status | 00130007 | 0x81c8023c: |
| fpl_lli_intr_status | 00030007 | |
| 0x81c80244: fpl_lli_def | 00100000 | 0x81c80254: |
| fpl_lli_intr_enable_clr | 001c0000 | |
| 0x81c80258: fpl_err_intr_status | 00000000 | 0x81c80260: |
| fpl_err_intr_enable_clr | 00000000 | |
| 0x81c80268: fpl_err_first_error | 00000000 | 0x81c8026c: |
| fpl_speed_neg_ctl | 00000000 | |
| 0x81c80270: fpl_speed_neg_stat | 00000000 | 0x81c80274: |
| fpl_softasn_ctl | 0000000f | |
| 0x81c80278: fpl_link_init_ctl | 00000000 | 0x81c8027c: |
| fpl_link_init_stat | 00000000 | |
| 0x81c80280: fpl_aec_ctl | 001c1060 | 0x81c80284: |
| fpl_aec_ctl2 | 04009f60 | |
| 0x81c80288: fpl_pcs_ctl | 00000170 | 0x81c8028c: |
| fpl_fec_ctl | 00000424 | |
| 0x81c80290: fpl_fec_cor | 00000000 | 0x81c80294: |
| fpl_fec_uncor | 00000000 | |
| 0x81c80298: fpl_hss_link_ctl | 0031f040 | 0x81c8029c: |
| fpl_afifo_link_ctl | 00000a86 | |
| 0x81c802a0: fpl_echo_lb_ctl | 0000028c | 0x81c802a4: |
| fpl_scratch | 00000121 | |
| 0x81c802a8: fpl_debug | 00060005 | 0x81c802ac: |
| fpl_misc_debug | 00000800 | |
| 0x00000000: SW_shadow_reg | 00000000 | 0x00000000: |
| SW_c4_phyp->cfgptr | 00030003 | |

per-fpg (per octet) registers

=====

| | | |
|------------------------------|----------|-------------|
| 0x8181382c: fpg_serdes_ctla0 | 81a37be7 | 0x81813830: |
| fpg_serdes_ctla1 | 81a37be7 | |
| 0x81813834: fpg_serdes_ctlb0 | 81a1c3c3 | 0x81813838: |
| fpg_serdes_ctlb1 | 81a1c3c3 | |

```

0x8181383c: fpg_serdes_xgmii_1ms      00067c28      0x81813840:
fpg_serdes_regtimctl      40e47946
0x81813844: fpg_serdes_asnrsttimctl 00000102

```

HSS PLL registers

```

=====
0x81811400: 00_hssplla_vco_coarse_cal0      00000000      0x81811404:
01_hssplla_vco_coarse_cal1      00000014
0x81811408: 02_hssplla_vco_coarse_cal2      00000000      0x8181140c:
03_hssplla_vco_coarse_cal3      00000000
0x81811410: 04_hssplla_vco_coarse_cal4      00000000      0x81811424:
09_hssplla_power_ctl      00000000
0x81811428: 0A_hssplla_charge_pump_ctl      00000004      0x81811438:
0E_hssplla_pll_misc_ctl      00000000
0x8181143c: 0F_hssplla_pclk_ctl      000000f8      0x81811440:
10_hssplla_eyem_intv_ctl      00000000
0x81811444: 11_hssplla_eyem_intv_lim1      00000000      0x81811448:
12_hssplla_eyem_intv_lim2      00000000
0x8181144c: 13_hssplla_eyem_intv_lim3      00000000      0x81811450:
14_hssplla_eyem_intv_lim4      00000000
0x818114f0: 3C_hssplla_macro_tst_ctl4      00000000      0x818114f4:
3D_hssplla_macro_tst_ctl3      00000000
0x818114f8: 3E_hssplla_macro_tst_ctl2      00000000      0x818114fc:
3F_hssplla_macro_tst_ctl1      00000000
0x81811500: 00_hsspllb_vco_coarse_cal0      0000000a      0x81811504:
01_hsspllb_vco_coarse_cal1      00000014
0x81811508: 02_hsspllb_vco_coarse_cal2      00000000      0x8181150c:
03_hsspllb_vco_coarse_cal3      00000000
0x81811510: 04_hsspllb_vco_coarse_cal4      00000000      0x81811524:
09_hsspllb_power_ctl      00000000
0x81811528: 0A_hsspllb_charge_pump_ctl      00000004      0x81811538:
0E_hsspllb_pll_misc_ctl      00000000
0x8181153c: 0F_hsspllb_pclk_ctl      000000f8      0x81811540:
10_hsspllb_eyem_intv_ctl      00000000
0x81811544: 11_hsspllb_eyem_intv_lim1      00000000      0x81811548:
12_hsspllb_eyem_intv_lim2      00000000
0x8181154c: 13_hsspllb_eyem_intv_lim3      00000000      0x81811550:
14_hsspllb_eyem_intv_lim4      00000000
0x818115f0: 3C_hsspllb_macro_tst_ctl4      00000000      0x818115f4:
3D_hsspllb_macro_tst_ctl3      00000000
0x818115f8: 3E_hsspllb_macro_tst_ctl2      00000000      0x818115fc:
3F_hsspllb_macro_tst_ctl1      00000000

```

HSS TX registers

```

=====
0x81810000: 00_hsstx_cfg_mode_PHY      00009f48      0x81810004:
01_hsstx_test_ctl      00000000
0x81810008: 02_hsstx_coeff_ctl_INV      00000000      0x8181000c:
03_hsstx_drv_mode_ctl      00000000
0x81810010: 04_hsstx_drv_ovrd_ctl      00000010      0x81810014:
05_hsstx_dclk_align_ovrd      00000080
0x81810018: 06_hsstx_imp_cal_ovrd      00000c0c      0x8181001c:
07_hsstx_dclk_drift_tol      00000004
0x81810020: 08_hsstx_tap0_coeff_TUNE      00000000      0x81810024:

```

| | | | |
|---|----------|-------------|--|
| 09_hsstx_tap1_coeff_TUNE | 00000003 | | |
| 0x81810028: 0A_hsstx_tap2_coeff_TUNE | 00000019 | 0x8181002c: | |
| 0B_hsstx_tap3_coeff_TUNE | 00000003 | | |
| 0x81810034: 0D_hsstx_pol_INV | 00000004 | 0x81810038: | |
| 0E_hsstx_ae_cmd | 00000000 | | |
| 0x8181003c: 0F_hsstx_ae_stat | 00000000 | 0x81810040: | |
| 10_hsstx_ae_tap0_TUNE | 00000000 | | |
| 0x81810044: 11_hsstx_ae_tap1_TUNE | 00000000 | 0x81810048: | |
| 12_hsstx_ae_tap2_TUNE | 00000028 | | |
| 0x8181004c: 13_hsstx_ae_tap3_TUNE | 00000000 | 0x81810054: | |
| 15_hsstx_app_tune | 0000120e | | |
| 0x81810058: 16_hsstx_analog_diag | 00000000 | 0x81810060: | |
| 18_hsstx_4x_seg_app | 0000aa00 | | |
| 0x81810064: 19_hsstx_2x_seg_app | 000000aa | 0x81810068: | |
| 1A_hsstx_1x_seg_app | 0000f5e4 | | |
| 0x8181006c: 1B_hsstx_seg_4x_term_app | 0000000f | 0x81810070: | |
| 1C_hsstx_seg_2x1x_term_app | 00000001 | | |
| 0x81810074: 1D_hsstx_tap_sign_app | 00000004 | 0x81810078: | |
| 1E_hsstx_ext_addr_data | 00000001 | | |
| 0x8181007c: 1F_hsstx_ext_addr_addr | 00000000 | 0x81810080: | |
| 20_hsstx_pat_buf_bytes_1_0 | 00000000 | | |
| 0x81810084: 21_hsstx_pat_buf_bytes_3_2 | 00000000 | 0x81810088: | |
| 22_hsstx_pat_buf_bytes_5_4 | 00000000 | | |
| 0x8181008c: 23_hsstx_pat_buf_bytes_7_6 | 00000000 | 0x8181009c: | |
| 27_hsstx_8023az_ctl | 00000000 | | |
| 0x818100a0: 28_hsstx_dcc_ctl | 000060c0 | 0x818100a4: | |
| 29_hsstx_dcc_ovrd | 00000000 | | |
| 0x818100a8: 2A_hsstx_dcc_app | 00000000 | 0x818100ac: | |
| 2B_hsstx_dcc_timeout | 0000ffff | | |
| 0x818100c0: 30_hsstx_tap_sign_ovrd | 00000000 | 0x818100c8: | |
| 32_hsstx_seg_4x_ovrd | 00000000 | | |
| 0x818100cc: 33_hsstx_seg_2x_ovrd | 00000000 | 0x818100d0: | |
| 34_hsstx_seg_1x_ovrd | 00000000 | | |
| 0x818100d8: 36_hsstx_tap_seg_4x_term_ovrd | 00000000 | 0x818100dc: | |
| 37_hsstx_tap_seg_2x_term_ovrd | 00000000 | | |
| 0x818100e0: 38_hsstx_tap_seg_1x_term_ovrd | 00000000 | 0x818100ec: | |
| 3B_hsstx_mac_test_ctl5 | 00000000 | | |
| 0x818100f0: 3C_hsstx_mac_test_ctl4 | 00000000 | 0x818100f4: | |
| 3D_hsstx_mac_test_ctl3 | 00000000 | | |
| 0x818100f8: 3E_hsstx_mac_test_ctl2 | 00000000 | 0x818100fc: | |
| 3F_hsstx_mac_test_ctl1 | 000000c6 | | |

HSS RX registers

=====

| | | | |
|---------------------------------------|----------|-------------|--|
| 0x81810200: 00_hssrx_cfg_mode_PHY | 00009e78 | 0x81810204: | |
| 01_hssrx_test_ctl | 00000000 | | |
| 0x81810208: 02_hssrx_phs_rot_ctl | 0000cb80 | 0x8181020c: | |
| 03_hssrx_phs_rot_ofs_ctl | 00000610 | | |
| 0x81810210: 04_hssrx_phs_rot_posn1 | 00000201 | 0x81810214: | |
| 05_hssrx_phs_rot_posn2 | 00000031 | | |
| 0x81810218: 06_hssrx_phs_rot_sta_ofs1 | 00000101 | 0x8181021c: | |
| 07_hssrx_phs_rot_sta_ofs2 | 00000000 | | |
| 0x81810220: 08_hssrx_dfe_ctl_PHY | 00002002 | 0x81810224: | |
| 09_hssrx_dfe_smpl_snap1 | 00000000 | | |

| | | |
|--|----------------|-------------|
| 0x81810228: 0A_hssrx_dfe_smpl_snap2 | 00008000 | 0x8181022c: |
| 0B_hssrx_vga_ctl1 | 00004001 | |
| 0x81810230: 0C_hssrx_vga_ctl2 | 00007aa0 | 0x81810234: |
| 0D_hssrx_vga_ctl3 | 000009e4 | |
| 0x81810238: 0E_hssrx_pwr_mgmt_ctl | 0000001f | 0x8181023c: |
| 0F_hssrx_iqamp_ctl1 | 0000001b | |
| 0x81810240: 10_hssrx_iqamp_ctl2 | 00000001 | 0x81810244: |
| 11_hssrx_dacap_dacan_sel | 00000003 | |
| 0x81810248: 12_hssrx_dacap_dacan | 00000000 | 0x8181024c: |
| 13_hssrx_daca_min | 00000000 | |
| 0x81810250: 14_hssrx_adac_ctl | 00000000 | 0x81810254: |
| 15_hssrx_ac_cp_ctl | 000031c3 | |
| 0x81810258: 16_hssrx_ac_cp_val | 00000051 | 0x8181025c: |
| 17_hssrx_dfe_h1h2h3_lcl_off_ch | 00000014 | |
| 0x81810260: 18_hssrx_dfe_h1h2h3_lcl_off_val | 00000000 | 0x81810264: |
| 19_hssrx_peaked_intg | 000000ff | |
| 0x81810268: 1A_hssrx_cdr_analog_sw | 0000ce00 | 0x8181026c: |
| 1B_hssrx_peaking_amp_init_c_PHY | 00000000 | |
| 0x81810270: 1C_hssrx_dac_dpc | 00000040 | 0x81810274: |
| 1D_hssrx_ddc | 00000000 | |
| 0x81810278: 1E_hssrx_int_stat_PHY | 00000c0f | 0x8181027c: |
| 1F_hssrx_dfe_func_ctl1_PHY | 0000ffff | |
| 0x81810280: 20_hssrx_dfe_func_ctl2_INV | 00007eff | 0x81810284: |
| 21_hssrx_ofs_ch_dcc_qcc_idx | 00002000 | |
| 0x81810288: 22_hssrx_dfe_ofs_val | 0000027b | 0x8181028c: |
| 23_hssrx_h_coeff_bist | 00000401 | |
| 0x81810290: 24_hssrx_ac_cap_bist | 00000000 | 0x81810294: |
| 25_hssrx_max_gain_path_idx_res | 00007800 | |
| 0x81810298: 26_hssrx_loff_ctl | 00000040 | 0x8181029c: |
| 27_hssrx_sigdet_ctl | 00002a80 | |
| 0x818102a0: 28_hssrx_ana_ctl_sw | 00000000 | 0x818102a4: |
| 29_hssrx_intg_dac_ofs | 0000e0de | |
| 0x818102a8: 2A_hssrx_eye_ctl | 00000000 | 0x818102ac: |
| 2B_hssrx_eye_met | 00000004 | |
| 0x818102b0: 2C_hssrx_eye_met_err_cnt | 00000000 | 0x818102b4: |
| 2D_hssrx_eye_met_pdf_eyec | 00000000 | |
| 0x818102b8: 2E_hssrx_eye_met_pat_len | 0000007f | 0x818102bc: |
| 2F_hssrx_dfe_func_ctl3 | 0000dfff | |
| 0x818102c0: 30_hssrx_dfe_tap_ctl_idx_ptr | 00000008 | 0x818102c4: |
| 31_hssrx_dfe_tap | 00003030 | |
| 0x818102c8: 32_hssrx_lte_ctl_TUNE | 00001601 | 0x818102e4: |
| 39_hssrx_int_stat2 | 0000c1ff | |
| 0x818102e8: 3A_hssrx_ac_cpl_cur_src_adj | 00000041 | 0x818102ec: |
| 3B_hssrx_dcd_ctl | 00007c47 | |
| 0x818102f0: 3C_hssrx_dcc_ctl | 00000d82 | 0x818102f4: |
| 3D_hssrx_qcc_ctl | 00006983 | |
| 0x818102f8: 3E_hssrx_mac_test_ctl2 | 00000000 | 0x818102fc: |
| 3F_hssrx_mac_test_ctl1 | 00000000 | |
| 0x81810248: 12_hssrx_dacap_dacan[02] | 00fe 0000 | |
| 0x81810260: 18_hssrx_dfe_h1h2h3_lcl_off_va[00] | 0000 0000 0000 | |
| 0000 0000 0000 0000 0000 | | |
| 0x81810260: 18_hssrx_dfe_h1h2h3_lcl_off_va[08] | 0000 0000 0000 | |
| 0000 0000 0000 0000 0000 | | |
| 0x81810260: 18_hssrx_dfe_h1h2h3_lcl_off_va[16] | 0000 0000 0000 | |

```

0000 0000
0x81810288: 22_hssrx_dfe_ofs_val[00][00] 027b 7f00 7f09
7f7f 017a 7f00
0x81810288: 22_hssrx_dfe_ofs_val[03][00] 7b07 007f 7b79
0000 7d7e 7f00
0x81810288: 22_hssrx_dfe_ofs_val[06][00] 0b05 7f7f 0979
7f00 7a06 007f
0x81810288: 22_hssrx_dfe_ofs_val[09][00] 0603 7f7f 0106
0000 7f7f 0000
0x81810288: 22_hssrx_dfe_ofs_val[12][00] 0501 0000 7f07
0000 0305 0000
0x81810288: 22_hssrx_dfe_ofs_val[15][00] 0107 0000 027d
0000 7e02 0000
0x81810288: 22_hssrx_dfe_ofs_val[18][00] 7b03 0100 0779
0000 007e 0000
0x81810288: 22_hssrx_dfe_ofs_val[21][00] 007e 0000 007e
0000 007e 0000
0x81810288: 22_hssrx_dfe_ofs_val[24][00] 7f07 007f 7a7d
017f 757a 0000
0x81810294: 25_hssrx_max_gain_path_idx_res[00] 005d 0858 1103
1887 20e0 28aa 308b 3800
0x81810294: 25_hssrx_max_gain_path_idx_res[08] 40c0 4890 5079
5800 6040 6800 70fd 7800
0x818102c4: 31_hssrx_dfe_tap[00] fffe 8080 0000
0000 0030 0030 3030 3030
0x818102c4: 31_hssrx_dfe_tap[08] 3030 3030 3030
0000
0x818102e8: 3A_hssrx_ac_cpl_cur_src_adj[00] 0041 0041 0041
0041
0x818102ec: 3B_hssrx_dcd_ctl[00] 7c47 5c00 7c41
5c00 7c00
0x818102f0: 3C_hssrx_dcc_ctl[00] 0d82 0d81 0d82
0d43
0x818102f4: 3D_hssrx_qcc_ctl[00] 6945 6983

```

xfipcs, fec, aec, & aet registers

=====

```

0x81c80400: xfipcs_reg [00] 00002040 00000080 00000000
00000000 00000001 00000008 00000000 00000000
0x81c80420: xfipcs_reg [08] 00008401 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c80440: xfipcs_reg [16] 00000000 00000000 00000000
00000000 00000040 00000000 00000000 00000000
0x81c80460: xfipcs_reg [24] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c80480: xfipcs_reg [32] 00000004 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c80620: fec_32g_128g_reg [08] 00000000 00008003 00000000
00000000 00000000 00000000 00000000
0x81c80648: fec_32g_128g_reg [18] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c80a00: aec_reg [00] 00000000 00000000 00000000
00000000 00000040 00000000 00000000 00002490
0x81c80c00: aet_reg [00] 000000b0 00007000 000008c4

```

00000000 00000000

bbc registers

=====

| | | | | | | | |
|---------------------------|----------|---|---|---|---|---|----------------------|
| 0x81c81800: bbc_trc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c81840: bbc_trc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c81880: bbc_trc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c818c0: bbc_trc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c81900: bbc_trc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c81804: bbc_mbc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c81844: bbc_mbc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c81884: bbc_mbc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c818c4: bbc_mbc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c81904: bbc_mbc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c81a00: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c81a20: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c81a40: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c81a60: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c81a80: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c81c00: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c81c20: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c81c40: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c81c60: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c81c80: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c81d00: bbc_fbpc | 00000000 | | | | | | 0x81c81d04: bbc_csc |
| 00000000 | | | | | | | |
| 0x81c81d08: bbc_rcc_inc | 00000000 | | | | | | 0x81c81d0c: |
| bbc_rqc_inc | 00000000 | | | | | | |
| 0x81c81d10: bbc_fbpc_inc | 00000000 | | | | | | 0x81c81d14: |
| bbc_tmc_inc | 00000000 | | | | | | |
| 0x81c81d18: bbc_threshold | 00080100 | | | | | | 0x81c81d1c: |
| bbc_counter_clr | 00000000 | | | | | | |
| 0x81c81d20: bbc_debug_en | 00000000 | | | | | | 0x81c81d24: bbc_ctrl |
| 00200120 | | | | | | | |

| | | |
|-------------------------------------|----------|-------------|
| 0x81c81d28: bbc_rqc_rcc_thresh | 00000055 | 0x81c81d34: |
| bbc_bb_sc_n | 00000000 | |
| 0x81c81d38: bbc_crd_reco_debug | 00000000 | 0x81c81d3c: |
| bbc_crd_reco_debug_data | 00000000 | |
| 0x81c81d40: bbc_multi_frm_loss_cnt | 00000000 | 0x81c81d44: |
| bbc_multi_rdy_loss_cnt | 00000000 | |
| 0x81c81d48: bbc_1frm_loss_recov_cnt | 00000000 | 0x81c81d4c: |
| bbc_1rdy_loss_recov_cnt | 00000000 | |
| 0x81c81d58: bbc_int_status | 00000000 | 0x81c81d5c: |
| bbc_int_set | 00000000 | |
| 0x81c81d60: bbc_int_first | 00000000 | 0x81c81d64: |
| bbc_frm_rdy_rx_err_addr | 00000000 | |
| 0x81c81d68: bbc_frm_rdy_tx_err_addr | 00000000 | 0x81c81d6c: |
| bbc_trc_mbc_err_addr | 00000000 | |
| 0x81c81d70: bbc_frm_rdy_rx_dbl_ecc | 00000000 | 0x81c81d74: |
| bbc_frm_rdy_tx_dbl_ecc | 00000000 | |
| 0x81c81d78: bbc_trc_mbc_dbl_ecc | 00000000 | |
| 0x81c81d7c: bbc_fsm_status | 00001011 | 0x81c81d80: |
| bbc_force_err | 00000000 | |
| 0x81c81d84: bbc_crdt_avail0 | 00000000 | 0x81c81d88: |
| bbc_crdt_avail1 | 00000000 | |
| 0x81c81d8c: bbc_scratch | 00000000 | |

FPS registers

=====

| | | |
|--------------------------------|----------|-------------|
| 0x81c80004: fps_er_enc_in | 00000000 | 0x81c80008: |
| fps_er_crc | 00000000 | |
| 0x81c8000c: fps_er_trunc | 00000000 | 0x81c80010: |
| fps_er_toolong | 00000000 | |
| 0x81c80014: fps_er_bad_eof | 00000000 | 0x81c80018: |
| fps_er_enc_out | 00000000 | |
| 0x81c8001c: fps_er_bad_os | 00000000 | 0x81c80020: |
| fps_er_flush | 00000000 | |
| 0x81c80024: fps_er_ifg | 00000000 | 0x81c80038: |
| fps_er_crc_good_eof | 00000000 | |
| 0x81c8003c: fps_inv_arb | 00000000 | 0x81c80040: |
| fps_slow_sts_status | 00000000 | |
| 0x81c80044: fps_tx_frm_cnt | 00000000 | 0x81c80048: |
| fps_rx_frm_cnt | 00000000 | |
| 0x81c80050: fps_tx_word_cnt_hi | 00000000 | 0x81c8004c: |
| fps_tx_word_cnt_lo | 00000000 | |
| 0x81c80058: fps_rx_word_cnt_hi | 00000000 | 0x81c80054: |
| fps_rx_word_cnt_lo | 00000000 | |

BAL registers

=====

| | | |
|---------------------------------|----------|-------------|
| 0x81c87000: bal_desired_buf | 00000000 | 0x81c87004: |
| bal_alloc_buf | 00000000 | |
| 0x81c87008: bal_busy_buf | 00000000 | 0x81c8700c: |
| bal_usable_buf | 00000000 | |
| 0x81c87010: bal_max_bor_buf | 00000000 | |
| 0x81c87014: bal_busy_buf_thresh | 00000002 | |

TXQ registers

=====

0x81c83004: txq_phys_port_ctl 00400000
0x81c83050: txq_link_skew 00000000
0x81c83068: txq_cr_lk_dttm_intr_sts [00] 00000000 00000000
0x81c83070: txq_cr_lk_dttm_intr_en [00] 00000000 00000000
0x81c83024: txq_disc_frm_trap_cnt 00000014

FDS registers

=====

0x81c84000: fds_rxf_ctl 00000002 0x81c84004:
fds_rxf_wait_thresh 00000909
0x81c84018: fds_rxf_first_error 00000000 0x81c8401c:
fds_rxf_first_error_info 00000000
0x81c84020: fds_rxf_inout_pkt_cnt 00000000
0x81c84008: fds_rxf_err_int_status 00000000 0x81c84024:
fds_rxf_fifo_status 00888888
0x81c85000: fds_txf_ctl 0000003a 0x81c85004:
fds_txf_wait_ifg_thresh 00a00106
0x81c85008: fds_txf_err_int_status 00000000 0x81c85024:
fds_txf_fifo_status 00088888
0x81c8502c: fds_txf_bbc_scs 00000000

Logical TXQ registers

=====

0x81c83000: txq_log_port_ctl 00000002 0x81c83008:
txq_port_status 00000000
0x81c8300c: txq_todo_flags [00] 00000000 00000000
0x81c83014: txq_spd_match_desc [00] 00000000 00000000 00000000
00000000
0x81c83024: txq_spd_match_desc [04] 00000014
0x81c83028: txq_vc_weight [00] 01010101 01010101 01010101
01010101
0x81c83038: txq_vc_weight [04] 01010101 01010101 01010101
01010101
0x81c83048: txq_vc_weight [08] 01010101 00010101
0x81c83054: txq_cong_dttm_ctrl 00000106
0x81c83058: txq_cong_dttm_intr_sts [00] 00000000 00000000
0x81c83060: txq_cong_dttm_intr_en [00] 00000000 00000000
0x81c83078: txq_bw_limit_en_reg [00] 00000000 00000000
0x81c83080: txq_bw_gua_en_reg [00] 00000000 00000000
0x81c83088: txq_vc_group [00] 03030300 03030303 03030303
03030303
0x81c83098: txq_vc_group [04] 03030303 03030303 03030303
03030303
0x81c830a8: txq_vc_group [08] 03030303 03030303 00000000
00000000
0x81c830b0: txq_bw_thresh_group [00] 00000000 00000000 00000000
00000000
0x81c830c0: txq_bw_thresh_group [04] 00000000 00000000 00000000
00000000
0x81c830d0: txq_bw_thresh_group [08] 00000000 00000000 00000000
00000000
0x81c830e0: txq_bw_thresh_group [12] 00000000 00000000 00000000
00000000

```

0x81c830f0: txq_bw_thresh_group    [16] 00000000 00000000 00000000
00000000
0x81c83100: txq_bw_thresh_group    [20] 00000000 00000000 00000000
00000000
0x81c83110: txq_bw_thresh_group    [24] 00000000 00000000 00000000
00000000
0x81c83120: txq_bw_thresh_group    [28] 00000000 00000000 00000000
00000000
0x81c83130: txq_bw_thresh_group    [32] 00000000 00000000 00000000
00000000
0x81c83140: txq_bw_thresh_group    [36] 00000000 00000000 00000000
00000000

```

txq Congestion detection Statistics RAM

=====

```

0x81090a00: vc[0]          00000000          0x81090a04: vc[1]
00000000
0x81090a08: vc[2]          00000000          0x81090a0c: vc[3]
00000000
0x81090a10: vc[4]          00000000          0x81090a14: vc[5]
00000000
0x81090a18: vc[6]          00000000          0x81090a1c: vc[7]
00000000
0x81090a20: vc[8]          00000000          0x81090a24: vc[9]
00000000
0x81090a28: vc[10]         00000000          0x81090a2c: vc[11]
00000000
0x81090a30: vc[12]         00000000          0x81090a34: vc[13]
00000000
0x81090a38: vc[14]         00000000          0x81090a3c: vc[15]
00000000
0x81090a40: vc[16]         00000000          0x81090a44: vc[17]
00000000
0x81090a48: vc[18]         00000000          0x81090a4c: vc[19]
00000000
0x81090a50: vc[20]         00000000          0x81090a54: vc[21]
00000000
0x81090a58: vc[22]         00000000          0x81090a5c: vc[23]
00000000
0x81090a60: vc[24]         00000000          0x81090a64: vc[25]
00000000
0x81090a68: vc[26]         00000000          0x81090a6c: vc[27]
00000000
0x81090a70: vc[28]         00000000          0x81090a74: vc[29]
00000000
0x81090a78: vc[30]         00000000          0x81090a7c: vc[31]
00000000
0x81090a80: vc[32]         00000000          0x81090a84: vc[33]
00000000
0x81090a88: vc[34]         00000000          0x81090a8c: vc[35]
00000000
0x81090a90: vc[36]         00000000          0x81090a94: vc[37]
00000000
0x81090a98: vc[38]         00000000          0x81090a9c: vc[39]

```

00000000

Logical STS registers

=====

| | | | |
|-------------|----------------------|----------------|------------------|
| 0x81584c84: | sts_ftb_type1_miss | 00000000 | |
| 0x81584c88: | sts_ftb_type2_miss | 00000000 | |
| 0x81584c8c: | sts_ftb_type6_miss | 00000000 | |
| 0x81584c90: | sts_hard_zoning_miss | 00000000 | |
| 0x81584c94: | sts_lun_zoning_miss | 00000000 | |
| 0x81584c9c: | sts_unroutable | 00000000 | |
| 0x81581cb4: | sts_rte_cl2 | 00000000 | 0x81581cb8: |
| sts_rte_cl3 | 00000000 | 0x81581cbc: | sts_rte_link_ctl |
| 00000000 | 0x81584ca8: | sts_tx_timeout | 00000000 |

Logical STS filter registers

=====

| | | | | | |
|-------------|-------------|------|----------|----------|----------|
| 0x81584c00: | stsflt_trig | [00] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | | |
| 0x81584c10: | stsflt_trig | [04] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | | |
| 0x81584c20: | stsflt_trig | [08] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | | |
| 0x81584c30: | stsflt_trig | [12] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | | |
| 0x81584c40: | stsflt_trig | [16] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | | |
| 0x81584c50: | stsflt_trig | [20] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | | |
| 0x81584c60: | stsflt_trig | [24] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | | |
| 0x81584c70: | stsflt_trig | [28] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | | |
| 0x81584c80: | stsflt_trig | [32] | | | |

Logical STS discard registers

=====

| | | | |
|------------------------|------------------------|----------|-------------|
| 0x81582740: | disc_mcast_wka | 00000000 | 0x81582744: |
| disc_inv_did | 00000000 | | |
| 0x81582748: | disc_cl1_cl4 | 00000000 | 0x8158274c: |
| disc_sid_chk_fail | 00000000 | | |
| 0x81582750: | disc_inv_dom_egid_txpt | 00000000 | 0x81582754: |
| disc_vft_hop_cnt_1 | 00000000 | | |
| 0x81582758: | disc_classf | 00000000 | 0x8158275c: |
| disc_fcp_cdb_inv | 00000000 | | |
| 0x81582760: | disc_vfid_trap_enabled | 00000000 | 0x81582764: |
| disc_vfid_hdr_chk_fail | 00000000 | | |
| 0x81582768: | disc_shim_cksum_fail | 00000000 | 0x8158276c: |
| disc_fed_edit_cmd_err | 00000000 | | |
| 0x81582770: | disc_ftb_vm_mode | 00000000 | 0x81582774: |
| disc_ftb_agnt2_miss | 00000000 | | |
| 0x81582778: | disc_ecb_reserved | 00000000 | 0x8158277c: |
| disc_ecb_de_pad_err | 00000000 | | |
| 0x81582780: | disc_ecb_de_tag_err | 00000000 | 0x81582784: |

```

disc_ecn_de_seq_err      00000000
0x81582788: disc_ecn_err      00000000      0x8158278c:
disc_ftb_type4_match    00000000
0x81582790: disc_fcp_rsp_ftb_type4 00000000      0x81582794:
disc_ftb_type5_match    00000000
0x81582798: disc_ftb_type3_match 00000000      0x8158279c:
disc_els_ftb_type3      00000000
0x815827a0: disc_ftb_type1_match 00000000      0x815827a4:
disc_els_rsp_ex_port    00000000
0x815827a8: disc_inv_drp_dps      00000000      0x815827ac:
disc_did_lookup_miss    00000000
0x815827b0: disc_ftb_type2_match 00000000      0x815827b4:
disc_trpd_plogi_pdisc   00000000
0x815827b8: disc_type2_lookup_miss 00000000      0x815827bc:
disc_ftb_type6_match    00000000
0x815827c0: disc_els_rep_ex_port 00000000      0x815827c4:
disc_els_sid_lkup_bit1  00000000
0x815827c8: disc_els_sid_lkup_bit0 00000000      0x815827cc:
disc_bls_frm_trap_bit1  00000000
0x815827d0: disc_ftb_token_err    00000000      0x815827d4:
disc_asic_internal_err  00000000
0x815827d8: disc_hard_zone_miss    00000000      0x815827dc:
disc_lun_zone_miss      00000000
0x815827e0: discflt_frame_disc    00000000      0x815827e4:
discflt_parity_err      00000000
0x815827e8: disc_frame_marked_du 00000000      0x815827ec:
disc_frame_marked_to    00000000
0x815827f0: disc_lkup_rte_prty_err 00000000

```

portstatsshow 47

```

stat_wtx      0      4-byte words transmitted
stat_wrx      0      4-byte words received
stat_ftx      0      Frames transmitted
stat_frx      0      Frames received
stat_c2_frx   0      Class 2 frames received
stat_c3_frx   0      Class 3 frames received
stat_lc_rx    0      Link control frames
received
stat_mc_rx    0      Multicast frames
received
stat_mc_to    0      Multicast timeouts
stat_mc_tx    0      Multicast frames
transmitted
tim_txcrd_z   0      Time TX Credit Zero
(2.5Us ticks)
tim_txcrd_z_vc 0- 3: 0      0      0      0
tim_txcrd_z_vc 4- 7: 0      0      0      0
tim_txcrd_z_vc 8-11: 0     0      0      0
tim_txcrd_z_vc 12-15: 0    0      0      0
lat_tot_pkt_vc 0- 3: 1      1      1      1
lat_tot_pkt_vc 4- 7: 1      1      1      1
lat_tot_pkt_vc 8-11: 1     1      1      1
lat_tot_pkt_vc 12-15: 1    1      1      1

```

| | | | | | |
|----------------|--------|---|---|---|---|
| lat_hi_time_vc | 0- 3: | 0 | 0 | 0 | 0 |
| lat_hi_time_vc | 4- 7: | 0 | 0 | 0 | 0 |
| lat_hi_time_vc | 8-11: | 0 | 0 | 0 | 0 |
| lat_hi_time_vc | 12-15: | 0 | 0 | 0 | 0 |
| lat_lo_time_vc | 0- 3: | 1 | 1 | 1 | 1 |
| lat_lo_time_vc | 4- 7: | 1 | 1 | 1 | 1 |
| lat_lo_time_vc | 8-11: | 1 | 1 | 1 | 1 |
| lat_lo_time_vc | 12-15: | 1 | 1 | 1 | 1 |
| max_latency_vc | 0- 3: | 1 | 1 | 1 | 1 |
| max_latency_vc | 4- 7: | 1 | 1 | 1 | 1 |
| max_latency_vc | 8-11: | 1 | 1 | 1 | 1 |
| max_latency_vc | 12-15: | 1 | 1 | 1 | 1 |

latency_dma_ts 09-09-2024 UTC Mon 08:47:25 TXQ

Latency DMA TimeStamp

| | | |
|------------------------------|---|-------------------------|
| fec_cor_detected | 0 | Count of blocks that |
| were corrected by FEC | | |
| fec_uncor_detected | 0 | Count of blocks that |
| were left uncorrected by FEC | | |
| er_enc_in | 0 | Encoding errors inside |
| of frames | | |
| er_crc | 0 | Frames with CRC errors |
| er_trunc | 0 | Frames shorter than |
| minimum | | |
| er_toolong | 0 | Frames longer than |
| maximum | | |
| er_bad_eof | 0 | Frames with bad end-of- |
| frame | | |
| er_enc_out | 0 | Encoding error outside |
| of frames | | |
| er_bad_os | 0 | Invalid ordered set |
| er_pcs_blk | 0 | PCS block errors |
| er_rx_c3_timeout | 0 | Class 3 receive frames |
| discarded due to timeout | | |
| er_tx_c3_timeout | 0 | Class 3 transmit frames |
| discarded due to timeout | | |
| er_unroutable | 0 | Frames that are |
| unroutable | | |
| er_unreachable | 0 | Frame with unreachable |
| destination | | |
| er_other_discard | 0 | Other discards |
| er_type1_miss | 0 | frames with FTB type 1 |
| miss | | |
| er_type2_miss | 0 | frames with FTB type 2 |
| miss | | |
| er_type6_miss | 0 | frames with FTB type 6 |
| miss | | |
| er_zone_miss | 0 | frames with hard zoning |
| miss | | |
| er_lun_zone_miss | 0 | frames with LUN zoning |
| miss | | |
| er_crc_good_eof | 0 | Crc error with good eof |
| er_inv_arb | 0 | Invalid ARB |
| er_single_credit_loss | 0 | Single vcrdy/frame loss |
| on link | | |

```

er_multi_credit_loss      0          Multiple vcrdy/frame
loss on link
other_credit_loss        0          Link timeout/complete
credit loss
phy_stats_clear_ts       09-06-2024 UTC Fri 08:30:19    Timestamp of
phy_port_stats_clear
lgc_stats_clear_ts       09-06-2024 UTC Fri 08:30:19    Timestamp of
lgc_port_stats_clear
fec_corrected_rate       0          FEC Corrected blocks per
second

```

```

portstats64show 47
stat64_wtx      0          top_int : 4-byte words transmitted
                0          bottom_int : 4-byte words transmitted
stat64_wrx      0          top_int : 4-byte words received
                0          bottom_int : 4-byte words received
stat64_ftx      0          top_int : Frames transmitted
                0          bottom_int : Frames transmitted
stat64_frx      0          top_int : Frames received
                0          bottom_int : Frames received
stat64_c2_frx   0          top_int : Class 2 frames received
                0          bottom_int : Class 2 frames received
stat64_c3_frx   0          top_int : Class 3 frames received
                0          bottom_int : Class 3 frames received
stat64_lc_rx    0          top_int : Link control frames received
                0          bottom_int : Link control frames
received
stat64_mc_rx    0          top_int : Multicast frames received
                0          bottom_int : Multicast frames received
stat64_mc_to    0          top_int : Multicast timeouts
                0          bottom_int : Multicast timeouts
stat64_mc_tx    0          top_int : Multicast frames transmitted
                0          bottom_int : Multicast frames
transmitted
tim64_rdy_pri   0          top_int : Time R_RDY high priority
                0          bottom_int : Time R_RDY high priority
tim64_txcrd_z   0          top_int : Time BB_credit zero
                0          bottom_int : Time BB_credit zero
er64_enc_in     0          top_int : Encoding errors inside of
frames
                0          bottom_int : Encoding errors inside of
frames
er64_crc        0          top_int : Frames with CRC errors
                0          bottom_int : Frames with CRC errors
er64_trunc      0          top_int : Frames shorter than minimum
                0          bottom_int : Frames shorter than minimum
er64_toolong    0          top_int : Frames longer than maximum
                0          bottom_int : Frames longer than maximum
er64_bad_eof    0          top_int : Frames with bad end-of-frame
                0          bottom_int : Frames with bad end-of-
frame
er64_enc_out    0          top_int : Encoding error outside of
frames
                0          bottom_int : Encoding error outside of

```

| | | | |
|---|---|------------|-------------------------------|
| frames | | | |
| er64_disc_c3 | 0 | top_int | : Class 3 frames discarded |
| | 0 | bottom_int | : Class 3 frames discarded |
| er64_pcs_blk | 0 | top_int | : PCS block errors |
| | 0 | bottom_int | : PCS block errors |
| stat64_rateTxFrame | 0 | | Tx frame rate (fr/sec) |
| stat64_rateRxFrame | 0 | | Rx frame rate (fr/sec) |
| stat64_rateTxPeakFrame | 0 | | Tx peak frame rate (fr/sec) |
| stat64_rateRxPeakFrame | 0 | | Rx peak frame rate (fr/sec) |
| stat64_rateTxWord | 0 | | Tx Word rate (words/sec) |
| stat64_rateRxWord | 0 | | Rx Word rate (words/sec) |
| stat64_rateTxPeakWord | 0 | | Tx peak Word rate (words/sec) |
| stat64_rateRxPeakWord | 0 | | Rx peak Word rate (words/sec) |
| stat64_PRJTFrames | 0 | top_int | : Number of PRJT frames |
| returned to this port | 0 | bottom_int | : Number of PRJT |
| frames returned to this port | 0 | | |
| stat64_PBSYFrames | 0 | top_int | : Number of PBSY frames |
| returned to this port | 0 | bottom_int | : Number of PBSY |
| frames returned to this port | 0 | | |
| stat64_inputBuffersFull | 0 | top_int | : Number of occurrences |
| when all input buffers full | 0 | bottom_int | : Number of |
| occurrences when all input buffers full | 0 | | |
| stat64_rxClass1Frames | 0 | top_int | : Number of class 1 |
| frames received | 0 | bottom_int | : Number of class 1 |
| frames received | 0 | | |
| stat64_aveTxFrameSize | 0 | | Average Tx Frame size |
| stat64_aveRxFrameSize | 0 | | Average Rx Frame size |
| Lr_in | 0 | top_int | |
| | 0 | bottom_int | |
| Ols_in | 0 | top_int | |
| | 0 | bottom_int | |
| Lr_out | 0 | top_int | |
| | 0 | bottom_int | |
| Ols_out | 0 | top_int | |
| | 0 | bottom_int | |
| Link_failure | 0 | top_int | |
| | 0 | bottom_int | |
| Invalid_CRC | 0 | top_int | |
| | 0 | bottom_int | |
| Invalid_word | 0 | top_int | |
| | 0 | bottom_int | |
| Protocol_err | 0 | top_int | |
| | 0 | bottom_int | |
| Loss_of_sig | 0 | top_int | |
| | 0 | bottom_int | |
| Loss_of_sync | 0 | top_int | |
| | 0 | bottom_int | |
| er_bad_os | 0 | top_int | : Invalid ordered set |
| | 0 | bottom_int | : Invalid ordered set |

```

portrouteshow 47
port address ID: 0x012f00
external unicast routing table:
    0: Embedded
    255: Embedded
internal unicast routing table:
    0: Embedded

```

```
portcamshow 47
```

```

-----
Port  SID used  DID used  SID entries  DID entries
47    0         0        000000      000000
-----

```

```
ptbufshow, ptcreditshow, ptdatashow, ptstatsshow 47
```

```

S:
S:VF Enable:          1
S:
S:C4 Global Variable:
S:-----

```

```

-----
S:trace_stop:        0
S:
S:C4 Phy Data Pointers: c4_phyp = 0xb6ad4100
S:-----

```

```

-----
S:tnodep              0xbb83d7e0      pt
    0x43028010
S:proto_phyp          0xb8809000      phy_cfg
0xb6ad5140
S:c4_chp              0x97e28000      c4_lgcp
0x97f88000
S:c4_phy_regp         0x81c80000      proc_dir
0xb8518d20
S:-----

```

```

-----
S:magic_id            0xc4345678      num_port_timer    12
S:prev_if_id         0x43020010      S:ftx              0
    tov              0
S:initialized         1                port_idx           16
S:ui_idx              47                slot_no
    0
S:blade_idx           16                sw_usr_ports       400
S:unused              0                intr_debounced
    0
S:aec_status          0x0              reason_code
    0
S:debug               0x00000004      debug_trc_line     0
S:rxbuf_list_head    0xffffffff      rxbuf_list_tail
0xffffffff
S:isAePort            0                port_misc_data
    0
S:num_fault1_rx_disc  0                num_fault2_rx_disc 0

```


| | | | | |
|------------------------------|-----|------------|-----------------------|-----|
| S:p_lli_cause0 | 0 | | p_sig_regained | 0 |
| S:p_sync_regained | | 0 | enc_out | |
| | 0x0 | | | |
| S:cached_fps_status | 0 | | cached_sts_status | 0 |
| S:cached_er_crc_good_eof | | 0 | | |
| S:cached_er_bad_os | 0 | | cached_er_too_long | 0 |
| S:cached_er_trunc | 0 | | | |
| cached_tot_er_crc_good_eof | | 0 | | |
| S:num_pt_excess_intr | 0 | | num_no_fid | 0 |
| S:num_fault1_cnt | | 0 | num_fault2_cnt | |
| | 0 | | | |
| S:num_fault_lip | 0 | | num_fault_lli | 0 |
| S:num_fault_rx_fifo | 0 | | num_fault_hss | 0 |
| S:num_fault_bwait | | 0 | lli_intr_prim | |
| | 0 | | | |
| S:num_sw_link_to | | 0 | | |
| be_link_err_mon_count | | 0 | | |
| S:ecb_enc_enabled | | 0 | ecb_comp_enabled | |
| | 0 | | | |
| S:ecb_rsv_enc | 0 | | ecb_rsv_comp | 0 |
| S:ecb_enc_bm | 0x0 | | ecb_key_index | |
| 0xffffffff | | | | |
| S:fab_idx | 0 | | | |
| S:num_be_lto | | 0 | lto_count_reset_intvl | |
| | 0 | | | |
| S:lr_count_reset_intvl | | 0 | num_be_lr | |
| | 0 | | | |
| S:num_fault_qsfm | | 0 | check_lto | |
| | 0 | | | |
| S:credit_loaded | | 0 | num_credit_overrun | |
| | 0 | | | |
| S:fec_enabled | 0x0 | | fec_los_to_flag | 0x0 |
| S:phy_stats_clear_ts | | 1725611419 | pcs_err_online | |
| | 0 | | | |
| S:pcs_err_light_det | | 0 | pcs_err_ignore | |
| | 0 | | | |
| S:pcs_blk_err | 0 | | pcs_hiber | 0 |
| S:phy_port_status | | 0 | ecb_enc_lr_count | |
| | 0 | | | |
| S:dport_mode | 0 | | avoid_lto_det | 0 |
| S:sn_debounced | 0x0 | | sn_started_kr_reqd | 0 |
| S:major_timer_started | 0x0 | | ready_bm | 0x0 |
| S:parln_1_bm | 0x0 | | parln_0_bm | 0x0 |
| S:be_los_of_sync_event_intvl | | | 0 | |
| be_los_of_sync_event | | 0 | | |
| S:errataPtenable_cntr | | 0 | errataPoll_cntr | |
| | 0 | | | |
| S:jda_rx_sig_loss_det | | 0 | jda_rx_sig_loss_cnt | |
| | 0 | | | |
| S:encrypt_blk_error | | 0 | | |
| S: | | | | |
| S: c4_trunk | | | | |
| S:===== | | | | |
| S:mark_ts | | 0x0 | deskew | 0x0 |

```

S:master_phyp          0x0
S:
S:adelay[00]: 0x00000000 0x00000000 0x00000000 0x00000000
S:adelay[04]: 0x00000000 0x00000000 0x00000000 0x00000000
S:
S:      c4_buf
S:=====
S:tx_csc                0                rx_csc
  0
S:ld_vc_credits        0                tx_flag                0x0
S:alloc_buffers        0                req_buffers            0
S:est_buffers          20               ld_use_est              0
S:bb_sc_n              0                rx_bb_sc_n
  0
S:data_cr              5                nondata_cr
  6
S:cr_enable            0
S:ld_nondata_cr        6                tnodep
0xbb83d8c0
S:tx_credits[0] 0    0    0    0    0    0    0    0
S:tx_credits[8] 0    0    0    0    0    0    0    0
S:tx_credits[16]    0    0    0    0    0    0    0    0    0
S:tx_credits[24]    0    0    0    0    0    0    0    0    0
S:tx_credits[32]    0    0    0    0    0    0    0    0    0
S:rx_credits[0] 0    0    0    0    0    0    0    0
S:rx_credits[8] 0    0    0    0    0    0    0    0
S:rx_credits[16]    0    0    0    0    0    0    0    0    0
S:rx_credits[24]    0    0    0    0    0    0    0    0    0
S:rx_credits[32]    0    0    0    0    0    0    0    0    0
S:tx_mbc[0] 0    0    0    0    0    0    0    0
S:tx_mbc[8] 0    0    0    0    0    0    0    0
S:tx_mbc[16] 0    0    0    0    0    0    0    0
S:tx_mbc[24] 0    0    0    0    0    0    0    0
S:tx_mbc[32] 0    0    0    0    0    0    0    0
S:rx_mbc[0] 0    0    0    0    0    0    0    0
S:rx_mbc[8] 0    0    0    0    0    0    0    0
S:rx_mbc[16] 0    0    0    0    0    0    0    0
S:rx_mbc[24] 0    0    0    0    0    0    0    0
S:rx_mbc[32] 0    0    0    0    0    0    0    0
S:
S:C4 Chip Variables: c4_phyp->c4_chp = 0x97e28000
S:-----
-----
S:version = 2.1
S:magic_id            0xc4234567        init_state            0x8
S:reset_reg_mem      0x1
S:ch_int0_en_bm      0x0                intr0_cause           0x0
S:ch_int1_en_bm      0x0                intr1_cause           0x0
S:ch_int2_en_bm      0x0                intr2_cause           0x0
S:ch                  0x43010080        ch_cfg
0xb7013ba0
S:raslog_hdl.hndl    0x0                obj_halted            0x0
S:c4_chip_regp       0x80000000        c4_fpg_regp
0x81800000

```

```

S:num_chip_timer          0x5
S:hi_task_bm             0x0          lo_task_bm             0x0
S:c4_deferq.q_head      0x0          c4_deferq.q_tail      0x0
S:c4_tmrq.q_head        0x0          c4_tmrq.q_tail        0x0
slot_no                   0
S:chip_inst              0          chip_idx               0
S:pll_initialized        1
pll_serdes_initialized   1
S:init_tries             0          init_ptEnableBM
0xba01b488
S:tick_polling           0xb980c9c0      sec_polling
0xb980c960
S:bb_fid                 129
S:ecb_key_bm[0]          0x0          ecb_key_bm[1]         0x0
S:ecb_key_bm[2]          0x0          ecb_key_bm[3]         0x0
S:is_chip_enc_enabled    0
is_chip_comp_enabled     0x0
S:ftb_rsrcp->ftb_flags  0x0          act_rsrcp->act_flag    0x1
S:lue_rsrcp->lue_flags[0] 0x0          lue_rsrcp-
>lue_flags[1]           0x0
S:c4_phyp[00]: 0xb6ab0000 0xb6ab2080 0xb6ab4100 0xb6ab6180
S:c4_phyp[04]: 0xb6ab9040 0xb6abb0c0 0xb6abd140 0xb6ac0000
S:c4_phyp[08]: 0xb6ac2080 0xb6ac4100 0xb6ac6180 0xb6ac9040
S:c4_phyp[12]: 0xb6ac60c0 0xb6acd140 0xb6ad0000 0xb6ad2080
S:c4_phyp[16]: 0xb6ad4100 0xb6ad6180 0xb6ad9040 0xb6adb0c0
S:c4_phyp[20]: 0xb6add140 0xb6ae0000 0xb6ae2080 0xb6ae4100
S:c4_phyp[24]: 0xb6ae6180 0xb6ae9040 0xb6aeb0c0 0xb6aed140
S:c4_phyp[28]: 0xb6af0000 0xb6af2080 0xb6af4100 0xb6af6180
S:c4_phyp[32]: 0xb6af9040 0xb6afb0c0 0xb6afd140 0xb6b00000
S:c4_phyp[36]: 0xb6b02080 0xb6b04100 0xb6b06180 0xb6b09040
S:c4_phyp[40]: 0xb6b0b0c0 0xb6b0d140 0xb6b10000 0xb6b12080
S:c4_phyp[44]: 0xb6b14100 0xb6b16180 0xb6b19040 0xb6b1b0c0
S:c4_phyp[48]: 0xb6b1d140 0xb6b20000 0xb6b22080 0xb6b24100
S:c4_phyp[52]: 0xb6b26180 0xb6b29040 0xb6b2b0c0 0xb6b2d140
S:c4_phyp[56]: 0xb6b30000 0xb6b32080 0xb6b34100 0xb6b36180
S:c4_phyp[60]: 0xb6b39040 0xb6b3b0c0 0xb6b3d140 0xb6b40000
S:c4_lgcp[00]: 0x97f48000 0x97f4c000 0x97f50000 0x97f54000
S:c4_lgcp[04]: 0x97f58000 0x97f5c000 0x97f60000 0x97f64000
S:c4_lgcp[08]: 0x97f68000 0x97f6c000 0x97f70000 0x97f74000
S:c4_lgcp[12]: 0x97f78000 0x97f7c000 0x97f80000 0x97f84000
S:c4_lgcp[16]: 0x97f88000 0x97f8c000 0x97f90000 0x97f94000
S:c4_lgcp[20]: 0x97f98000 0x97f9c000 0x97fa0000 0x97fa4000
S:c4_lgcp[24]: 0x97fa8000 0x97fac000 0x97fb0000 0x97fb4000
S:c4_lgcp[28]: 0x97fb8000 0x97fbc000 0x97fc0000 0x97fc4000
S:c4_lgcp[32]: 0x97fc8000 0x97fcc000 0x97fd0000 0x97fd4000
S:c4_lgcp[36]: 0x97fd8000 0x97fdc000 0x97fe0000 0x97fe4000
S:c4_lgcp[40]: 0x97fe8000 0x97fec000 0x97ff0000 0x97ff4000
S:c4_lgcp[44]: 0x97ff8000 0x97ffc000 0x8e000000 0x8e004000
S:c4_lgcp[48]: 0x8e008000 0x8e00c000 0x8e010000 0x8e014000
S:c4_lgcp[52]: 0x8e018000 0x8e01c000 0x8e020000 0x8e024000
S:c4_lgcp[56]: 0x8e028000 0x8e02c000 0x8e030000 0x8e034000
S:c4_lgcp[60]: 0x8e038000 0x8e03c000 0x8e040000 0x8e044000
S:chip_timers[00]: 0xb980c720 0xb980c780 0xb980c7e0 0xb980c840
S:chip_timers[04]: 0xb980c8a0 0xb980c900

```

```

S:disc_trap_enable_required      0x0          rxlp_disc_log_stop
    0x0
S:curr_rxlp_frm_cnt             0x0          curr_rxlp_disc_frm_cnt  0x0
S:sw_disc_frm_cnt              0x0          last_disc_frm_cnt      0x0
S:txq_nopop_pr_cnt            0x0          pollErrataDfe_ptBM
0xba01b4b0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][0]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][1] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][2]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][0] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][1]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][2] 0x0

```

S:
S:C4 Logical Port Variables

S:-----

```

S:c4_lgc_regp                   0x81c80000
S:c4_phyp:
S:    0xb6ad4100                0x0          0x0          0x0

S:    0x0                        0x0          0x0          0x0

S:master_phyp                   0xb6ad4100    if_id
0x43020010
S:min_phyp                       0x0          max_phyp          0x0
S:num_phy_ports                  1           lgc_num           16
S:num_iu_to                       0           sw_txq_bm
0
S:port_fid                       128         unused            0
S:port_group                     2           lgc_stats_clear_ts
1725611419
S:domain_tbl_sel                 0           area_tbl_sel
0
S:egid_tbl_sel                   0
S:serv_lo_bm                      0x0

```

S:
S:Proto Phy Variables:

S:-----

```

S:magic_id                       0xc4123456    asic_phyp
0xb6ad4100
S:port_id                         0x43028010    phy_cfg
0xb6ad5140
S:upsm_hdl                       0xb8014a00    physm_hdl
0xb8014780
S:ov_snsn_hdl                    0xb8014640    sw_snsn_hdl
0xb80146e0
S:ov_lksm_hdl                    0xb8014820    sw_lksm_hdl
0xb80148c0
S:trksm_hdl                      0xb8014960    lr_flag          0x0
S:lr_active                      0x0          qsfm_ttrx_rate_sel
0x0

```

S:
S:UPSM UP00: UPST_PORT_DISABLED --> UP01:

UPST_START_PORT_INIT

S:SNSM(OV) SN00: OV_SNST_STOPPED --> SN00: OV_SNST_STOPPED
 S:SNSM(SW) SW00: SW_SNST_STAGE_WS --> SW00: SW_SNST_STAGE_WS
 S:PHYSM UNKNOWN --> PP03: PHYST_NO_SIGNAL
 S:LKSM(OV) LK00: OV_LKST_INACTIVE --> LK00: OV_LKST_INACTIVE
 S:LKSM(SW) SW13: INACTIVE --> SW13: INACTIVE
 S:TRKSM TRK0: TRKST_INIT --> TRK0: TRKST_INIT

S:

S:physm variables:

S:-----

S:proto_phyph 0xb8809000 physm_hdl
 0xb8014780
 S:force_offline 0 copper 0
 S:fault_reason 0: UNKNOWN
 S:phy_media_present 1

S:

S:sns variables:

S:-----

S:speed 0xff proto_phyph
 0xb8809000
 S:hw_sn_tries_left 0x0 sw_sn_tries_left 0x0
 S:curr_txsp_count 0x0
 S:tx_max 0x0 curr_tx_indx
 0x0
 S:curr_tx 0x0 curr_rxsp_count
 0x0
 S:rx_max 0x0 curr_rx_indx
 0x0
 S:curr_rx 0x0 rx_mem
 0x0
 S:rxsp_rec_count 0x0
 S:nc_start 0x0 tx_start 0x0
 S:sync_start 0x0 sync_present 0x0
 S:diag_auto 0x0 diag_speed 0xff
 S:striped_wd_tov 3000 hw_wd_tov
 3000
 S:step 0x0 qsfp28_speed_mode
 0x0
 S:qsfp_mode0_hw_sn_tries_left 0x0
 S:qsfp_mode1_hw_sn_tries_left 0x0

S:

S:lksm variables:

S:-----

S:proto_phyph 0xb8809000 ov_lksm_hdl
 0xb8014820
 sw_lksm_hdl 0xb80148c0
 num_lf1 0
 S:hw_link_tries_left 0 sw_link_tries_left 0
 S:buf_ptype 0x0 stored_entry_state 0x6
 S:handshake_owner 0x0 mark_unsent
 0x0

```

S:busybuf_stuck          0x0          lr_wait          0x0
S:
S:trksm variables:
S:-----
-----
S:Not a trunk port
S:
S:upsm variables:
S:-----
-----
S:proto_phy             0xb8809000      upsm_hdl
0xb8014a00
S:bb_credits            0              port_beacon      0
S:port_diag_flag        0              force_offline
0
S:port_fault_rsn        0: PORT_NO_FAULT
S:retry_init_rsn        0: UNKNOWN
S:limit_reason          0              linit_result     0
S:ie_fctl_mode          0              fec_in_sync_tries_left 0
S:retry_sn_fail_init    0
retry_link_fail_init    0
S:excess_lr_count       0
S:
S:c4_ch_cfg
S:-----
-----
S:c4_desc_ring_size     256           292           256           256           292
292           2           292           292
S:thresh_def            0              16             1              0
S:intr_tries            500           cmem_pattern
0xdeadbeef
S:cmem_pattern_upwd     2              cmem_init_time   16
S:cmem_init_tries       5
S:ctrl_par_thresh       2              data_par_thresh
4
S:cam_par_thresh        4              buf_loss_thresh
12
S:crit_par_thresh       2              non_crit_par_thresh
6
S:pci_abort_thresh      10             pci_err_thresh   5
S:excess_chintr_thresh  8              sw_err_thresh    20
S:err_sample_period     300           intr_sleep
20000
S:frame_timeout         2500           proxy_dev        16384
S:vf_route              81920          qos              2048
S:stats 2048            f_redirect      2048
S:rsp_trap              2048           lun_zoning       20480
S:area_mode             0              ftb_max_loop[0]  0
S:ftb_max_loop[1]       6              ftb_max_loop[2]  9
S:ftb_max_loop[3]       10             ftb_max_loop[4]  10
S:ftb_max_loop[5]       5              ftb_max_loop[6]  6
S:ftb_seg_size[0]       0              ftb_seg_size[1]
16384
S:ftb_seg_size[2]       65536          ftb_seg_size[3]

```

```

16384
S:ftb_seg_size[4]      16384      ftb_seg_size[5]
65536
S:ftb_seg_size[6]      16384      ftb_seg_base[0]      0
S:ftb_seg_base[1]      0          ftb_seg_base[2]
65536
S:ftb_seg_base[3]      16384      ftb_seg_base[4]
32768
S:ftb_seg_base[5]      131072     ftb_seg_base[6]
49152
asic_err_monitor_period1      300
asic_err_monitor_period2      86400
zone_chk_to_poll_period 25
zone_chk_class2_reject_tov    220
S:
S:c4_phy_cfg
S:-----
-----
S:version = 2.1
S:pt      0x43028010      fab_ptr
0x9a800000
S:fabattr      0x9a8000d4      fab_iop
      0x9a800050
S:cfgbm      0xbb83d624      port_ctrl
0xb6ad5158
S:pcap.pcap_bm      0x8d215547      pcap.pcap2_bm
0x588289
S:pcap.pcap3_bm      0x1bea60c
ui_idx      47      S:slot_no
      0
is_icl      0      S:sw_usr_ports      400
S:neg_speed      0 0 0 0 0 0
S:my_domain      0x1      port_mode      0x0
S:hw_sn_maxtries      100      sw_sn_maxtries
      0
S:hw_link_maxtries      10      sw_link_maxtries      5
S:rx_cyc_tov      28      rttov      300
S:bufrdy_tov      300      busybuf_tov      286
S:mark_tov      300      lksm_tov      3000
S:buf_dealloc_wait      4      hw_wd_tov      3000
S:hw_lk_train_tov      540      hw_lk_test_tov
      150
S:syswait_tx_12_lips      1      lip_rx_tov      55
S:al_time_tov      15      lp_tov      2000
S:intr_tries_port      500      intr_mod_debounce
      250
S:intr_lsrflt_debounce      500      intr_efifo_debounce      100
S:port_no_fid      3      excess_ptintr_thresh      8
S:port_fault1_thresh      100      port_fault1_spur_thresh      250
S:port_fault1_disc_thresh      500
port_fault1_disc_spur_thresh      1000
S:port_fault2_thresh      5      losync_tov      100
S:port_sw_link_to      15      en_8g_scramble
      1

```

```

frc_hw_sn_mode          0x1
S:enc_poll_thresh      0          fec_enable
  0
S:fec_in_sync_to      50          fec_in_sync_try_max
  4
S:port_be_lto_threshold 100        port_be_lr_threshold
  2
S:be_cr_in_sync_to    5
port_credit_overrun_thresh 10
S:jda_sfp_losig_tov   400
jda_sfp_losig_try_max 30
S:striped_wd_tov      3000
no_sync_debounce      1200
S:
S:    fab_iop
S:=====
S:fab_iop->interop_mode 0x0        fab_iop->lab_mode      0x0
S:fab_iop->fl_bbc       0x0        fab_iop->fl_fan
  0x0
S:fab_iop->fl_cls       0x4        fab_iop->fl_rscn
  0x0
S:fab_iop->domain_id_offset 0x60    fab_iop-
>mcdt_fabric_mode      0x0
S:fab_iop->mcdt_default_zone 0x0        fab_iop-
>mcdt_safe_zone        0x0
S:
S:    port_ctrl
S:=====
S:port_ctrl.port_type  1          port_ctrl.port_grp    2
S:port_ctrl.port_number 47        port_ctrl.vc_mode      1
S:
S:    port_ctrl.lcap
S:=====
S:has_serdes           0          has_media              1
S:topology             1          skip_nego              0
S:skip_pnego           0          skip_init_event        0
S:en_shim              0          speed_neg
  1
S:loop_back            0          num_speeds             5
S:fec_enable           0
S:
S:    port_ctrl.speed_list array
S:=====
S:speed_list[0].auto_neg 1    speed_list[0].lnk_speed 0x0000000a
S:speed_list[1].auto_neg 1    speed_list[1].lnk_speed 0x00000008
S:speed_list[2].auto_neg 0    speed_list[2].lnk_speed 0x00000006
S:speed_list[3].auto_neg 1    speed_list[3].lnk_speed 0x00000005
S:speed_list[4].auto_neg 0    speed_list[4].lnk_speed 0x00000003
S:speed_list[5].auto_neg 0    speed_list[5].lnk_speed 0x00000000
S:
S:    port_ctrl.cm
S:=====
S:port_ctrl.cm.num_vcs    8
S:port_ctrl.cm.min_bufs  8

```



```

S:port_ctrl.cm.cr_shar_bufs      0
S:port_ctrl.vc_alloc
S:port_ctrl.vc_alloc            2 0 1 1 1 1 1 1
S:port_ctrl.vc_alloc            0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.norm_vc_alloc
S:port_ctrl.norm_vc_alloc       4 0 5 5 5 5 1 1
S:port_ctrl.norm_vc_alloc       0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.cm.skip_bb_credit    0
S:port_ctrl.cm.use_shim_based_sublist 0
S:
S:      port_ctrl.serdes_set
S:=====
S:serdes_type                    0x8
S:serdes_data_t.ibm_hss_serdes.tx_drive_power      0x1
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b_sign 0x1
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b      0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_a      0x0
S:serdes_data_t.ibm_hss_serdes.rxeq                0x0
S:
S:      cfgbm
S:=====
S:old_distance                    0x0          gport_lockdown      0x0
S:tport                            0x1          speed                0x0
S:disable_eport                    0x0          fcacc                0x0
S:lport_lockdown                    0x0          priv_lport_lockdown
0x0
S:vcxlt_linit                      0x0          delay_flogi          0x0
S:isl_interop                      0x0          distance              0x0
S:BufStarvFlag                     0x0          credit_sharing       0x0
S:lport_halfduplex                  0x0          lport_fairness       0x0
S:soft_neg                          0x0          asn_frc_hwretry      0x0
S:cr_recov                          0x0          fport_buffers        0x0
S:export                            0x0          export_mode
0x0
S:csctl_en                          0x0          mirror_port          0x0
S:fault_delay                       0x0          non_dfe               0x0
S:fec_configured*(0=ENAB)           0          fec_tts
0
S:port_persistently_disabled (permanently) 0 (0)
S:
S:      cfg property
S:=====
S:priv_pcfg_bm                      0x00000000      lgcl_pcfg_bm
0xbb83d664
S:fport_buffer                      0x00000000
S:
S:
S:C4 Discard Cntrs: rxlp_stats = 0xb6ad44b0
S:-----
-----
S:disc_mcast_wka                    0x0          disc_inv_did         0x0
S:disc_cl1_cl4                      0x0          disc_sid_chk_fail    0x0

```

```

S:disc_inv_dom_egid_txpt      0x0          disc_vft_hop_cnt_1
    0x0
S:disc_classf                0x0          disc_fcp_cdb_inv      0x0
S:disc_vfid_trap_enabled     0x0
disc_vfid_hdr_chk_fail      0x0
S:disc_shim_cksum_fail       0x0          disc_fed_edit_cmd_err 0x0
S:disc_shim_cksum_fail       0x0          disc_fed_edit_cmd_err 0x0
S:disc_ftb_vm_mode           0x0          disc_ftb_agn_t2_miss  0x0
S:disc_ecb_de_pad_err        0x0          disc_ecb_de_tag_err   0x0
S:disc_ecb_de_seq_err        0x0          disc_ecb_err          0x0
S:disc_ftb_type4_match       0x0          disc_fcp_rsp_ftb_type4 0x0
S:disc_fcp_rsp_ftb_type4     0x0          disc_ftb_type5_match
    0x0
S:disc_ftb_type3_match       0x0          disc_els_ftb_type3    0x0
S:disc_ftb_type1_match       0x0          disc_els_rsp_ex_port  0x0
S:disc_inv_drp_dps           0x0          disc_did_lookup_miss  0x0
S:disc_ftb_type2_match       0x0          disc_trpd_plogi_pdisc 0x0
S:disc_type2_lookup_miss     0x0          disc_ftb_type6_match
    0x0
S:disc_els_rep_ex_port       0x0          disc_els_sid_lkup_bit1 0x0
S:disc_els_sid_lkup_bit0     0x0
disc_bls_frm_trap_bit1      0x0
S:disc_ftb_token_err         0x0          disc_asic_internal_err 0x0
S:disc_hard_zone_miss        0x0          disc_lun_zone_miss    0x0
S:discflt_frame_disc         0x0          discflt_parity_err    0x0
S:disc_frame_marked_du       0x0          disc_frame_marked_to  0x0
E:Connection type: FE
E:Port type: F_port
E:Trunk port: No
E:Configured Speed: AUTO_SPEED_NEGO
E:Max Capable Speed: 32G
E:Current SNSM Speed: UNDEFINED
E:Hardware TX Speed: 32G (0x00000004)
E:Hardware RX Speed: 32G (0x00000040)
E:
E:Interrupts:    0          Link_failure:        0
Loss_of_sync:    0          Loss_of_sig:         0
E:Lli:           0          Invalid_word:        0
E:trapped_frm:   0          fwd_status_ok:       0
E:fwd_timeout:   0          fwd_tx_unavail:     0
E:fwd_unroutable: 0          fwd_zone_out:        0
E:fwd_other_err: 0          frm_err_discard:     0
E:Fltr listA:    0          Fltr listB:         0
E:Zone trap fwd: 0          Zone trap disc:     0
E:shim_csum:     0          RTE_perr:           0
E:Invalid_crc:   0          Delim_err:          0
E:Protocol_err:  0
E:Lr_in:         0          Lr_out:             0
E:Ols_in:        0          Ols_out:            0

```

filterportshow 47

FILTER DATA

Shadow settings:
Filter Enable: 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass: 0x00000000

Real settings:
Enable RAM: 0x00000000, 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000

Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass RAM: 0x00000000

Shadowed filters:

Filter 0: Not Installed (MIRROR1)(LISTA)
c4_fldenable[0] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[0] = 0x00000000,c4_fltr_config[0] = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
c4_fldenable[1] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[1] = 0x00000000,c4_fltr_config[1] = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
c4_fldenable[2] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[2] = 0x00000000,c4_fltr_config[2] = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
c4_fldenable[3] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[3] = 0x00000000,c4_fltr_config[3] = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
c4_fldenable[4] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[4] = 0x00000000,c4_fltr_config[4] = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
c4_fldenable[5] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[5] = 0x00000000,c4_fltr_config[5] = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
c4_fldenable[6] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[6] = 0x00000000,c4_fltr_config[6] = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
c4_fldenable[7] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[7] = 0x00000000,c4_fltr_config[7] = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
c4_fldenable[8] = 0x00000000 0x00000000 0x00000000

```
0x00000000
    c4_fldnegate[8] = 0x00000000,c4_fltr_config[8] = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
    c4_fldenable[9] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[9] = 0x00000000,c4_fltr_config[9] = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
    c4_fldenable[10] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[10] = 0x00000000,c4_fltr_config[10] =
0x00000000
Filter 11: Not Installed (SIM)(LISTA)
    c4_fldenable[11] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[11] = 0x00000000,c4_fltr_config[11] =
0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
    c4_fldenable[12] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[12] = 0x00000000,c4_fltr_config[12] =
0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
    c4_fldenable[13] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[13] = 0x00000000,c4_fltr_config[13] =
0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
    c4_fldenable[14] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[14] = 0x00000000,c4_fltr_config[14] =
0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
    c4_fldenable[15] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[15] = 0x00000000,c4_fltr_config[15] =
0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
    c4_fldenable[16] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[16] = 0x00000000,c4_fltr_config[16] =
0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
    c4_fldenable[17] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[17] = 0x00000000,c4_fltr_config[17] =
0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
    c4_fldenable[18] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[18] = 0x00000000,c4_fltr_config[18] =
0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
    c4_fldenable[19] = 0x00000000 0x00000000 0x00000000
0x00000000
```

```
    c4_fldnegate[19] = 0x00000000,c4_fltr_config[19] =
0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
    c4_fldenable[20] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[20] = 0x00000000,c4_fltr_config[20] =
0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
    c4_fldenable[21] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[21] = 0x00000000,c4_fltr_config[21] =
0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
    c4_fldenable[22] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[22] = 0x00000000,c4_fltr_config[22] =
0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
    c4_fldenable[23] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[23] = 0x00000000,c4_fltr_config[23] =
0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
    c4_fldenable[24] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[24] = 0x00000000,c4_fltr_config[24] =
0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
    c4_fldenable[25] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[25] = 0x00000000,c4_fltr_config[25] =
0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
    c4_fldenable[26] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[26] = 0x00000000,c4_fltr_config[26] =
0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
    c4_fldenable[27] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[27] = 0x00000000,c4_fltr_config[27] =
0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
    c4_fldenable[28] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[28] = 0x00000000,c4_fltr_config[28] =
0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
    c4_fldenable[29] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[29] = 0x00000000,c4_fltr_config[29] =
0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    c4_fldenable[30] = 0x00000000 0x00000000 0x00000000
```

```
0x00000000
    c4_fldnegate[30] = 0x00000000,c4_fltr_config[30] =
0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    c4_fldenable[31] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[31] = 0x00000000,c4_fltr_config[31] =
0x00000000
```

Real filters:

```
Filter 0: Not Installed (MIRROR1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
```

0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 11: Not Installed (SIM)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 24: Not Installed (PERF9)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter dirty indicator: 0x00000000
Performance filters: 0
Port Mirror filters: 0 (0x0)

FIELD DATA

Shadowed fields:

fldoffset[0] = 0x00, fldmask[0] = 0x00, fldvalue_dyna[0]: 0x00 0x00
0x00 0x00
fldcontrol[0].inuse = 0x0 fldcontrol[0].refcnt = 0x00 0x00 0x00
0x00
fldoffset[1] = 0x00, fldmask[1] = 0x00, fldvalue_dyna[1]: 0x00 0x00
0x00 0x00
fldcontrol[1].inuse = 0x0 fldcontrol[1].refcnt = 0x00 0x00 0x00
0x00
fldoffset[2] = 0x00, fldmask[2] = 0x00, fldvalue_dyna[2]: 0x00 0x00
0x00 0x00
fldcontrol[2].inuse = 0x0 fldcontrol[2].refcnt = 0x00 0x00 0x00

```
0x00
fldoffset[3] = 0x00, fldmask[3] = 0x00, fldvalue_dyna[3]:0x00 0x00
0x00 0x00
fldcontrol[3].inuse = 0x0  fldcontrol[3].refcnt = 0x00 0x00 0x00
0x00
fldoffset[4] = 0x00, fldmask[4] = 0x00, fldvalue_dyna[4]:0x00 0x00
0x00 0x00
fldcontrol[4].inuse = 0x0  fldcontrol[4].refcnt = 0x00 0x00 0x00
0x00
fldoffset[5] = 0x00, fldmask[5] = 0x00, fldvalue_dyna[5]:0x00 0x00
0x00 0x00
fldcontrol[5].inuse = 0x0  fldcontrol[5].refcnt = 0x00 0x00 0x00
0x00
fldoffset[6] = 0x00, fldmask[6] = 0x00, fldvalue_dyna[6]:0x00 0x00
0x00 0x00
fldcontrol[6].inuse = 0x0  fldcontrol[6].refcnt = 0x00 0x00 0x00
0x00
fldoffset[7] = 0x00, fldmask[7] = 0x00, fldvalue_dyna[7]:0x00 0x00
0x00 0x00
fldcontrol[7].inuse = 0x0  fldcontrol[7].refcnt = 0x00 0x00 0x00
0x00
fldoffset[8] = 0x00, fldmask[8] = 0x00, fldvalue_dyna[8]:0x00 0x00
0x00 0x00
fldcontrol[8].inuse = 0x0  fldcontrol[8].refcnt = 0x00 0x00 0x00
0x00
fldoffset[9] = 0x00, fldmask[9] = 0x00, fldvalue_dyna[9]:0x00 0x00
0x00 0x00
fldcontrol[9].inuse = 0x0  fldcontrol[9].refcnt = 0x00 0x00 0x00
0x00
fldoffset[10] = 0x00, fldmask[10] = 0x00, fldvalue_dyna[10]:0x00 0x00
0x00 0x00
fldcontrol[10].inuse = 0x0  fldcontrol[10].refcnt = 0x00 0x00 0x00
0x00
fldoffset[11] = 0x00, fldmask[11] = 0x00, fldvalue_dyna[11]:0x00 0x00
0x00 0x00
fldcontrol[11].inuse = 0x0  fldcontrol[11].refcnt = 0x00 0x00 0x00
0x00
fldoffset[12] = 0x00, fldmask[12] = 0x00, fldvalue_dyna[12]:0x00 0x00
0x00 0x00
fldcontrol[12].inuse = 0x0  fldcontrol[12].refcnt = 0x00 0x00 0x00
0x00
fldoffset[13] = 0x00, fldmask[13] = 0x00, fldvalue_dyna[13]:0x00 0x00
0x00 0x00
fldcontrol[13].inuse = 0x0  fldcontrol[13].refcnt = 0x00 0x00 0x00
0x00
fldoffset[14] = 0x00, fldmask[14] = 0x00, fldvalue_dyna[14]:0x00 0x00
0x00 0x00
fldcontrol[14].inuse = 0x0  fldcontrol[14].refcnt = 0x00 0x00 0x00
0x00
fldoffset[15] = 0x00, fldmask[15] = 0x00, fldvalue_dyna[15]:0x00 0x00
0x00 0x00
fldcontrol[15].inuse = 0x0  fldcontrol[15].refcnt = 0x00 0x00 0x00
0x00
fldoffset[16] = 0x00, fldmask[16] = 0x00, fldvalue_dyna[16]:0x00 0x00
```

0x00 0x00
fldcontrol[16].inuse = 0x0 fldcontrol[16].refcnt = 0x00 0x00 0x00
0x00
fldoffset[17] = 0x00, fldmask[17] = 0x00, fldvalue_dyna[17]:0x00 0x00
0x00 0x00
fldcontrol[17].inuse = 0x0 fldcontrol[17].refcnt = 0x00 0x00 0x00
0x00
fldoffset[18] = 0x00, fldmask[18] = 0x00, fldvalue_dyna[18]:0x00 0x00
0x00 0x00
fldcontrol[18].inuse = 0x0 fldcontrol[18].refcnt = 0x00 0x00 0x00
0x00
fldoffset[19] = 0x00, fldmask[19] = 0x00, fldvalue_dyna[19]:0x00 0x00
0x00 0x00
fldcontrol[19].inuse = 0x0 fldcontrol[19].refcnt = 0x00 0x00 0x00
0x00

Real fields:

fldoffset RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000
fldmask RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000
fld value4 RAM:
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
Field dirty indicator: 0x00000000

FDB reference count fdb: 0 [0 0 0 0]
FDB reference count fdb: 1 [0 0 0 0]
FDB reference count fdb: 2 [0 0 0 0]
FDB reference count fdb: 3 [0 0 0 0]
FDB reference count fdb: 4 [0 0 0 0]
FDB reference count fdb: 5 [0 0 0 0]
FDB reference count fdb: 6 [0 0 0 0]
FDB reference count fdb: 7 [0 0 0 0]
FDB reference count fdb: 8 [0 0 0 0]

FDB reference count fdb: 9 [0 0 0 0]
FDB reference count fdb: 10 [0 0 0 0]
FDB reference count fdb: 11 [0 0 0 0]
FDB reference count fdb: 12 [0 0 0 0]
FDB reference count fdb: 13 [0 0 0 0]
FDB reference count fdb: 14 [0 0 0 0]
FDB reference count fdb: 15 [0 0 0 0]
FDB reference count fdb: 16 [0 0 0 0]
FDB reference count fdb: 17 [0 0 0 0]
FDB reference count fdb: 18 [0 0 0 0]
FDB reference count fdb: 19 [0 0 0 0]

Filter counters:

Filter counter 0: 0 (MIRROR1)
Filter counter 1: 0 (MIRROR2)
Filter counter 2: 0 (MIRROR3)
Filter counter 3: 0 (MIRROR4)
Filter counter 4: 0 (AEPORT_NON_MIRR_DROP)
Filter counter 5: 0 (ZONING TRAP)
Filter counter 6: 0 (FCR_EXPORT_DC)
Filter counter 7: 0 (TIN TRAP)
Filter counter 8: 0 (FICON CUP)
Filter counter 9: 0 (FICON CUP DST)
Filter counter 10: 0 (WELL KNOWN ADDR)
Filter counter 11: 0 (SIM)
Filter counter 12: 0 (UNUSED)
Filter counter 13: 0 (UNUSED)
Filter counter 14: 0 (UNUSED)
Filter counter 15: 0 (UNUSED)
Filter counter 16: 0 (PERF1)
Filter counter 17: 0 (PERF2)
Filter counter 18: 0 (PERF3)
Filter counter 19: 0 (PERF4)
Filter counter 20: 0 (PERF5)
Filter counter 21: 0 (PERF6)
Filter counter 22: 0 (PERF7)
Filter counter 23: 0 (PERF8)
Filter counter 24: 0 (PERF9)
Filter counter 25: 0 (PERF10)
Filter counter 26: 0 (PERF11)
Filter counter 27: 0 (PERF12)
Filter counter 28: 0 (OPM1)
Filter counter 29: 0 (OPM2)
Filter counter 30: 0 (IPM1)
Filter counter 31: 0 (IPM2)

ACL DATA

Logical port 16: Hard Zoning disabled, Soft Zoning disabled
Zone type: WWN Zoning
Frames with hard zone miss: 0

*** Please use filterportshow on user port 56 to display ACL hash tables and Mirroring resources of thischip.

***We show this data only for the first physical port which is an external port.

portFcPortCmdShow --slot 0 48 3
doing portFcPortCmdShow: arg1 = 3, arg2 = -2

portshow 48
portDisableReason: None
portCFlags: 0x0
portFlags: 0x4021 PRESENT U_PORT DISABLED LED
LocalSwcFlags: 0x0
portType: 26.0
POD Port: Need license to enable the port
portState: 2 Offline
Protocol: FC
portPhys: 2 No_Module portScn: 2 Offline
port generation number: 0
state transition count: 0

portId: 013000
portIfId: 43020008
portWwn: 20:30:d8:1f:cc:2c:99:90
portWwn of device(s) connected:
16b Area list:
Distance: normal
portSpeed: N32Gbps

FEC: Inactive
Credit Recovery: Inactive
LE domain: 0
Peer beacon: Off
FC Fastwrite: OFF

| | | | | |
|-------------|---|---------------|---|-------|
| Interrupts: | 0 | Link_failure: | 0 | Frjt: |
| 0 | | | | |
| Unknown: | 0 | Loss_of_sync: | 0 | Fbsy: |
| 0 | | | | |
| Lli: | 0 | Loss_of_sig: | 0 | |
| Proc_rqrd: | 0 | Protocol_err: | 0 | |
| Timed_out: | 0 | Invalid_word: | 0 | |
| Tx_unavail: | 0 | Invalid_crc: | 0 | |
| Delim_err: | 0 | Address_err: | 0 | |
| Lr_in: | 0 | Ols_in: | 0 | |
| Lr_out: | 0 | Ols_out: | 0 | |

portloginshow 48
Type PID World Wide Name credit df_sz cos
=====

portloginshow 48 -history
Type PID World Wide Name logout time
=====

portregshow 48

LED registers

=====

| | | |
|---------------------------|----------|-------------|
| 0x81c42000: c4_led_status | 00000000 | 0x81c42004: |
| c4_led_ctl | 00000000 | |

FPL registers

=====

| | | |
|---------------------------------|----------|-------------|
| 0x81c40200: fpl_port_config | 23490000 | |
| 0x81c4020c: fpl_port_id_ctl | 00000000 | 0x81c40210: |
| fpl_port_id_addr | 00013000 | |
| 0x81c40214: fpl_port_speed | 00000004 | 0x81c4021c: |
| fpl_lli_ctl | 00000903 | |
| 0x81c40228: fpl_lli_os_ctl | bc95b5b5 | 0x81c4022c: |
| fpl_lli_send_word | bc95b5b5 | |
| 0x81c40230: fpl_lli_mark_rx | 00000000 | 0x81c40234: |
| fpl_lli_rnd_trip_time | 00000000 | |
| 0x81c40238: fpl_lli_ns_status | 80070007 | 0x81c4023c: |
| fpl_lli_intr_status | 80070007 | |
| 0x81c40244: fpl_lli_def | 00000000 | 0x81c40254: |
| fpl_lli_intr_enable_clr | 00100000 | |
| 0x81c40258: fpl_err_intr_status | 00000000 | 0x81c40260: |
| fpl_err_intr_enable_clr | 00000000 | |
| 0x81c40268: fpl_err_first_error | 00000000 | 0x81c4026c: |
| fpl_speed_neg_ctl | 00000000 | |
| 0x81c40270: fpl_speed_neg_stat | 00000000 | 0x81c40274: |
| fpl_softasn_ctl | 0000000f | |
| 0x81c40278: fpl_link_init_ctl | 00000000 | 0x81c4027c: |
| fpl_link_init_stat | 00000000 | |
| 0x81c40280: fpl_aec_ctl | 00051060 | 0x81c40284: |
| fpl_aec_ctl2 | 04009f60 | |
| 0x81c40288: fpl_pcs_ctl | 00000160 | 0x81c4028c: |
| fpl_fec_ctl | 00000441 | |
| 0x81c40290: fpl_fec_cor | 00000000 | 0x81c40294: |
| fpl_fec_uncor | 00000000 | |
| 0x81c40298: fpl_hss_link_ctl | 0031f040 | 0x81c4029c: |
| fpl_afifo_link_ctl | 00000a86 | |
| 0x81c402a0: fpl_echo_lb_ctl | 0000028c | 0x81c402a4: |
| fpl_scratch | 00000121 | |
| 0x81c402a8: fpl_debug | 00030005 | 0x81c402ac: |
| fpl_misc_debug | 00001800 | |
| 0x00000000: SW_shadow_reg | 00000000 | 0x00000000: |
| SW_c4_phyp->cfgptr | 00030000 | |

per-fpg (per octet) registers

=====

| | | |
|----------------------------------|----------|-------------|
| 0x8180b82c: fpg_serdes_ctla0 | 81a37be7 | 0x8180b830: |
| fpg_serdes_ctla1 | 81a37be7 | |
| 0x8180b834: fpg_serdes_ctlb0 | 81a1c3c3 | 0x8180b838: |
| fpg_serdes_ctlb1 | 81a1c3c3 | |
| 0x8180b83c: fpg_serdes_xgmii_1ms | 00067c28 | 0x8180b840: |
| fpg_serdes_regtimctl | 40e47946 | |

0x8180b844: fpg_serdes_asnrsttimctl 00000102

HSS PLL registers

=====

| | | |
|---------------------------------------|----------|-------------|
| 0x81809400: 00_hsspll_vco_coarse_cal0 | 00000000 | 0x81809404: |
| 01_hsspll_vco_coarse_cal1 | 00000014 | |
| 0x81809408: 02_hsspll_vco_coarse_cal2 | 00000000 | 0x8180940c: |
| 03_hsspll_vco_coarse_cal3 | 00000000 | |
| 0x81809410: 04_hsspll_vco_coarse_cal4 | 00000000 | 0x81809424: |
| 09_hsspll_power_ctl | 00000000 | |
| 0x81809428: 0A_hsspll_charge_pump_ctl | 00000004 | 0x81809438: |
| 0E_hsspll_pll_misc_ctl | 00000000 | |
| 0x8180943c: 0F_hsspll_pclk_ctl | 000000f8 | 0x81809440: |
| 10_hsspll_eyem_intv_ctl | 00000000 | |
| 0x81809444: 11_hsspll_eyem_intv_lim1 | 00000000 | 0x81809448: |
| 12_hsspll_eyem_intv_lim2 | 00000000 | |
| 0x8180944c: 13_hsspll_eyem_intv_lim3 | 00000000 | 0x81809450: |
| 14_hsspll_eyem_intv_lim4 | 00000000 | |
| 0x818094f0: 3C_hsspll_macro_tst_ctl4 | 00000000 | 0x818094f4: |
| 3D_hsspll_macro_tst_ctl3 | 00000000 | |
| 0x818094f8: 3E_hsspll_macro_tst_ctl2 | 00000000 | 0x818094fc: |
| 3F_hsspll_macro_tst_ctl1 | 00000000 | |
| 0x81809500: 00_hsspll_vco_coarse_cal0 | 0000000a | 0x81809504: |
| 01_hsspll_vco_coarse_cal1 | 00000014 | |
| 0x81809508: 02_hsspll_vco_coarse_cal2 | 00000000 | 0x8180950c: |
| 03_hsspll_vco_coarse_cal3 | 00000000 | |
| 0x81809510: 04_hsspll_vco_coarse_cal4 | 00000000 | 0x81809524: |
| 09_hsspll_power_ctl | 00000000 | |
| 0x81809528: 0A_hsspll_charge_pump_ctl | 00000004 | 0x81809538: |
| 0E_hsspll_pll_misc_ctl | 00000000 | |
| 0x8180953c: 0F_hsspll_pclk_ctl | 000000f8 | 0x81809540: |
| 10_hsspll_eyem_intv_ctl | 00000000 | |
| 0x81809544: 11_hsspll_eyem_intv_lim1 | 00000000 | 0x81809548: |
| 12_hsspll_eyem_intv_lim2 | 00000000 | |
| 0x8180954c: 13_hsspll_eyem_intv_lim3 | 00000000 | 0x81809550: |
| 14_hsspll_eyem_intv_lim4 | 00000000 | |
| 0x818095f0: 3C_hsspll_macro_tst_ctl4 | 00000000 | 0x818095f4: |
| 3D_hsspll_macro_tst_ctl3 | 00000000 | |
| 0x818095f8: 3E_hsspll_macro_tst_ctl2 | 00000000 | 0x818095fc: |
| 3F_hsspll_macro_tst_ctl1 | 00000000 | |

HSS TX registers

=====

| | | |
|--------------------------------------|----------|-------------|
| 0x81808000: 00_hsstx_cfg_mode_PHY | 00009f48 | 0x81808004: |
| 01_hsstx_test_ctl | 00000000 | |
| 0x81808008: 02_hsstx_coeff_ctl_INV | 00000000 | 0x8180800c: |
| 03_hsstx_drv_mode_ctl | 00000000 | |
| 0x81808010: 04_hsstx_drv_ovrd_ctl | 00000010 | 0x81808014: |
| 05_hsstx_dclk_align_ovrd | 00000080 | |
| 0x81808018: 06_hsstx_imp_cal_ovrd | 00000c0c | 0x8180801c: |
| 07_hsstx_dclk_drift_tol | 00000004 | |
| 0x81808020: 08_hsstx_tap0_coeff_TUNE | 00000000 | 0x81808024: |
| 09_hsstx_tap1_coeff_TUNE | 00000003 | |
| 0x81808028: 0A_hsstx_tap2_coeff_TUNE | 00000018 | 0x8180802c: |

| | | | |
|---|----------|----------|-------------|
| 0B_hsstx_tap3_coeff_TUNE | 0000000d | | |
| 0x81808034: 0D_hsstx_pol_INV | | 0000000a | 0x81808038: |
| 0E_hsstx_ae_cmd | 00000000 | | |
| 0x8180803c: 0F_hsstx_ae_stat | | 00000000 | 0x81808040: |
| 10_hsstx_ae_tap0_TUNE | 00000000 | | |
| 0x81808044: 11_hsstx_ae_tap1_TUNE | | 00000000 | 0x81808048: |
| 12_hsstx_ae_tap2_TUNE | 00000028 | | |
| 0x8180804c: 13_hsstx_ae_tap3_TUNE | | 00000000 | 0x81808054: |
| 15_hsstx_app_tune | 0000120e | | |
| 0x81808058: 16_hsstx_analog_diag | | 00000000 | 0x81808060: |
| 18_hsstx_4x_seg_app | 0000aafa | | |
| 0x81808064: 19_hsstx_2x_seg_app | | 00000000 | 0x81808068: |
| 1A_hsstx_1x_seg_app | 0000ff5d | | |
| 0x8180806c: 1B_hsstx_seg_4x_term_app | | 00000000 | 0x81808070: |
| 1C_hsstx_seg_2x1x_term_app | 00000f00 | | |
| 0x81808074: 1D_hsstx_tap_sign_app | | 0000000a | 0x81808078: |
| 1E_hsstx_ext_addr_data | 00000001 | | |
| 0x8180807c: 1F_hsstx_ext_addr_addr | | 00000000 | 0x81808080: |
| 20_hsstx_pat_buf_bytes_1_0 | 00000000 | | |
| 0x81808084: 21_hsstx_pat_buf_bytes_3_2 | | 00000000 | 0x81808088: |
| 22_hsstx_pat_buf_bytes_5_4 | 00000000 | | |
| 0x8180808c: 23_hsstx_pat_buf_bytes_7_6 | | 00000000 | 0x8180809c: |
| 27_hsstx_8023az_ctl | 00000000 | | |
| 0x818080a0: 28_hsstx_dcc_ctl | | 000060c0 | 0x818080a4: |
| 29_hsstx_dcc_ovrd | 00001000 | | |
| 0x818080a8: 2A_hsstx_dcc_app | | 00000085 | 0x818080ac: |
| 2B_hsstx_dcc_timeout | 0000ffff | | |
| 0x818080c0: 30_hsstx_tap_sign_ovrd | | 00000000 | 0x818080c8: |
| 32_hsstx_seg_4x_ovrd | 00000000 | | |
| 0x818080cc: 33_hsstx_seg_2x_ovrd | | 00000000 | 0x818080d0: |
| 34_hsstx_seg_1x_ovrd | 00000000 | | |
| 0x818080d8: 36_hsstx_tap_seg_4x_term_ovrd | | 00000000 | 0x818080dc: |
| 37_hsstx_tap_seg_2x_term_ovrd | 00000000 | | |
| 0x818080e0: 38_hsstx_tap_seg_1x_term_ovrd | | 00000000 | 0x818080ec: |
| 3B_hsstx_mac_test_ctl5 | 00000000 | | |
| 0x818080f0: 3C_hsstx_mac_test_ctl4 | | 00000000 | 0x818080f4: |
| 3D_hsstx_mac_test_ctl3 | 00000000 | | |
| 0x818080f8: 3E_hsstx_mac_test_ctl2 | | 00000000 | 0x818080fc: |
| 3F_hsstx_mac_test_ctl1 | 000000c6 | | |

HSS RX registers

=====

| | | | |
|---------------------------------------|----------|----------|-------------|
| 0x81808200: 00_hssrx_cfg_mode_PHY | | 00009e78 | 0x81808204: |
| 01_hssrx_test_ctl | 00000000 | | |
| 0x81808208: 02_hssrx_phs_rot_ctl | | 0000cb80 | 0x8180820c: |
| 03_hssrx_phs_rot_ofs_ctl | 00004610 | | |
| 0x81808210: 04_hssrx_phs_rot_posn1 | | 00003132 | 0x81808214: |
| 05_hssrx_phs_rot_posn2 | 0000001d | | |
| 0x81808218: 06_hssrx_phs_rot_sta_ofs1 | | 00000100 | 0x8180821c: |
| 07_hssrx_phs_rot_sta_ofs2 | 00000001 | | |
| 0x81808220: 08_hssrx_dfe_ctl_PHY | | 00002002 | 0x81808224: |
| 09_hssrx_dfe_smpl_snap1 | 00000000 | | |
| 0x81808228: 0A_hssrx_dfe_smpl_snap2 | | 00008000 | 0x8180822c: |
| 0B_hssrx_vga_ctl1 | 000041fe | | |

| | | |
|--|-----------|-------------|
| 0x81808230: 0C_hssrx_vga_ctl2 | 00007aa0 | 0x81808234: |
| 0D_hssrx_vga_ctl3 | 000009e4 | |
| 0x81808238: 0E_hssrx_pwr_mgmt_ctl | 0000001f | 0x8180823c: |
| 0F_hssrx_iqamp_ctl1 | 00000018 | |
| 0x81808240: 10_hssrx_iqamp_ctl2 | 00000003 | 0x81808244: |
| 11_hssrx_dacap_dacan_sel | 00000003 | |
| 0x81808248: 12_hssrx_dacap_dacan | 0000ffff | 0x8180824c: |
| 13_hssrx_daca_min | 00000000 | |
| 0x81808250: 14_hssrx_adac_ctl | 00000000 | 0x81808254: |
| 15_hssrx_ac_cp_ctl | 000031c3 | |
| 0x81808258: 16_hssrx_ac_cp_val | 0000804c | 0x8180825c: |
| 17_hssrx_dfe_h1h2h3_lcl_off_ch | 00000014 | |
| 0x81808260: 18_hssrx_dfe_h1h2h3_lcl_off_val | 00000000 | 0x81808264: |
| 19_hssrx_peaked_intg | 000000ff | |
| 0x81808268: 1A_hssrx_cdr_analog_sw | 0000ce00 | 0x8180826c: |
| 1B_hssrx_peaking_amp_init_c_PHY | 00000000 | |
| 0x81808270: 1C_hssrx_dac_dpc | 00000040 | 0x81808274: |
| 1D_hssrx_ddc | 00000000 | |
| 0x81808278: 1E_hssrx_int_stat_PHY | 00000c0f | 0x8180827c: |
| 1F_hssrx_dfe_func_ctl1_PHY | 0000ffff | |
| 0x81808280: 20_hssrx_dfe_func_ctl2_INV | 00007ebf | 0x81808284: |
| 21_hssrx_ofs_ch_dcc_qcc_idx | 00002000 | |
| 0x81808288: 22_hssrx_dfe_ofs_val | 00007b00 | 0x8180828c: |
| 23_hssrx_h_coeff_bist | 00000401 | |
| 0x81808290: 24_hssrx_ac_cap_bist | 00000080 | 0x81808294: |
| 25_hssrx_max_gain_path_idx_res | 00007800 | |
| 0x81808298: 26_hssrx_loff_ctl | 00000040 | 0x8180829c: |
| 27_hssrx_sigdet_ctl | 00003180 | |
| 0x818082a0: 28_hssrx_ana_ctl_sw | 00000000 | 0x818082a4: |
| 29_hssrx_intg_dac_ofs | 0000e1e1 | |
| 0x818082a8: 2A_hssrx_eye_ctl | 00000000 | 0x818082ac: |
| 2B_hssrx_eye_met | 00000004 | |
| 0x818082b0: 2C_hssrx_eye_met_err_cnt | 00000000 | 0x818082b4: |
| 2D_hssrx_eye_met_pdf_eyec | 00000000 | |
| 0x818082b8: 2E_hssrx_eye_met_pat_len | 0000007f | 0x818082bc: |
| 2F_hssrx_dfe_func_ctl3 | 0000dfff | |
| 0x818082c0: 30_hssrx_dfe_tap_ctl_idx_ptr | 00000008 | 0x818082c4: |
| 31_hssrx_dfe_tap | 00003030 | |
| 0x818082c8: 32_hssrx_lte_ctl_TUNE | 00001601 | 0x818082e4: |
| 39_hssrx_int_stat2 | 0000c1ff | |
| 0x818082e8: 3A_hssrx_ac_cpl_cur_src_adj | 00000040 | 0x818082ec: |
| 3B_hssrx_dcd_ctl | 00007c00 | |
| 0x818082f0: 3C_hssrx_dcc_ctl | 00000d45 | 0x818082f4: |
| 3D_hssrx_qcc_ctl | 0000698c | |
| 0x818082f8: 3E_hssrx_mac_test_ctl2 | 00000000 | 0x818082fc: |
| 3F_hssrx_mac_test_ctl1 | 00000000 | |
| 0x81808248: 12_hssrx_dacap_dacan[02] | 00ff ffff | |
| 0x81808260: 18_hssrx_dfe_h1h2h3_lcl_off_va[00] | 0000 0000 | 0000 |
| 0000 0000 0000 0000 0000 | | |
| 0x81808260: 18_hssrx_dfe_h1h2h3_lcl_off_va[08] | 0000 0000 | 0000 |
| 0000 0000 0000 0000 0000 | | |
| 0x81808260: 18_hssrx_dfe_h1h2h3_lcl_off_va[16] | 0000 0000 | 0000 |
| 0000 0000 | | |
| 0x81808288: 22_hssrx_dfe_ofs_val[00][00] | 7b00 0000 | 097b |

```

7f00 037b 0000
0x81808288: 22_hssrx_dfe_ofs_val[03][00] 007b 0000 017b
0000 057f 7f00
0x81808288: 22_hssrx_dfe_ofs_val[06][00] 7f7f 0000 7d05
007f 0b7c 7f00
0x81808288: 22_hssrx_dfe_ofs_val[09][00] 7f7e 0000 010b
7f7f 087d 7f00
0x81808288: 22_hssrx_dfe_ofs_val[12][00] 7c09 007f 7e0c
007f 7d7f 0000
0x81808288: 22_hssrx_dfe_ofs_val[15][00] 0409 7f7f 7f7b
0000 797b 0000
0x81808288: 22_hssrx_dfe_ofs_val[18][00] 7f09 007f 7d7b
0000 0003 007f
0x81808288: 22_hssrx_dfe_ofs_val[21][00] 0003 007f 0003
007f 0003 007f
0x81808288: 22_hssrx_dfe_ofs_val[24][00] 0102 7f00 7e7f
0000 797d 0000
0x81808294: 25_hssrx_max_gain_path_idx_res[00] 005c 0849 1012
18a1 20df 289f 3084 3800
0x81808294: 25_hssrx_max_gain_path_idx_res[08] 409f 487f 5074
5801 6040 6800 70fe 7800
0x818082c4: 31_hssrx_dfe_tap[00] fffe 8181 0000
0000 0030 0030 3030 3030
0x818082c4: 31_hssrx_dfe_tap[08] 3030 3030 3030
0000
0x818082e8: 3A_hssrx_ac_cpl_cur_src_adj[00] 0040 0040 0040
0040
0x818082ec: 3B_hssrx_dcd_ctl[00] 7c00 5c00 7c83
5c00 7c00
0x818082f0: 3C_hssrx_dcc_ctl[00] 0d45 0d81 0d81
0d41
0x818082f4: 3D_hssrx_qcc_ctl[00] 6988 698c

```

xfipcs, fec, aec, & aet registers

```

=====
0x81c40400: xfipcs_reg [00] 00002040 00000080 00000000
00000000 00000001 00000008 00000000 00000000
0x81c40420: xfipcs_reg [08] 00008c01 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c40440: xfipcs_reg [16] 00000000 00000000 00000000
00000000 00000040 00000000 00000000 00000000
0x81c40460: xfipcs_reg [24] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c40480: xfipcs_reg [32] 00000004 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c40620: fec_32g_128g_reg [08] 00000000 00000000 00000000
00000000 00000000 00000000 00000000
0x81c40648: fec_32g_128g_reg [18] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c40a00: aec_reg [00] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c40c00: aet_reg [00] 00000000 00000000 00000000
00000000 00000000

```

bbc registers

=====

| | | | | | | | |
|--------------------------------|----------|----------------------|---|---|---|---|---|
| 0x81c41800: bbc_trc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c41840: bbc_trc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c41880: bbc_trc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c418c0: bbc_trc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c41900: bbc_trc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c41804: bbc_mbc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c41844: bbc_mbc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c41884: bbc_mbc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c418c4: bbc_mbc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c41904: bbc_mbc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c41a00: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c41a20: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c41a40: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c41a60: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c41a80: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c41c00: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c41c20: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c41c40: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c41c60: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c41c80: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c41d00: bbc_fbpc | 00000000 | | | | | | |
| 00000000 | | | | | | | |
| 0x81c41d08: bbc_rcc_inc | 00000000 | | | | | | |
| bbc_rqc_inc | 00000000 | | | | | | |
| 0x81c41d10: bbc_fbpc_inc | 00000000 | | | | | | |
| bbc_tmc_inc | 00000000 | | | | | | |
| 0x81c41d18: bbc_threshold | 00080100 | | | | | | |
| bbc_counter_clr | 00000000 | | | | | | |
| 0x81c41d20: bbc_debug_en | 00000000 | | | | | | |
| 00200020 | | | | | | | |
| 0x81c41d28: bbc_rqc_rcc_thresh | 00000055 | | | | | | |
| bbc_bb_sc_n | 00000000 | | | | | | |
| | | 0x81c41d04: bbc_csc | | | | | |
| | | 0x81c41d0c: | | | | | |
| | | 0x81c41d14: | | | | | |
| | | 0x81c41d1c: | | | | | |
| | | 0x81c41d24: bbc_ctrl | | | | | |
| | | 0x81c41d34: | | | | | |

| | | |
|-------------------------------------|----------|-------------|
| 0x81c41d38: bbc_crd_reco_debug | 00000000 | 0x81c41d3c: |
| bbc_crd_reco_debug_data | 00000000 | |
| 0x81c41d40: bbc_multi_frm_loss_cnt | 00000000 | 0x81c41d44: |
| bbc_multi_rdy_loss_cnt | 00000000 | |
| 0x81c41d48: bbc_1frm_loss_recov_cnt | 00000000 | 0x81c41d4c: |
| bbc_1rdy_loss_recov_cnt | 00000000 | |
| 0x81c41d58: bbc_int_status | 00000000 | 0x81c41d5c: |
| bbc_int_set | 00000000 | |
| 0x81c41d60: bbc_int_first | 00000000 | 0x81c41d64: |
| bbc_frm_rdy_rx_err_addr | 00000000 | |
| 0x81c41d68: bbc_frm_rdy_tx_err_addr | 00000000 | 0x81c41d6c: |
| bbc_trc_mbc_err_addr | 00000000 | |
| 0x81c41d70: bbc_frm_rdy_rx_dbl_ecc | 00000000 | 0x81c41d74: |
| bbc_frm_rdy_tx_dbl_ecc | 00000000 | |
| 0x81c41d78: bbc_trc_mbc_dbl_ecc | 00000000 | |
| 0x81c41d7c: bbc_fsm_status | 00001011 | 0x81c41d80: |
| bbc_force_err | 00000000 | |
| 0x81c41d84: bbc_crdt_avail0 | ffffffff | 0x81c41d88: |
| bbc_crdt_avail1 | 000000ff | |
| 0x81c41d8c: bbc_scratch | 00000000 | |

FPS registers

=====

| | | |
|--------------------------------|----------|-------------|
| 0x81c40004: fps_er_enc_in | 00000000 | 0x81c40008: |
| fps_er_crc | 00000000 | |
| 0x81c4000c: fps_er_trunc | 00000000 | 0x81c40010: |
| fps_er_toolong | 00000000 | |
| 0x81c40014: fps_er_bad_eof | 00000000 | 0x81c40018: |
| fps_er_enc_out | 00000000 | |
| 0x81c4001c: fps_er_bad_os | 00000000 | 0x81c40020: |
| fps_er_flush | 00000000 | |
| 0x81c40024: fps_er_ifg | 00000000 | 0x81c40038: |
| fps_er_crc_good_eof | 00000000 | |
| 0x81c4003c: fps_inv_arb | 00000000 | 0x81c40040: |
| fps_slow_sts_status | 00000000 | |
| 0x81c40044: fps_tx_frm_cnt | 00000000 | 0x81c40048: |
| fps_rx_frm_cnt | 00000000 | |
| 0x81c40050: fps_tx_word_cnt_hi | 00000000 | 0x81c4004c: |
| fps_tx_word_cnt_lo | 00000000 | |
| 0x81c40058: fps_rx_word_cnt_hi | 00000000 | 0x81c40054: |
| fps_rx_word_cnt_lo | 00000000 | |

BAL registers

=====

| | | |
|---------------------------------|----------|-------------|
| 0x81c47000: bal_desired_buf | 00000000 | 0x81c47004: |
| bal_alloc_buf | 00000000 | |
| 0x81c47008: bal_busy_buf | 00000000 | 0x81c4700c: |
| bal_usable_buf | 00000000 | |
| 0x81c47010: bal_max_bor_buf | 00000000 | |
| 0x81c47014: bal_busy_buf_thresh | 00000002 | |

TXQ registers

=====

| | | |
|-------------------------------|----------|--|
| 0x81c43004: txq_phys_port_ctl | 00400000 | |
|-------------------------------|----------|--|

```

0x81c43050: txq_link_skew          00000000
0x81c43068: txq_cr_lk_dttm_intr_sts [00] 00000000 00000000
0x81c43070: txq_cr_lk_dttm_intr_en  [00] 00000000 00000000
0x81c43024: txq_disc_frm_trap_cnt    00000014

```

FDS registers

=====

```

0x81c44000: fds_rxf_ctl          00000002    0x81c44004:
fds_rxf_wait_thresh    00000909
0x81c44018: fds_rxf_first_error  00000000    0x81c4401c:
fds_rxf_first_error_info 00000000
0x81c44020: fds_rxf_inout_pkt_cnt 00000000
0x81c44008: fds_rxf_err_int_status 00000000    0x81c44024:
fds_rxf_fifo_status    00888888
0x81c45000: fds_txf_ctl          0000003a    0x81c45004:
fds_txf_wait_ifg_thresh 00a00106
0x81c45008: fds_txf_err_int_status 00000000    0x81c45024:
fds_txf_fifo_status    00088888
0x81c4502c: fds_txf_bbc_scs      00000000

```

Logical TXQ registers

=====

```

0x81c43000: txq_log_port_ctl      00000002    0x81c43008:
txq_port_status        00000000
0x81c4300c: txq_todo_flags        [00] 00000000 00000000
0x81c43014: txq_spd_match_desc    [00] 00000000 00000000 00000000
00000000
0x81c43024: txq_spd_match_desc    [04] 00000014
0x81c43028: txq_vc_weight        [00] 01010101 01010101 01010101
01010101
0x81c43038: txq_vc_weight        [04] 01010101 01010101 01010101
01010101
0x81c43048: txq_vc_weight        [08] 01010101 00010101
0x81c43054: txq_cong_dttm_ctrl    00000000
0x81c43058: txq_cong_dttm_intr_sts [00] 00000000 00000000
0x81c43060: txq_cong_dttm_intr_en [00] 00000000 00000000
0x81c43078: txq_bw_limit_en_reg   [00] 00000000 00000000
0x81c43080: txq_bw_gua_en_reg     [00] 00000000 00000000
0x81c43088: txq_vc_group          [00] 03030300 03030303 03030303
03030303
0x81c43098: txq_vc_group          [04] 03030303 03030303 03030303
03030303
0x81c430a8: txq_vc_group          [08] 03030303 03030303 00000000
00000000
0x81c430b0: txq_bw_thresh_group   [00] 00000000 00000000 00000000
00000000
0x81c430c0: txq_bw_thresh_group   [04] 00000000 00000000 00000000
00000000
0x81c430d0: txq_bw_thresh_group   [08] 00000000 00000000 00000000
00000000
0x81c430e0: txq_bw_thresh_group   [12] 00000000 00000000 00000000
00000000
0x81c430f0: txq_bw_thresh_group   [16] 00000000 00000000 00000000
00000000

```

```

0x81c43100: txq_bw_thresh_group [20] 00000000 00000000 00000000
00000000
0x81c43110: txq_bw_thresh_group [24] 00000000 00000000 00000000
00000000
0x81c43120: txq_bw_thresh_group [28] 00000000 00000000 00000000
00000000
0x81c43130: txq_bw_thresh_group [32] 00000000 00000000 00000000
00000000
0x81c43140: txq_bw_thresh_group [36] 00000000 00000000 00000000
00000000

```

txq Congestion detection Statistics RAM

=====

```

0x81090500: vc[0]          00000000          0x81090504: vc[1]
00000000
0x81090508: vc[2]          00000000          0x8109050c: vc[3]
00000000
0x81090510: vc[4]          00000000          0x81090514: vc[5]
00000000
0x81090518: vc[6]          00000000          0x8109051c: vc[7]
00000000
0x81090520: vc[8]          00000000          0x81090524: vc[9]
00000000
0x81090528: vc[10]         00000000          0x8109052c: vc[11]
00000000
0x81090530: vc[12]         00000000          0x81090534: vc[13]
00000000
0x81090538: vc[14]         00000000          0x8109053c: vc[15]
00000000
0x81090540: vc[16]         00000000          0x81090544: vc[17]
00000000
0x81090548: vc[18]         00000000          0x8109054c: vc[19]
00000000
0x81090550: vc[20]         00000000          0x81090554: vc[21]
00000000
0x81090558: vc[22]         00000000          0x8109055c: vc[23]
00000000
0x81090560: vc[24]         00000000          0x81090564: vc[25]
00000000
0x81090568: vc[26]         00000000          0x8109056c: vc[27]
00000000
0x81090570: vc[28]         00000000          0x81090574: vc[29]
00000000
0x81090578: vc[30]         00000000          0x8109057c: vc[31]
00000000
0x81090580: vc[32]         00000000          0x81090584: vc[33]
00000000
0x81090588: vc[34]         00000000          0x8109058c: vc[35]
00000000
0x81090590: vc[36]         00000000          0x81090594: vc[37]
00000000
0x81090598: vc[38]         00000000          0x8109059c: vc[39]
00000000

```

Logical STS registers

=====

| | | | |
|-------------|----------------------|----------------|------------------|
| 0x81584684: | sts_ftb_type1_miss | 00000000 | |
| 0x81584688: | sts_ftb_type2_miss | 00000000 | |
| 0x8158468c: | sts_ftb_type6_miss | 00000000 | |
| 0x81584690: | sts_hard_zoning_miss | 00000000 | |
| 0x81584694: | sts_lun_zoning_miss | 00000000 | |
| 0x8158469c: | sts_unroutable | 00000000 | |
| 0x815816b4: | sts_rte_cl2 | 00000000 | 0x815816b8: |
| sts_rte_cl3 | 00000000 | 0x815816bc: | sts_rte_link_ctl |
| 00000000 | 0x815846a8: | sts_tx_timeout | 00000000 |

Logical STS filter registers

=====

| | | | | | |
|-------------|-------------|------|----------|----------|----------|
| 0x81584600: | stsflt_trig | [00] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | | |
| 0x81584610: | stsflt_trig | [04] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | | |
| 0x81584620: | stsflt_trig | [08] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | | |
| 0x81584630: | stsflt_trig | [12] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | | |
| 0x81584640: | stsflt_trig | [16] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | | |
| 0x81584650: | stsflt_trig | [20] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | | |
| 0x81584660: | stsflt_trig | [24] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | | |
| 0x81584670: | stsflt_trig | [28] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | | |
| 0x81584680: | stsflt_trig | [32] | | | |

Logical STS discard registers

=====

| | | | |
|------------------------|------------------------|----------|-------------|
| 0x81581ba0: | disc_mcast_wka | 00000000 | 0x81581ba4: |
| disc_inv_did | 00000000 | | |
| 0x81581ba8: | disc_cl1_cl4 | 00000000 | 0x81581bac: |
| disc_sid_chk_fail | 00000000 | | |
| 0x81581bb0: | disc_inv_dom_egid_txpt | 00000000 | 0x81581bb4: |
| disc_vft_hop_cnt_1 | 00000000 | | |
| 0x81581bb8: | disc_classf | 00000000 | 0x81581bbc: |
| disc_fcp_cdb_inv | 00000000 | | |
| 0x81581bc0: | disc_vfid_trap_enabled | 00000000 | 0x81581bc4: |
| disc_vfid_hdr_chk_fail | 00000000 | | |
| 0x81581bc8: | disc_shim_cksum_fail | 00000000 | 0x81581bcc: |
| disc_fed_edit_cmd_err | 00000000 | | |
| 0x81581bd0: | disc_ftb_vm_mode | 00000000 | 0x81581bd4: |
| disc_ftb_agnt2_miss | 00000000 | | |
| 0x81581bd8: | disc_ecb_reserved | 00000000 | 0x81581bdc: |
| disc_ecb_de_pad_err | 00000000 | | |
| 0x81581be0: | disc_ecb_de_tag_err | 00000000 | 0x81581be4: |
| disc_ecb_de_seq_err | 00000000 | | |
| 0x81581be8: | disc_ecb_err | 00000000 | 0x81581bec: |

```

disc_ftb_type4_match      00000000
0x81581bf0: disc_fcp_rsp_ftb_type4  00000000      0x81581bf4:
disc_ftb_type5_match      00000000
0x81581bf8: disc_ftb_type3_match      00000000      0x81581bfc:
disc_els_ftb_type3        00000000
0x81581c00: disc_ftb_type1_match      00000000      0x81581c04:
disc_els_rsp_ex_port      00000000
0x81581c08: disc_inv_drp_dps          00000000      0x81581c0c:
disc_did_lookup_miss      00000000
0x81581c10: disc_ftb_type2_match      00000000      0x81581c14:
disc_trpd_plogi_pdisc     00000000
0x81581c18: disc_type2_lookup_miss    00000000      0x81581c1c:
disc_ftb_type6_match      00000000
0x81581c20: disc_els_rep_ex_port      00000000      0x81581c24:
disc_els_sid_lkup_bit1    00000000
0x81581c28: disc_els_sid_lkup_bit0    00000000      0x81581c2c:
disc_bls_frm_trap_bit1    00000000
0x81581c30: disc_ftb_token_err        00000000      0x81581c34:
disc_asic_internal_err    00000000
0x81581c38: disc_hard_zone_miss       00000000      0x81581c3c:
disc_lun_zone_miss        00000000
0x81581c40: discflt_frame_disc        00000000      0x81581c44:
discflt_parity_err        00000000
0x81581c48: disc_frame_marked_du      00000000      0x81581c4c:
disc_frame_marked_to      00000000
0x81581c50: disc_lkup_rte_prty_err   00000000

```

portstatsshow 48

```

stat_wtx      0      4-byte words transmitted
stat_wrx      0      4-byte words received
stat_ftx      0      Frames transmitted
stat_frx      0      Frames received
stat_c2_frx   0      Class 2 frames received
stat_c3_frx   0      Class 3 frames received
stat_lc_rx    0      Link control frames
received
stat_mc_rx    0      Multicast frames
received
stat_mc_to    0      Multicast timeouts
stat_mc_tx    0      Multicast frames
transmitted
tim_txcrd_z   0      Time TX Credit Zero
(2.5Us ticks)
tim_txcrd_z_vc 0- 3: 0      0      0      0
tim_txcrd_z_vc 4- 7: 0      0      0      0
tim_txcrd_z_vc 8-11: 0     0      0      0
tim_txcrd_z_vc 12-15: 0    0      0      0
lat_tot_pkt_vc 0- 3: 1      1      1      1
lat_tot_pkt_vc 4- 7: 1      1      1      1
lat_tot_pkt_vc 8-11: 1     1      1      1
lat_tot_pkt_vc 12-15: 1    1      1      1
lat_hi_time_vc 0- 3: 0      0      0      0
lat_hi_time_vc 4- 7: 0      0      0      0

```


| | | | | |
|------------------------------|-----------------------------|-------------------------|---|-----|
| lat_hi_time_vc 8-11: | 0 | 0 | 0 | 0 |
| lat_hi_time_vc 12-15: | 0 | 0 | 0 | 0 |
| lat_lo_time_vc 0- 3: | 1 | 1 | 1 | 1 |
| lat_lo_time_vc 4- 7: | 1 | 1 | 1 | 1 |
| lat_lo_time_vc 8-11: | 1 | 1 | 1 | 1 |
| lat_lo_time_vc 12-15: | 1 | 1 | 1 | 1 |
| max_latency_vc 0- 3: | 1 | 1 | 1 | 1 |
| max_latency_vc 4- 7: | 1 | 1 | 1 | 1 |
| max_latency_vc 8-11: | 1 | 1 | 1 | 1 |
| max_latency_vc 12-15: | 1 | 1 | 1 | 1 |
| latency_dma_ts | 09-09-2024 UTC Mon 08:47:25 | | | TXQ |
| Latency DMA TimeStamp | | | | |
| fec_cor_detected | 0 | Count of blocks that | | |
| were corrected by FEC | | | | |
| fec_uncor_detected | 0 | Count of blocks that | | |
| were left uncorrected by FEC | | | | |
| er_enc_in | 0 | Encoding errors inside | | |
| of frames | | | | |
| er_crc | 0 | Frames with CRC errors | | |
| er_trunc | 0 | Frames shorter than | | |
| minimum | | | | |
| er_toolong | 0 | Frames longer than | | |
| maximum | | | | |
| er_bad_eof | 0 | Frames with bad end-of- | | |
| frame | | | | |
| er_enc_out | 0 | Encoding error outside | | |
| of frames | | | | |
| er_bad_os | 0 | Invalid ordered set | | |
| er_pcs_blk | 0 | PCS block errors | | |
| er_rx_c3_timeout | 0 | Class 3 receive frames | | |
| discarded due to timeout | | | | |
| er_tx_c3_timeout | 0 | Class 3 transmit frames | | |
| discarded due to timeout | | | | |
| er_unroutable | 0 | Frames that are | | |
| unroutable | | | | |
| er_unreachable | 0 | Frame with unreachable | | |
| destination | | | | |
| er_other_discard | 0 | Other discards | | |
| er_type1_miss | 0 | frames with FTB type 1 | | |
| miss | | | | |
| er_type2_miss | 0 | frames with FTB type 2 | | |
| miss | | | | |
| er_type6_miss | 0 | frames with FTB type 6 | | |
| miss | | | | |
| er_zone_miss | 0 | frames with hard zoning | | |
| miss | | | | |
| er_lun_zone_miss | 0 | frames with LUN zoning | | |
| miss | | | | |
| er_crc_good_eof | 0 | Crc error with good eof | | |
| er_inv_arb | 0 | Invalid ARB | | |
| er_single_credit_loss | 0 | Single vcrdy/frame loss | | |
| on link | | | | |
| er_multi_credit_loss | 0 | Multiple vcrdy/frame | | |
| loss on link | | | | |

```

other_credit_loss      0          Link timeout/complete
credit loss
phy_stats_clear_ts    09-06-2024 UTC Fri 08:30:19    Timestamp of
phy_port_stats clear
lgc_stats_clear_ts    09-06-2024 UTC Fri 08:30:19    Timestamp of
lgc_port_stats clear
fec_corrected_rate    0          FEC Corrected blocks per
second

```

```
portstats64show 48
```

```

stat64_wtx      0          top_int : 4-byte words transmitted
                0          bottom_int : 4-byte words transmitted
stat64_wrx      0          top_int : 4-byte words received
                0          bottom_int : 4-byte words received
stat64_ftx      0          top_int : Frames transmitted
                0          bottom_int : Frames transmitted
stat64_frx      0          top_int : Frames received
                0          bottom_int : Frames received
stat64_c2_frx   0          top_int : Class 2 frames received
                0          bottom_int : Class 2 frames received
stat64_c3_frx   0          top_int : Class 3 frames received
                0          bottom_int : Class 3 frames received
stat64_lc_rx    0          top_int : Link control frames received
                0          bottom_int : Link control frames
received
stat64_mc_rx    0          top_int : Multicast frames received
                0          bottom_int : Multicast frames received
stat64_mc_to    0          top_int : Multicast timeouts
                0          bottom_int : Multicast timeouts
stat64_mc_tx    0          top_int : Multicast frames transmitted
                0          bottom_int : Multicast frames
transmitted
tim64_rdy_pri   0          top_int : Time R_RDY high priority
                0          bottom_int : Time R_RDY high priority
tim64_txcrd_z   0          top_int : Time BB_credit zero
                0          bottom_int : Time BB_credit zero
er64_enc_in     0          top_int : Encoding errors inside of
frames
                0          bottom_int : Encoding errors inside of
frames
er64_crc        0          top_int : Frames with CRC errors
                0          bottom_int : Frames with CRC errors
er64_trunc      0          top_int : Frames shorter than minimum
                0          bottom_int : Frames shorter than minimum
er64_toolong    0          top_int : Frames longer than maximum
                0          bottom_int : Frames longer than maximum
er64_bad_eof    0          top_int : Frames with bad end-of-frame
                0          bottom_int : Frames with bad end-of-
frame
er64_enc_out    0          top_int : Encoding error outside of
frames
                0          bottom_int : Encoding error outside of
frames
er64_disc_c3    0          top_int : Class 3 frames discarded

```

```

er64_pcs_blk      0          bottom_int : Class 3 frames discarded
                  0          top_int : PCS block errors
                  0          bottom_int : PCS block errors
stat64_rateTxFrame 0          Tx frame rate (fr/sec)
stat64_rateRxFrame 0          Rx frame rate (fr/sec)
stat64_rateTxPeakFrame 0      Tx peak frame rate (fr/sec)
stat64_rateRxPeakFrame 0      Rx peak frame rate (fr/sec)
stat64_rateTxWord  0          Tx Word rate (words/sec)
stat64_rateRxWord  0          Rx Word rate (words/sec)
stat64_rateTxPeakWord 0      Tx peak Word rate (words/sec)
stat64_rateRxPeakWord 0      Rx peak Word rate (words/sec)
stat64_PRJTFrames  0          top_int : Number of PRJT frames
returned to this port
                  0          bottom_int : Number of PRJT
frames returned to this port
stat64_PBSYFrames  0          top_int : Number of PBSY frames
returned to this port
                  0          bottom_int : Number of PBSY
frames returned to this port
stat64_inputBuffersFull 0      top_int : Number of occurrences
when all input buffers full
                  0          bottom_int : Number of
occurrences when all input buffers full
stat64_rxClass1Frames 0      top_int : Number of class 1
frames received
                  0          bottom_int : Number of class 1
frames received
stat64_aveTxFrameSize 0      Average Tx Frame size
stat64_aveRxFrameSize 0      Average Rx Frame size
Lr_in             0          top_int
                  0          bottom_int
Ols_in            0          top_int
                  0          bottom_int
Lr_out            0          top_int
                  0          bottom_int
Ols_out           0          top_int
                  0          bottom_int
Link_failure      0          top_int
                  0          bottom_int
Invalid_CRC       0          top_int
                  0          bottom_int
Invalid_word      0          top_int
                  0          bottom_int
Protocol_err      0          top_int
                  0          bottom_int
Loss_of_sig       0          top_int
                  0          bottom_int
Loss_of_sync      0          top_int
                  0          bottom_int
er_bad_os         0          top_int : Invalid ordered set
                  0          bottom_int: Invalid ordered set

```

```

port address ID: 0x013000
external unicast routing table:
  0: Embedded
 255: Embedded
internal unicast routing table:
  0: Embedded

```

```
portcamshow 48
```

```

-----
Port  SID used  DID used  SID entries  DID entries
48    0         0         000000      000000
-----

```

```
ptbufshow, ptcridtshow, ptdatashow, ptstatsshow 48
```

```

S:
S:VF Enable:          1
S:
S:C4 Global Variable:
S:-----

```

```

S:trace_stop:        0
S:
S:C4 Phy Data Pointers: c4_phyp = 0xb6ac2080
S:-----

```

```

S:tnodep              0xbb8342a0      pt
   0x43028008
S:proto_phyp          0xb8807480      phy_cfg
0xb6ac30c0
S:c4_chp              0x97e28000      c4_lgcp
0x97f68000
S:c4_phy_regp         0x81c40000      proc_dir
0xb8515500
S:-----

```

```

S:magic_id            0xc4345678      num_port_timer      12
S:prev_if_id         0x43020008      S:ftx                0
   tov              0
S:initialized         0          port_idx             8
S:ui_idx              48          slot_no
   0
S:blade_idx          8          sw_usr_ports         400
S:unused              0          intr_debounced
   0
S:aec_status         0x0          reason_code
   0
S:debug              0x00000004      debug_trc_line       0
S:rxbuf_list_head    0xffffffff      rxbuf_list_tail
0xffffffff
S:isAePort            0          port_misc_data
   0
S:num_fault1_rx_disc  0          num_fault2_rx_disc   0
S:p_lli_cause0        0          p_sig_regained        0
S:p_sync_regained     0          enc_out

```

```

0x0
S:cached_fps_status      0          cached_sts_status      0
S:cached_er_crc_good_eof      0          cached_er_too_long     0
S:cached_er_bad_os          0
S:cached_er_trunc          0
cached_tot_er_crc_good_eof    0
S:num_pt_excess_intr      0          num_no_fid             0
S:num_fault1_cnt          0          num_fault2_cnt        0
0
S:num_fault_lip           0          num_fault_llli        0
S:num_fault_rx_fifo       0          num_fault_hss         0
S:num_fault_bwait         0          lli_intr_prim         0
0
S:num_sw_link_to          0
be_link_err_mon_count        0
S:ecb_enc_enabled         0          ecb_comp_enabled      0
0
S:ecb_rsv_enc             0          ecb_rsv_comp          0
S:ecb_enc_bm              0x0       ecb_key_index         0
0xffffffff
S:fab_idx                 4
S:num_be_lto              0          lto_count_reset_intvl
0
S:lr_count_reset_intvl    0          num_be_lr             0
0
S:num_fault_qsf           0          check_lto             0
0
S:credit_loaded          0          num_credit_overrun    0
0
S:fec_enabled             0x0       fec_los_to_flag       0x0
S:phy_stats_clear_ts      0          1725611419           pcs_err_online
0
S:pcs_err_light_det       0          pcs_err_ignore        0
0
S:pcs_blk_err            0          pcs_hiber             0
S:phy_port_status         0          ecb_enc_lr_count      0
0
S:dport_mode              0          avoid_lto_det         0
S:sn_debounced           0x0       sn_started_kr_reqd    0
S:major_timer_started     0x0       ready_bm              0x0
S:parln_1_bm              0x0       parln_0_bm            0x0
S:be_los_of_sync_event_intvl 0          0
be_los_of_sync_event        0
S:errataPtenable_cntr     0          errataPoll_cntr      0
0
S:jda_rx_sig_loss_det     0          jda_rx_sig_loss_cnt  0
0
S:encrypt_blk_error       0
S:
S:      c4_trunk
S:=====
S:mark_ts                  0x0       deskew                0x0
S:master_phyp              0x0
S:

```

```

S:adelay[00]: 0x00000000 0x00000000 0x00000000 0x00000000
S:adelay[04]: 0x00000000 0x00000000 0x00000000 0x00000000
S:
S:      c4_buf
S:=====
S:tx_csc          0          rx_csc
      0
S:ld_vc_credits  0          tx_flag          0x0
S:alloc_buffers  0          req_buffers     0
S:est_buffers    20        ld_use_est    0
S:bb_sc_n        0          rx_bb_sc_n
      0
S:data_cr        5          nondata_cr
      6
S:cr_enable      0
S:ld_nondata_cr  6          tnodep
0xbb834380
S:tx_credits[0] 0  0  0  0  0  0  0  0
S:tx_credits[8] 0  0  0  0  0  0  0  0
S:tx_credits[16]    0  0  0  0  0  0  0  0  0
S:tx_credits[24]    0  0  0  0  0  0  0  0  0
S:tx_credits[32]    0  0  0  0  0  0  0  0  0
S:rx_credits[0] 0  0  0  0  0  0  0  0
S:rx_credits[8] 0  0  0  0  0  0  0  0
S:rx_credits[16]    0  0  0  0  0  0  0  0  0
S:rx_credits[24]    0  0  0  0  0  0  0  0  0
S:rx_credits[32]    0  0  0  0  0  0  0  0  0
S:tx_mbc[0]    0  0  0  0  0  0  0  0
S:tx_mbc[8]    0  0  0  0  0  0  0  0
S:tx_mbc[16]   0  0  0  0  0  0  0  0
S:tx_mbc[24]   0  0  0  0  0  0  0  0
S:tx_mbc[32]   0  0  0  0  0  0  0  0
S:rx_mbc[0]    0  0  0  0  0  0  0  0
S:rx_mbc[8]    0  0  0  0  0  0  0  0
S:rx_mbc[16]   0  0  0  0  0  0  0  0
S:rx_mbc[24]   0  0  0  0  0  0  0  0
S:rx_mbc[32]   0  0  0  0  0  0  0  0
S:
S:C4 Chip Variables: c4_phyp->c4_chp = 0x97e28000
S:-----
-----
S:version = 2.1
S:magic_id      0xc4234567  init_state      0x8
S:reset_reg_mem 0x1
S:ch_int0_en_bm 0x0          intr0_cause     0x0
S:ch_int1_en_bm 0x0          intr1_cause     0x0
S:ch_int2_en_bm 0x0          intr2_cause     0x0
S:ch             0x43010080  ch_cfg
0xb7013ba0
S:raslog_hdl.hndl 0x0          obj_halted     0x0
S:c4_chip_regp   0x80000000  c4_fpg_regp
0x81800000
S:num_chip_timer 0x5
S:hi_task_bm     0x0          lo_task_bm     0x0

```

| | | | |
|-----------------------------|-----------------------|-----------------------|-----|
| S:c4_deferq.q_head | 0x0 | c4_deferq.q_tail | 0x0 |
| S:c4_tmrq.q_head | 0x0 | c4_tmrq.q_tail | 0x0 |
| slot_no | 0 | | |
| S:chip_inst | 0 | chip_idx | 0 |
| S:pll_initialized | 1 | | |
| pll_serdes_initialized | 1 | | |
| S:init_tries | 0 | init_ptEnableBM | |
| 0xba01b488 | | | |
| S:tick_polling | 0xb980c9c0 | sec_polling | |
| 0xb980c960 | | | |
| S:bb_fid | 129 | | |
| S:ecb_key_bm[0] | 0x0 | ecb_key_bm[1] | 0x0 |
| S:ecb_key_bm[2] | 0x0 | ecb_key_bm[3] | 0x0 |
| S:is_chip_enc_enabled | | 0 | |
| is_chip_comp_enabled | 0x0 | | |
| S:ftb_rsrcp->ftb_flags | 0x0 | act_rsrcp->act_flag | 0x1 |
| S:lue_rsrcp->lue_flags[0] | 0x0 | lue_rsrcp- | |
| >lue_flags[1] | 0x0 | | |
| S:c4_phyp[00]: | 0xb6ab0000 0xb6ab2080 | 0xb6ab4100 0xb6ab6180 | |
| S:c4_phyp[04]: | 0xb6ab9040 0xb6abb0c0 | 0xb6abd140 0xb6ac0000 | |
| S:c4_phyp[08]: | 0xb6ac2080 0xb6ac4100 | 0xb6ac6180 0xb6ac9040 | |
| S:c4_phyp[12]: | 0xb6ac60c0 0xb6acd140 | 0xb6ad0000 0xb6ad2080 | |
| S:c4_phyp[16]: | 0xb6ad4100 0xb6ad6180 | 0xb6ad9040 0xb6adb0c0 | |
| S:c4_phyp[20]: | 0xb6add140 0xb6ae0000 | 0xb6ae2080 0xb6ae4100 | |
| S:c4_phyp[24]: | 0xb6ae6180 0xb6ae9040 | 0xb6aeb0c0 0xb6aed140 | |
| S:c4_phyp[28]: | 0xb6af0000 0xb6af2080 | 0xb6af4100 0xb6af6180 | |
| S:c4_phyp[32]: | 0xb6af9040 0xb6afb0c0 | 0xb6afd140 0xb6b00000 | |
| S:c4_phyp[36]: | 0xb6b02080 0xb6b04100 | 0xb6b06180 0xb6b09040 | |
| S:c4_phyp[40]: | 0xb6b0b0c0 0xb6b0d140 | 0xb6b10000 0xb6b12080 | |
| S:c4_phyp[44]: | 0xb6b14100 0xb6b16180 | 0xb6b19040 0xb6b1b0c0 | |
| S:c4_phyp[48]: | 0xb6b1d140 0xb6b20000 | 0xb6b22080 0xb6b24100 | |
| S:c4_phyp[52]: | 0xb6b26180 0xb6b29040 | 0xb6b2b0c0 0xb6b2d140 | |
| S:c4_phyp[56]: | 0xb6b30000 0xb6b32080 | 0xb6b34100 0xb6b36180 | |
| S:c4_phyp[60]: | 0xb6b39040 0xb6b3b0c0 | 0xb6b3d140 0xb6b40000 | |
| S:c4_lgcp[00]: | 0x97f48000 0x97f4c000 | 0x97f50000 0x97f54000 | |
| S:c4_lgcp[04]: | 0x97f58000 0x97f5c000 | 0x97f60000 0x97f64000 | |
| S:c4_lgcp[08]: | 0x97f68000 0x97f6c000 | 0x97f70000 0x97f74000 | |
| S:c4_lgcp[12]: | 0x97f78000 0x97f7c000 | 0x97f80000 0x97f84000 | |
| S:c4_lgcp[16]: | 0x97f88000 0x97f8c000 | 0x97f90000 0x97f94000 | |
| S:c4_lgcp[20]: | 0x97f98000 0x97f9c000 | 0x97fa0000 0x97fa4000 | |
| S:c4_lgcp[24]: | 0x97fa8000 0x97fac000 | 0x97fb0000 0x97fb4000 | |
| S:c4_lgcp[28]: | 0x97fb8000 0x97fbc000 | 0x97fc0000 0x97fc4000 | |
| S:c4_lgcp[32]: | 0x97fc8000 0x97fcc000 | 0x97fd0000 0x97fd4000 | |
| S:c4_lgcp[36]: | 0x97fd8000 0x97fdc000 | 0x97fe0000 0x97fe4000 | |
| S:c4_lgcp[40]: | 0x97fe8000 0x97fec000 | 0x97ff0000 0x97ff4000 | |
| S:c4_lgcp[44]: | 0x97ff8000 0x97ffc000 | 0x8e000000 0x8e004000 | |
| S:c4_lgcp[48]: | 0x8e008000 0x8e00c000 | 0x8e010000 0x8e014000 | |
| S:c4_lgcp[52]: | 0x8e018000 0x8e01c000 | 0x8e020000 0x8e024000 | |
| S:c4_lgcp[56]: | 0x8e028000 0x8e02c000 | 0x8e030000 0x8e034000 | |
| S:c4_lgcp[60]: | 0x8e038000 0x8e03c000 | 0x8e040000 0x8e044000 | |
| S:chip_timers[00]: | 0xb980c720 0xb980c780 | 0xb980c7e0 0xb980c840 | |
| S:chip_timers[04]: | 0xb980c8a0 0xb980c900 | | |
| S:disc_trap_enable_required | 0x0 | rxlp_disc_log_stop | |
| 0x0 | | | |

```

S:curr_rxlp_frm_cnt      0x0          curr_rxlp_disc_frm_cnt  0x0
S:sw_disc_frm_cnt       0x0          last_disc_frm_cnt      0x0
S:txq_nopop_pr_cnt     0x0          pollErrataDfe_ptBM
0xba01b4b0

```

```

S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][0]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][1] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][2]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][0] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][1]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][2] 0x0

```

```

S:
S:C4 Logical Port Variables

```

```

S:-----
-----

```

```

S:c4_lgc_regp          0x81c40000
S:c4_phyp:
S:      0xb6ac2080      0x0          0x0          0x0

S:      0x0            0x0          0x0          0x0

S:master_phyp         0xb6ac2080      if_id
0x43020008
S:min_phyp            0x0          max_phyp          0x0
S:num_phy_ports      1          lgc_num          8
S:num_iu_to          0          sw_txq_bm
0

S:port_fid           129          unused          0
S:port_group        1          lgc_stats_clear_ts
1725611419

S:domain_tbl_sel     0          area_tbl_sel
0

S:egid_tbl_sel       0
S:serv_lo_bm         0x0

```

```

S:
S:Proto Phy Variables:

```

```

S:-----
-----

```

```

S:magic_id           0xc4123456      asic_phyp
0xb6ac2080
S:port_id            0x43028008      phy_cfg
0xb6ac30c0

S:upsm_hdl           0xb8011be0      physm_hdl
0xb8011960
S:ov_snsn_hdl        0xb8011820      sw_snsn_hdl
0xb80118c0
S:ov_lksm_hdl        0xb8011a00      sw_lksm_hdl
0xb8011aa0
S:trksm_hdl          0xb8011b40      lr_flag          0x0
S:lr_active          0x0          qsfm_txrx_rate_sel
0x0

```

```

S:
S:UPSM      UP00: UPST_PORT_DISABLED    --> UP00: UPST_PORT_DISABLED
S:SNSM(OV)  SN00: OV_SNST_STOPPED      --> SN00: OV_SNST_STOPPED
S:SNSM(SW)  SW00: SW_SNST_STAGE_WS     --> SW00: SW_SNST_STAGE_WS

```


S:PHYSM PP00: PHYST_STOPPED --> PP00: PHYST_STOPPED
 S:LKSM(OV) LK00: OV_LKST_INACTIVE --> LK00: OV_LKST_INACTIVE
 S:LKSM(SW) SW13: INACTIVE --> SW13: INACTIVE
 S:TRKSM TRK0: TRKST_INIT --> TRK0: TRKST_INIT

S:
 S:physm variables:

S:-----

 S:proto_phyp 0xb8807480 physm_hdl
 0xb8011960
 S:force_offline 0 copper 0
 S:fault_reason 0: UNKNOWN
 S:phy_media_present 0

S:
 S:sns variables:

S:-----

 S:speed 0xff proto_phyp
 0xb8807480
 S:hw_sn_tries_left 0x0 sw_sn_tries_left 0x0
 S:curr_txsp_count 0x0
 S:tx_max 0x0 curr_tx_indx
 0x0
 S:curr_tx 0x0 curr_rxsp_count
 0x0
 S:rx_max 0x0 curr_rx_indx
 0x0
 S:curr_rx 0x0 rx_mem
 0x0
 S:rxsp_rec_count 0x0
 S:nc_start 0x0 tx_start 0x0
 S:sync_start 0x0 sync_present 0x0
 S:diag_auto 0x0 diag_speed 0xff
 S:striped_wd_tov 3000 hw_wd_tov
 3000
 S:step 0x0 qsfp28_speed_mode
 0x0
 S:qsfp_mode0_hw_sn_tries_left 0x0
 S:qsfp_mode1_hw_sn_tries_left 0x0

S:
 S:lksm variables:

S:-----

 S:proto_phyp 0xb8807480 ov_lksm_hdl
 0xb8011a00
 sw_lksm_hdl 0xb8011aa0
 num_lf1 0
 S:hw_link_tries_left 0 sw_link_tries_left 0
 S:buf_ptype 0x0 stored_entry_state 0x6
 S:handshake_owner 0x0 mark_unsent
 0x0
 S:busybuf_stuck 0x0 lr_wait 0x0

S:
 S:trksm variables:

S:-----

S:Not a trunk port

S:

S:upsm variables:

S:-----

S:proto_phy 0xb8807480 upsm_hdl
0xb8011be0
S:bb_credits 0 port_beacon 0
S:port_diag_flag 0 force_offline
0
S:port_fault_rsn 0: PORT_NO_FAULT
S:retry_init_rsn 0: UNKNOWN
S:linit_reason 0 linit_result 0
S:ie_fctl_mode 0 fec_in_sync_tries_left 0
S:retry_sn_fail_init 0
retry_link_fail_init 0
S:excess_lr_count 0
S:

S:c4_ch_cfg

S:-----

S:c4_desc_ring_size 256 292 256 256 292
292 2 292 292
S:thresh_def 0 16 1 0
S:intr_tries 500 cmem_pattern
0xdeadbeef
S:cmem_pattern_upwd 2 cmem_init_time 16
S:cmem_init_tries 5
S:ctrl_par_thresh 2 data_par_thresh
4
S:cam_par_thresh 4 buf_loss_thresh
12
S:crit_par_thresh 2 non_crit_par_thresh
6
S:pci_abort_thresh 10 pci_err_thresh 5
S:excess_chintr_thresh 8 sw_err_thresh 20
S:err_sample_period 300 intr_sleep
20000
S:frame_timeout 2500 proxy_dev 16384
S:vf_route 81920 qos 2048
S:stats 2048 f_redirect 2048
S:rsp_trap 2048 lun_zoning 20480
S:area_mode 0 ftb_max_loop[0] 0
S:ftb_max_loop[1] 6 ftb_max_loop[2] 9
S:ftb_max_loop[3] 10 ftb_max_loop[4] 10
S:ftb_max_loop[5] 5 ftb_max_loop[6] 6
S:ftb_seg_size[0] 0 ftb_seg_size[1]
16384
S:ftb_seg_size[2] 65536 ftb_seg_size[3]
16384
S:ftb_seg_size[4] 16384 ftb_seg_size[5]
65536

```

S:ftb_seg_size[6]          16384          ftb_seg_base[0]          0
S:ftb_seg_base[1]          0          ftb_seg_base[2]
65536
S:ftb_seg_base[3]          16384          ftb_seg_base[4]
32768
S:ftb_seg_base[5]          131072         ftb_seg_base[6]
49152
asic_err_monitor_period1    300
asic_err_monitor_period2    86400
zone_chk_to_poll_period 25
zone_chk_class2_reject_tov  220
S:
S:c4_phy_cfg
S:-----
-----
S:version = 2.1
S:pt          0x43028008          fab_ptr
0x9a800000
S:fabattr          0x9a8000d4          fab_iop
0x9a800050
S:cfgbm          0xbb8340e4          port_ctrl
0xb6ac30d8
S:pcap.pcap_bm          0x8d215547          pcap.pcap2_bm
0x2588289
S:pcap.pcap3_bm          0x1bebe0c
ui_idx          48          S:slot_no
0
is_icl          0          S:sw_usr_ports          400
S:neg_speed          0 0 0 0 0 0
S:my_domain          0x1          port_mode          0x0
S:hw_sn_maxtries          100          sw_sn_maxtries
0
S:hw_link_maxtries          10          sw_link_maxtries          5
S:rx_cyc_tov          28          rttov          300
S:bufrdy_tov          300          busybuf_tov          286
S:mark_tov          300          lksm_tov          3000
S:buf_dealloc_wait          4          hw_wd_tov          3000
S:hw_lk_train_tov          540          hw_lk_test_tov
150
S:syswait_tx_12_lips          1          lip_rx_tov          55
S:al_time_tov          15          lp_tov          2000
S:intr_tries_port          500          intr_mod_debounce
250
S:intr_lsrflt_debounce          500          intr_efifo_debounce          100
S:port_no_fid          3          excess_ptintr_thresh          8
S:port_fault1_thresh          100          port_fault1_spur_thresh          250
S:port_fault1_disc_thresh          500
port_fault1_disc_spur_thresh          1000
S:port_fault2_thresh          5          losync_tov          100
S:port_sw_link_to          15          en_8g_scramble
1
frc_hw_sn_mode          0x1
S:enc_poll_thresh          0          fec_enable
0

```

```

S:fec_in_sync_to          50          fec_in_sync_try_max
   4
S:port_be_lto_threshold   100          port_be_lr_threshold
   2
S:be_cr_in_sync_to        5
port_credit_overrun_thresh          10
S:jda_sfp_losig_tov       400
jda_sfp_losig_try_max    30
S:striped_wd_tov         3000
no_sync_debounce         1200
S:
S:      fab_iop
S:=====
S:fab_iop->interop_mode 0x0          fab_iop->lab_mode          0x0
S:fab_iop->fl_bbc        0x0          fab_iop->fl_fan
   0x0
S:fab_iop->fl_cls        0x4          fab_iop->fl_rscn
   0x0
S:fab_iop->domain_id_offset 0x60          fab_iop-
>mcdt_fabric_mode      0x0
S:fab_iop->mcdt_default_zone          0x0          fab_iop-
>mcdt_safe_zone        0x0
S:
S:      port_ctrl
S:=====
S:port_ctrl.port_type    1          port_ctrl.port_grp        1
S:port_ctrl.port_number 48          port_ctrl.vc_mode         1
S:
S:      port_ctrl.lcap
S:=====
S:has_serdes             0          has_media                  1
S:topology               1          skip_nego                  0
S:skip_pnego             0          skip_init_event           0
S:en_shim                 0          speed_neg
   1
S:loop_back              0          num_speeds                 5
S:fec_enable             0
S:
S:      port_ctrl.speed_list array
S:=====
S:speed_list[0].auto_neg 1          speed_list[0].lnk_speed   0x0000000a
S:speed_list[1].auto_neg 1          speed_list[1].lnk_speed   0x00000008
S:speed_list[2].auto_neg 1          speed_list[2].lnk_speed   0x00000006
S:speed_list[3].auto_neg 1          speed_list[3].lnk_speed   0x00000005
S:speed_list[4].auto_neg 1          speed_list[4].lnk_speed   0x00000003
S:speed_list[5].auto_neg 0          speed_list[5].lnk_speed   0x00000000
S:
S:      port_ctrl.cm
S:=====
S:port_ctrl.cm.num_vcs    8
S:port_ctrl.cm.min_bufs   8
S:port_ctrl.cm.cr_shar_bufs 0
S:port_ctrl.vc_alloc
S:port_ctrl.vc_alloc      2 0 1 1 1 1 1 1

```

```

S:port_ctrl.vc_alloc          0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.norm_vc_alloc
S:port_ctrl.norm_vc_alloc    4 0 5 5 5 5 1 1
S:port_ctrl.norm_vc_alloc    0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.cm.skip_bb_credit      0
S:port_ctrl.cm.use_shim_based_sublist      0
S:
S:      port_ctrl.serdes_set
S:=====
S:serdes_type          0x8
S:serdes_data_t.ibm_hss_serdes.tx_drive_power      0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b_sign  0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b      0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_a      0x0
S:serdes_data_t.ibm_hss_serdes.rxeq              0x0
S:
S:      cfgbm
S:=====
S:old_distance          0x0          gport_lockdown      0x0
S:tport                0x1          speed              0x0
S:disable_eport        0x0          fcacc              0x0
S:lport_lockdown      0x0          0x0                priv_lport_lockdown
0x0
S:vcxlt_linit          0x0          delay_flogi        0x0
S:isl_interop          0x0          distance           0x0
S:BufStarvFlag        0x0          credit_sharing     0x0
S:lport_halfduplex    0x0          lport_fairness     0x0
S:soft_neg             0x0          asn_frc_hwretry    0x0
S:cr_recov             0x0          fport_buffers      0x0
S:export               0x0          0x0                export_mode
0x0
S:csctl_en             0x0          mirror_port        0x0
S:fault_delay          0x0          non_dfe            0x0
S:fec_configured*(0=ENAB)  0          fec_tts
0
S:port_persistently_disabled (permanently) 0 (0)
S:
S:      cfg property
S:=====
S:priv_pcfg_bm          0x00000000      lgcl_pcfg_bm
0xbb834124
S:fport_buffer          0x00000000
S:
S:
S:C4 Discard Cntrs: rxlp_stats = 0xb6ac2430
S:-----
-----
S:disc_mcast_wka        0x0          disc_inv_did        0x0
S:disc_cl1_cl4         0x0          disc_sid_chk_fail   0x0
S:disc_inv_dom_egid_txpt 0x0          disc_vft_hop_cnt_1
0x0
S:disc_classf          0x0          disc_fcp_cdb_inv    0x0

```

```

S:disc_vfid_trap_enabled          0x0
disc_vfid_hdr_chk_fail 0x0
S:disc_shim_cksum_fail 0x0      disc_fed_edit_cmd_err 0x0
S:disc_shim_cksum_fail 0x0      disc_fed_edit_cmd_err 0x0
S:disc_ftb_vm_mode 0x0          disc_ftb_agn_t2_miss 0x0
S:disc_ecb_de_pad_err 0x0       disc_ecb_de_tag_err 0x0
S:disc_ecb_de_seq_err 0x0       disc_ecb_err 0x0
S:disc_ftb_type4_match 0x0      disc_fcp_rsp_ftb_type4 0x0
S:disc_fcp_rsp_ftb_type4 0x0    disc_ftb_type5_match
0x0
S:disc_ftb_type3_match 0x0      disc_els_ftb_type3 0x0
S:disc_ftb_type1_match 0x0      disc_els_rsp_ex_port 0x0
S:disc_inv_drp_dps 0x0          disc_did_lookup_miss 0x0
S:disc_ftb_type2_match 0x0      disc_trpd_plogi_pdisc 0x0
S:disc_type2_lookup_miss 0x0    disc_ftb_type6_match
0x0
S:disc_els_rep_ex_port 0x0      disc_els_sid_lkup_bit1 0x0
S:disc_els_sid_lkup_bit0 0x0
disc_bls_frm_trap_bit1 0x0
S:disc_ftb_token_err 0x0        disc_asic_internal_err 0x0
S:disc_hard_zone_miss 0x0       disc_lun_zone_miss 0x0
S:discflt_frame_disc 0x0        discflt_parity_err 0x0
S:disc_frame_marked_du 0x0      disc_frame_marked_to 0x0

```

```

E:Connection type: FE
E:Port type: E_port
E:Trunk port: No
E:Configured Speed: AUTO_SPEED_NEGO
E:Max Capable Speed: 32G
E:Current SNSM Speed: UNDEFINED
E:Hardware TX Speed: 32G (0x00000004)
E:Hardware RX Speed: 32G (0x00000040)

```

```

E:
E:Interrupts: 0      Link_failure: 0
Loss_of_sync: 0      Loss_of_sig: 0
E:Lli: 0             Invalid_word: 0
E:trapped_frm: 0     fwd_status_ok: 0
E:fwd_timeout: 0     fwd_tx_unavail: 0
E:fwd_unroutable: 0     fwd_zone_out: 0
E:fwd_other_err: 0     frm_err_discard: 0
E:Fltr listA: 0       Fltr listB: 0
E:Zone trap fwd: 0     Zone trap disc: 0
E:shim_csum: 0        RTE_perr: 0
E:Invalid_crc: 0      Delim_err: 0
E:Protocol_err: 0
E:Lr_in: 0            Lr_out: 0
E:Ols_in: 0           Ols_out: 0

```

filterportshow 48

FILTER DATA

```

Shadow settings:
  Filter Enable: 0x00000000

```

Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass: 0x00000000

Real settings:

Enable RAM: 0x00000000, 0x00000000

Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000

Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass RAM: 0x00000000

Shadowed filters:

Filter 0: Not Installed (MIRROR1)(LISTA)
c4_fldenable[0] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[0] = 0x00000000,c4_fltr_config[0] = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
c4_fldenable[1] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[1] = 0x00000000,c4_fltr_config[1] = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
c4_fldenable[2] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[2] = 0x00000000,c4_fltr_config[2] = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
c4_fldenable[3] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[3] = 0x00000000,c4_fltr_config[3] = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
c4_fldenable[4] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[4] = 0x00000000,c4_fltr_config[4] = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
c4_fldenable[5] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[5] = 0x00000000,c4_fltr_config[5] = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
c4_fldenable[6] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[6] = 0x00000000,c4_fltr_config[6] = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
c4_fldenable[7] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[7] = 0x00000000,c4_fltr_config[7] = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
c4_fldenable[8] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[8] = 0x00000000,c4_fltr_config[8] = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)


```
    c4_fldenable[9] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[9] = 0x00000000,c4_fltr_config[9] = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
    c4_fldenable[10] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[10] = 0x00000000,c4_fltr_config[10] =
0x00000000
Filter 11: Not Installed (SIM)(LISTA)
    c4_fldenable[11] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[11] = 0x00000000,c4_fltr_config[11] =
0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
    c4_fldenable[12] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[12] = 0x00000000,c4_fltr_config[12] =
0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
    c4_fldenable[13] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[13] = 0x00000000,c4_fltr_config[13] =
0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
    c4_fldenable[14] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[14] = 0x00000000,c4_fltr_config[14] =
0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
    c4_fldenable[15] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[15] = 0x00000000,c4_fltr_config[15] =
0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
    c4_fldenable[16] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[16] = 0x00000000,c4_fltr_config[16] =
0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
    c4_fldenable[17] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[17] = 0x00000000,c4_fltr_config[17] =
0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
    c4_fldenable[18] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[18] = 0x00000000,c4_fltr_config[18] =
0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
    c4_fldenable[19] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[19] = 0x00000000,c4_fltr_config[19] =
0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
```

```
    c4_fldenable[20] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[20] = 0x00000000,c4_fltr_config[20] =
0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
    c4_fldenable[21] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[21] = 0x00000000,c4_fltr_config[21] =
0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
    c4_fldenable[22] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[22] = 0x00000000,c4_fltr_config[22] =
0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
    c4_fldenable[23] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[23] = 0x00000000,c4_fltr_config[23] =
0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
    c4_fldenable[24] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[24] = 0x00000000,c4_fltr_config[24] =
0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
    c4_fldenable[25] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[25] = 0x00000000,c4_fltr_config[25] =
0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
    c4_fldenable[26] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[26] = 0x00000000,c4_fltr_config[26] =
0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
    c4_fldenable[27] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[27] = 0x00000000,c4_fltr_config[27] =
0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
    c4_fldenable[28] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[28] = 0x00000000,c4_fltr_config[28] =
0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
    c4_fldenable[29] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[29] = 0x00000000,c4_fltr_config[29] =
0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    c4_fldenable[30] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[30] = 0x00000000,c4_fltr_config[30] =
0x00000000
```

Filter 31: Not Installed (IPM2)(LISTA)
c4_fldenable[31] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[31] = 0x00000000,c4_fltr_config[31] =
0x00000000

Real filters:

Filter 0: Not Installed (MIRROR1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 11: Not Installed (SIM)(LISTA)

fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,

```

    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter dirty indicator: 0x00000000
Performance filters: 0
Port Mirror filters: 0 (0x0)

```

FIELD DATA

Shadowed fields:

```

fldoffset[0] = 0x00, fldmask[0] = 0x00, fldvalue_dyna[0]: 0x00 0x00
0x00 0x00
fldcontrol[0].inuse = 0x0  fldcontrol[0].refcnt = 0x00 0x00 0x00
0x00
fldoffset[1] = 0x00, fldmask[1] = 0x00, fldvalue_dyna[1]: 0x00 0x00
0x00 0x00
fldcontrol[1].inuse = 0x0  fldcontrol[1].refcnt = 0x00 0x00 0x00
0x00
fldoffset[2] = 0x00, fldmask[2] = 0x00, fldvalue_dyna[2]: 0x00 0x00
0x00 0x00
fldcontrol[2].inuse = 0x0  fldcontrol[2].refcnt = 0x00 0x00 0x00
0x00
fldoffset[3] = 0x00, fldmask[3] = 0x00, fldvalue_dyna[3]: 0x00 0x00
0x00 0x00

```

```
fldcontrol[3].inuse = 0x0 fldcontrol[3].refcnt = 0x00 0x00 0x00
0x00
fldoffset[4] = 0x00, fldmask[4] = 0x00, fldvalue_dyna[4]:0x00 0x00
0x00 0x00
fldcontrol[4].inuse = 0x0 fldcontrol[4].refcnt = 0x00 0x00 0x00
0x00
fldoffset[5] = 0x00, fldmask[5] = 0x00, fldvalue_dyna[5]:0x00 0x00
0x00 0x00
fldcontrol[5].inuse = 0x0 fldcontrol[5].refcnt = 0x00 0x00 0x00
0x00
fldoffset[6] = 0x00, fldmask[6] = 0x00, fldvalue_dyna[6]:0x00 0x00
0x00 0x00
fldcontrol[6].inuse = 0x0 fldcontrol[6].refcnt = 0x00 0x00 0x00
0x00
fldoffset[7] = 0x00, fldmask[7] = 0x00, fldvalue_dyna[7]:0x00 0x00
0x00 0x00
fldcontrol[7].inuse = 0x0 fldcontrol[7].refcnt = 0x00 0x00 0x00
0x00
fldoffset[8] = 0x00, fldmask[8] = 0x00, fldvalue_dyna[8]:0x00 0x00
0x00 0x00
fldcontrol[8].inuse = 0x0 fldcontrol[8].refcnt = 0x00 0x00 0x00
0x00
fldoffset[9] = 0x00, fldmask[9] = 0x00, fldvalue_dyna[9]:0x00 0x00
0x00 0x00
fldcontrol[9].inuse = 0x0 fldcontrol[9].refcnt = 0x00 0x00 0x00
0x00
fldoffset[10] = 0x00, fldmask[10] = 0x00, fldvalue_dyna[10]:0x00 0x00
0x00 0x00
fldcontrol[10].inuse = 0x0 fldcontrol[10].refcnt = 0x00 0x00 0x00
0x00
fldoffset[11] = 0x00, fldmask[11] = 0x00, fldvalue_dyna[11]:0x00 0x00
0x00 0x00
fldcontrol[11].inuse = 0x0 fldcontrol[11].refcnt = 0x00 0x00 0x00
0x00
fldoffset[12] = 0x00, fldmask[12] = 0x00, fldvalue_dyna[12]:0x00 0x00
0x00 0x00
fldcontrol[12].inuse = 0x0 fldcontrol[12].refcnt = 0x00 0x00 0x00
0x00
fldoffset[13] = 0x00, fldmask[13] = 0x00, fldvalue_dyna[13]:0x00 0x00
0x00 0x00
fldcontrol[13].inuse = 0x0 fldcontrol[13].refcnt = 0x00 0x00 0x00
0x00
fldoffset[14] = 0x00, fldmask[14] = 0x00, fldvalue_dyna[14]:0x00 0x00
0x00 0x00
fldcontrol[14].inuse = 0x0 fldcontrol[14].refcnt = 0x00 0x00 0x00
0x00
fldoffset[15] = 0x00, fldmask[15] = 0x00, fldvalue_dyna[15]:0x00 0x00
0x00 0x00
fldcontrol[15].inuse = 0x0 fldcontrol[15].refcnt = 0x00 0x00 0x00
0x00
fldoffset[16] = 0x00, fldmask[16] = 0x00, fldvalue_dyna[16]:0x00 0x00
0x00 0x00
fldcontrol[16].inuse = 0x0 fldcontrol[16].refcnt = 0x00 0x00 0x00
0x00
```

```
fldoffset[17] = 0x00, fldmask[17] = 0x00, fldvalue_dyna[17]:0x00 0x00  
0x00 0x00  
fldcontrol[17].inuse = 0x0 fldcontrol[17].refcnt = 0x00 0x00 0x00  
0x00  
fldoffset[18] = 0x00, fldmask[18] = 0x00, fldvalue_dyna[18]:0x00 0x00  
0x00 0x00  
fldcontrol[18].inuse = 0x0 fldcontrol[18].refcnt = 0x00 0x00 0x00  
0x00  
fldoffset[19] = 0x00, fldmask[19] = 0x00, fldvalue_dyna[19]:0x00 0x00  
0x00 0x00  
fldcontrol[19].inuse = 0x0 fldcontrol[19].refcnt = 0x00 0x00 0x00  
0x00
```

Real fields:

```
fldoffset RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,  
0x00000000
```

```
fldmask RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,  
0x00000000
```

```
fld value4 RAM:
```

```
0x00000000
```

```
0x00000000
```

```
0x00000000
```

```
0x00000000
```

```
0x00000000
```

```
0x00000000
```

```
0x00000000
```

```
0x00000000
```

```
0x00000000
```

```
0x00000000
```

```
0x00000000
```

```
0x00000000
```

```
0x00000000
```

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0x00000000
```

```
0x00000000
```

```
0x00000000
```

```
0x00000000
```

```
0x00000000
```

```
0x00000000
```

```
0x00000000
```

```
Field dirty indicator: 0x00000000
```

```
FDB reference count fdb: 0 [0 0 0 0 ]
```

```
FDB reference count fdb: 1 [0 0 0 0 ]
```

```
FDB reference count fdb: 2 [0 0 0 0 ]
```

```
FDB reference count fdb: 3 [0 0 0 0 ]
```

```
FDB reference count fdb: 4 [0 0 0 0 ]
```

```
FDB reference count fdb: 5 [0 0 0 0 ]
```

```
FDB reference count fdb: 6 [0 0 0 0 ]
```

```
FDB reference count fdb: 7 [0 0 0 0 ]
```

```
FDB reference count fdb: 8 [0 0 0 0 ]
```

```
FDB reference count fdb: 9 [0 0 0 0 ]
```

```
FDB reference count fdb: 10 [0 0 0 0 ]
```

```
FDB reference count fdb: 11 [0 0 0 0 ]
```

FDB reference count fdb: 12 [0 0 0 0]
FDB reference count fdb: 13 [0 0 0 0]
FDB reference count fdb: 14 [0 0 0 0]
FDB reference count fdb: 15 [0 0 0 0]
FDB reference count fdb: 16 [0 0 0 0]
FDB reference count fdb: 17 [0 0 0 0]
FDB reference count fdb: 18 [0 0 0 0]
FDB reference count fdb: 19 [0 0 0 0]

Filter counters:

Filter counter 0: 0 (MIRROR1)
Filter counter 1: 0 (MIRROR2)
Filter counter 2: 0 (MIRROR3)
Filter counter 3: 0 (MIRROR4)
Filter counter 4: 0 (AEPORT_NON_MIRR_DROP)
Filter counter 5: 0 (ZONING TRAP)
Filter counter 6: 0 (FCR_EXPORT_DC)
Filter counter 7: 0 (TIN TRAP)
Filter counter 8: 0 (FICON CUP)
Filter counter 9: 0 (FICON CUP DST)
Filter counter 10: 0 (WELL KNOWN ADDR)
Filter counter 11: 0 (SIM)
Filter counter 12: 0 (UNUSED)
Filter counter 13: 0 (UNUSED)
Filter counter 14: 0 (UNUSED)
Filter counter 15: 0 (UNUSED)
Filter counter 16: 0 (PERF1)
Filter counter 17: 0 (PERF2)
Filter counter 18: 0 (PERF3)
Filter counter 19: 0 (PERF4)
Filter counter 20: 0 (PERF5)
Filter counter 21: 0 (PERF6)
Filter counter 22: 0 (PERF7)
Filter counter 23: 0 (PERF8)
Filter counter 24: 0 (PERF9)
Filter counter 25: 0 (PERF10)
Filter counter 26: 0 (PERF11)
Filter counter 27: 0 (PERF12)
Filter counter 28: 0 (OPM1)
Filter counter 29: 0 (OPM2)
Filter counter 30: 0 (IPM1)
Filter counter 31: 0 (IPM2)

ACL DATA

Logical port 8: Hard Zoning disabled, Soft Zoning disabled
Zone type: WWN Zoning
Frames with hard zone miss: 0

*** Please use filterportshow on user port 56 to display ACL hash tables and Mirroring resources of thischip.

***We show this data only for the first physical port which is an external port.

portFcPortCmdShow --slot 0 49 3
doing portFcPortCmdShow: arg1 = 3, arg2 = -2

portshow 49
portDisableReason: None
portCFlags: 0x0
portFlags: 0x4021 PRESENT U_PORT DISABLED LED
LocalSwcFlags: 0x0
portType: 26.0
POD Port: Need license to enable the port
portState: 2 Offline
Protocol: FC
portPhys: 2 No_Module portScn: 2 Offline
port generation number: 0
state transition count: 0

portId: 013100
portIfId: 4302000b
portWwn: 20:31:d8:1f:cc:2c:99:90
portWwn of device(s) connected:
16b Area list:
Distance: normal
portSpeed: N32Gbps

FEC: Inactive
Credit Recovery: Inactive
LE domain: 0
Peer beacon: Off
FC Fastwrite: OFF

| | | | | |
|-------------|---|---------------|---|-------|
| Interrupts: | 0 | Link_failure: | 0 | Frjt: |
| 0 | | | | |
| Unknown: | 0 | Loss_of_sync: | 0 | Fbsy: |
| 0 | | | | |
| Lli: | 0 | Loss_of_sig: | 0 | |
| Proc_rqrd: | 0 | Protocol_err: | 0 | |
| Timed_out: | 0 | Invalid_word: | 0 | |
| Tx_unavail: | 0 | Invalid_crc: | 0 | |
| Delim_err: | 0 | Address_err: | 0 | |
| Lr_in: | 0 | 0ls_in: | 0 | |
| Lr_out: | 0 | 0ls_out: | 0 | |

portloginshow 49
Type PID World Wide Name credit df_sz cos
=====

portloginshow 49 -history
Type PID World Wide Name logout time
=====

portregshow 49

LED registers

=====

| | | |
|---------------------------|----------|-------------|
| 0x81c5a000: c4_led_status | 00000000 | 0x81c5a004: |
| c4_led_ctl | 00000000 | |

FPL registers

=====

| | | |
|---------------------------------|----------|-------------|
| 0x81c58200: fpl_port_config | 23490000 | |
| 0x81c5820c: fpl_port_id_ctl | 00000000 | 0x81c58210: |
| fpl_port_id_addr | 00013100 | |
| 0x81c58214: fpl_port_speed | 00000004 | 0x81c5821c: |
| fpl_lli_ctl | 00000903 | |
| 0x81c58228: fpl_lli_os_ctl | bc95b5b5 | 0x81c5822c: |
| fpl_lli_send_word | bc95b5b5 | |
| 0x81c58230: fpl_lli_mark_rx | 00000000 | 0x81c58234: |
| fpl_lli_rnd_trip_time | 00000000 | |
| 0x81c58238: fpl_lli_ns_status | 80070007 | 0x81c5823c: |
| fpl_lli_intr_status | 80070007 | |
| 0x81c58244: fpl_lli_def | 00000000 | 0x81c58254: |
| fpl_lli_intr_enable_clr | 00100000 | |
| 0x81c58258: fpl_err_intr_status | 00000000 | 0x81c58260: |
| fpl_err_intr_enable_clr | 00000000 | |
| 0x81c58268: fpl_err_first_error | 00000000 | 0x81c5826c: |
| fpl_speed_neg_ctl | 00000000 | |
| 0x81c58270: fpl_speed_neg_stat | 00000000 | 0x81c58274: |
| fpl_softasn_ctl | 0000000f | |
| 0x81c58278: fpl_link_init_ctl | 00000000 | 0x81c5827c: |
| fpl_link_init_stat | 00000000 | |
| 0x81c58280: fpl_aec_ctl | 00051060 | 0x81c58284: |
| fpl_aec_ctl2 | 04009f60 | |
| 0x81c58288: fpl_pcs_ctl | 00000160 | 0x81c5828c: |
| fpl_fec_ctl | 00000441 | |
| 0x81c58290: fpl_fec_cor | 00000000 | 0x81c58294: |
| fpl_fec_uncor | 00000000 | |
| 0x81c58298: fpl_hss_link_ctl | 0031f040 | 0x81c5829c: |
| fpl_afifo_link_ctl | 00000a86 | |
| 0x81c582a0: fpl_echo_lb_ctl | 0000028c | 0x81c582a4: |
| fpl_scratch | 00000121 | |
| 0x81c582a8: fpl_debug | 00030005 | 0x81c582ac: |
| fpl_misc_debug | 00001800 | |
| 0x00000000: SW_shadow_reg | 00000000 | 0x00000000: |
| SW_c4_phyp->cfgptr | 00030000 | |

per-fpg (per octet) registers

=====

| | | |
|-------------------------------------|----------|-------------|
| 0x8180b82c: fpg_serdes_ctla0 | 81a37be7 | 0x8180b830: |
| fpg_serdes_ctla1 | 81a37be7 | |
| 0x8180b834: fpg_serdes_ctlb0 | 81a1c3c3 | 0x8180b838: |
| fpg_serdes_ctlb1 | 81a1c3c3 | |
| 0x8180b83c: fpg_serdes_xgmii_1ms | 00067c28 | 0x8180b840: |
| fpg_serdes_regtimctl | 40e47946 | |
| 0x8180b844: fpg_serdes_asnrsttimctl | 00000102 | |

HSS PLL registers

```

=====
0x81809400: 00_hssplla_vco_coarse_cal0      00000000      0x81809404:
01_hssplla_vco_coarse_cal1      00000014
0x81809408: 02_hssplla_vco_coarse_cal2      00000000      0x8180940c:
03_hssplla_vco_coarse_cal3      00000000
0x81809410: 04_hssplla_vco_coarse_cal4      00000000      0x81809424:
09_hssplla_power_ctl      00000000
0x81809428: 0A_hssplla_charge_pump_ctl      00000004      0x81809438:
0E_hssplla_pll_misc_ctl      00000000
0x8180943c: 0F_hssplla_pclk_ctl      000000f8      0x81809440:
10_hssplla_eyem_intv_ctl      00000000
0x81809444: 11_hssplla_eyem_intv_lim1      00000000      0x81809448:
12_hssplla_eyem_intv_lim2      00000000
0x8180944c: 13_hssplla_eyem_intv_lim3      00000000      0x81809450:
14_hssplla_eyem_intv_lim4      00000000
0x818094f0: 3C_hssplla_macro_tst_ctl4      00000000      0x818094f4:
3D_hssplla_macro_tst_ctl3      00000000
0x818094f8: 3E_hssplla_macro_tst_ctl2      00000000      0x818094fc:
3F_hssplla_macro_tst_ctl1      00000000
0x81809500: 00_hssppll_vco_coarse_cal0      0000000a      0x81809504:
01_hssppll_vco_coarse_cal1      00000014
0x81809508: 02_hssppll_vco_coarse_cal2      00000000      0x8180950c:
03_hssppll_vco_coarse_cal3      00000000
0x81809510: 04_hssppll_vco_coarse_cal4      00000000      0x81809524:
09_hssppll_power_ctl      00000000
0x81809528: 0A_hssppll_charge_pump_ctl      00000004      0x81809538:
0E_hssppll_pll_misc_ctl      00000000
0x8180953c: 0F_hssppll_pclk_ctl      000000f8      0x81809540:
10_hssppll_eyem_intv_ctl      00000000
0x81809544: 11_hssppll_eyem_intv_lim1      00000000      0x81809548:
12_hssppll_eyem_intv_lim2      00000000
0x8180954c: 13_hssppll_eyem_intv_lim3      00000000      0x81809550:
14_hssppll_eyem_intv_lim4      00000000
0x818095f0: 3C_hssppll_macro_tst_ctl4      00000000      0x818095f4:
3D_hssppll_macro_tst_ctl3      00000000
0x818095f8: 3E_hssppll_macro_tst_ctl2      00000000      0x818095fc:
3F_hssppll_macro_tst_ctl1      00000000

```

HSS TX registers

```

=====
0x81808500: 00_hsstx_cfg_mode_PHY      00009f48      0x81808504:
01_hsstx_test_ctl      00000000
0x81808508: 02_hsstx_coeff_ctl_INV      00000000      0x8180850c:
03_hsstx_drv_mode_ctl      00000000
0x81808510: 04_hsstx_drv_ovrd_ctl      00000010      0x81808514:
05_hsstx_dclk_align_ovrd      00000080
0x81808518: 06_hsstx_imp_cal_ovrd      00000c0c      0x8180851c:
07_hsstx_dclk_drift_tol      00000004
0x81808520: 08_hsstx_tap0_coeff_TUNE      00000000      0x81808524:
09_hsstx_tap1_coeff_TUNE      00000003
0x81808528: 0A_hsstx_tap2_coeff_TUNE      00000018      0x8180852c:
0B_hsstx_tap3_coeff_TUNE      0000000d
0x81808534: 0D_hsstx_pol_INV      0000000a      0x81808538:
0E_hsstx_ae_cmd      00000000

```

| | | |
|---|----------|-------------|
| 0x8180853c: 0F_hsstx_ae_stat | 00000000 | 0x81808540: |
| 10_hsstx_ae_tap0_TUNE | 00000000 | |
| 0x81808544: 11_hsstx_ae_tap1_TUNE | 00000000 | 0x81808548: |
| 12_hsstx_ae_tap2_TUNE | 00000028 | |
| 0x8180854c: 13_hsstx_ae_tap3_TUNE | 00000000 | 0x81808554: |
| 15_hsstx_app_tune | 0000120e | |
| 0x81808558: 16_hsstx_analog_diag | 00000000 | 0x81808560: |
| 18_hsstx_4x_seg_app | 0000aafa | |
| 0x81808564: 19_hsstx_2x_seg_app | 00000000 | 0x81808568: |
| 1A_hsstx_1x_seg_app | 0000ff5d | |
| 0x8180856c: 1B_hsstx_seg_4x_term_app | 00000000 | 0x81808570: |
| 1C_hsstx_seg_2x1x_term_app | 00000f00 | |
| 0x81808574: 1D_hsstx_tap_sign_app | 0000000a | 0x81808578: |
| 1E_hsstx_ext_addr_data | 00000001 | |
| 0x8180857c: 1F_hsstx_ext_addr_addr | 00000000 | 0x81808580: |
| 20_hsstx_pat_buf_bytes_1_0 | 00000000 | |
| 0x81808584: 21_hsstx_pat_buf_bytes_3_2 | 00000000 | 0x81808588: |
| 22_hsstx_pat_buf_bytes_5_4 | 00000000 | |
| 0x8180858c: 23_hsstx_pat_buf_bytes_7_6 | 00000000 | 0x8180859c: |
| 27_hsstx_8023az_ctl | 00000000 | |
| 0x818085a0: 28_hsstx_dcc_ctl | 000060c0 | 0x818085a4: |
| 29_hsstx_dcc_ovrd | 00000000 | |
| 0x818085a8: 2A_hsstx_dcc_app | 00000108 | 0x818085ac: |
| 2B_hsstx_dcc_timeout | 0000ffff | |
| 0x818085c0: 30_hsstx_tap_sign_ovrd | 00000000 | 0x818085c8: |
| 32_hsstx_seg_4x_ovrd | 00000000 | |
| 0x818085cc: 33_hsstx_seg_2x_ovrd | 00000000 | 0x818085d0: |
| 34_hsstx_seg_1x_ovrd | 00000000 | |
| 0x818085d8: 36_hsstx_tap_seg_4x_term_ovrd | 00000000 | 0x818085dc: |
| 37_hsstx_tap_seg_2x_term_ovrd | 00000000 | |
| 0x818085e0: 38_hsstx_tap_seg_1x_term_ovrd | 00000000 | 0x818085ec: |
| 3B_hsstx_mac_test_ctl5 | 00000000 | |
| 0x818085f0: 3C_hsstx_mac_test_ctl4 | 00000000 | 0x818085f4: |
| 3D_hsstx_mac_test_ctl3 | 00000000 | |
| 0x818085f8: 3E_hsstx_mac_test_ctl2 | 00000000 | 0x818085fc: |
| 3F_hsstx_mac_test_ctl1 | 000000c6 | |

HSS RX registers

=====

| | | |
|---------------------------------------|----------|-------------|
| 0x81808700: 00_hssrx_cfg_mode_PHY | 00009e78 | 0x81808704: |
| 01_hssrx_test_ctl | 00000000 | |
| 0x81808708: 02_hssrx_phs_rot_ctl | 0000cb80 | 0x8180870c: |
| 03_hssrx_phs_rot_ofs_ctl | 00002610 | |
| 0x81808710: 04_hssrx_phs_rot_posn1 | 00002322 | 0x81808714: |
| 05_hssrx_phs_rot_posn2 | 0000000f | |
| 0x81808718: 06_hssrx_phs_rot_sta_ofs1 | 00000002 | 0x8180871c: |
| 07_hssrx_phs_rot_sta_ofs2 | 00000001 | |
| 0x81808720: 08_hssrx_dfe_ctl_PHY | 00002002 | 0x81808724: |
| 09_hssrx_dfe_smpl_snap1 | 00000000 | |
| 0x81808728: 0A_hssrx_dfe_smpl_snap2 | 00008000 | 0x8180872c: |
| 0B_hssrx_vga_ctl1 | 00004001 | |
| 0x81808730: 0C_hssrx_vga_ctl2 | 00007aa0 | 0x81808734: |
| 0D_hssrx_vga_ctl3 | 000009e4 | |
| 0x81808738: 0E_hssrx_pwr_mgmt_ctl | 0000001f | 0x8180873c: |

| | | | |
|--|----------------|-------------|--|
| 0F_hssrx_iqamp_ctl1 | 00000019 | | |
| 0x81808740: 10_hssrx_iqamp_ctl2 | 00000006 | 0x81808744: | |
| 11_hssrx_dacap_dacan_sel | 00000003 | | |
| 0x81808748: 12_hssrx_dacap_dacan | 0000fe00 | 0x8180874c: | |
| 13_hssrx_daca_min | 00000000 | | |
| 0x81808750: 14_hssrx_adac_ctl | 00000000 | 0x81808754: | |
| 15_hssrx_ac_cp_ctl | 000031c3 | | |
| 0x81808758: 16_hssrx_ac_cp_val | 00008053 | 0x8180875c: | |
| 17_hssrx_dfe_h1h2h3_lcl_off_ch | 00000014 | | |
| 0x81808760: 18_hssrx_dfe_h1h2h3_lcl_off_val | 00000000 | 0x81808764: | |
| 19_hssrx_peaked_intg | 000000ff | | |
| 0x81808768: 1A_hssrx_cdr_analog_sw | 0000ce00 | 0x8180876c: | |
| 1B_hssrx_peaking_amp_init_c_PHY | 00000000 | | |
| 0x81808770: 1C_hssrx_dac_dpc | 00000040 | 0x81808774: | |
| 1D_hssrx_ddc | 00000000 | | |
| 0x81808778: 1E_hssrx_int_stat_PHY | 00000c0f | 0x8180877c: | |
| 1F_hssrx_dfe_func_ctl1_PHY | 0000ffff | | |
| 0x81808780: 20_hssrx_dfe_func_ctl2_INV | 00007eff | 0x81808784: | |
| 21_hssrx_ofs_ch_dcc_qcc_idx | 00002000 | | |
| 0x81808788: 22_hssrx_dfe_ofs_val | 00000109 | 0x8180878c: | |
| 23_hssrx_h_coeff_bist | 00000401 | | |
| 0x81808790: 24_hssrx_ac_cap_bist | 00000000 | 0x81808794: | |
| 25_hssrx_max_gain_path_idx_res | 00007800 | | |
| 0x81808798: 26_hssrx_loff_ctl | 00000040 | 0x8180879c: | |
| 27_hssrx_sigdet_ctl | 00004980 | | |
| 0x818087a0: 28_hssrx_ana_ctl_sw | 00000000 | 0x818087a4: | |
| 29_hssrx_intg_dac_ofs | 0000ace5 | | |
| 0x818087a8: 2A_hssrx_eye_ctl | 00000000 | 0x818087ac: | |
| 2B_hssrx_eye_met | 00000004 | | |
| 0x818087b0: 2C_hssrx_eye_met_err_cnt | 00000000 | 0x818087b4: | |
| 2D_hssrx_eye_met_pdf_eyec | 00000000 | | |
| 0x818087b8: 2E_hssrx_eye_met_pat_len | 0000007f | 0x818087bc: | |
| 2F_hssrx_dfe_func_ctl3 | 0000dfff | | |
| 0x818087c0: 30_hssrx_dfe_tap_ctl_idx_ptr | 00000008 | 0x818087c4: | |
| 31_hssrx_dfe_tap | 00003030 | | |
| 0x818087c8: 32_hssrx_lte_ctl_TUNE | 00001601 | 0x818087e4: | |
| 39_hssrx_int_stat2 | 0000c1ff | | |
| 0x818087e8: 3A_hssrx_ac_cpl_cur_src_adj | 00000043 | 0x818087ec: | |
| 3B_hssrx_dcd_ctl | 00007c53 | | |
| 0x818087f0: 3C_hssrx_dcc_ctl | 00000d00 | 0x818087f4: | |
| 3D_hssrx_qcc_ctl | 00006900 | | |
| 0x818087f8: 3E_hssrx_mac_test_ctl2 | 00000000 | 0x818087fc: | |
| 3F_hssrx_mac_test_ctl1 | 00000000 | | |
| 0x81808748: 12_hssrx_dacap_dacan[02] | 0100 fe00 | | |
| 0x81808760: 18_hssrx_dfe_h1h2h3_lcl_off_va[00] | 0000 0000 0000 | | |
| 0000 0000 0000 0000 0000 | | | |
| 0x81808760: 18_hssrx_dfe_h1h2h3_lcl_off_va[08] | 0000 0000 0000 | | |
| 0000 0000 0000 0000 0000 | | | |
| 0x81808760: 18_hssrx_dfe_h1h2h3_lcl_off_va[16] | 0000 0000 0000 | | |
| 0000 0000 | | | |
| 0x81808788: 22_hssrx_dfe_ofs_val[00][00] | 0109 007f 097f | | |
| 7f00 7d7f 0000 | | | |
| 0x81808788: 22_hssrx_dfe_ofs_val[03][00] | 037d 7f00 7b7f | | |
| 0000 7d00 0000 | | | |

```

0x81808788: 22_hssrx_dfe_ofs_val[06][00]          0a05 7f00  097b
7f7f  0379 0000
0x81808788: 22_hssrx_dfe_ofs_val[09][00]          0705 7f7f  0101
0000  057f 0000
0x81808788: 22_hssrx_dfe_ofs_val[12][00]         077d 0000  0505
0000  037e 0000
0x81808788: 22_hssrx_dfe_ofs_val[15][00]         7d7f 0000  7f05
0000  7b03 007f
0x81808788: 22_hssrx_dfe_ofs_val[18][00]         0101 0000  0107
7f7f  0003 0000
0x81808788: 22_hssrx_dfe_ofs_val[21][00]         0003 0000  0003
0000  0003 0000
0x81808788: 22_hssrx_dfe_ofs_val[24][00]         7b7e 0000  0300
7f00  7f7d 0000
0x81808794: 25_hssrx_max_gain_path_idx_res[00]    005f 0848  1007
18a8  20df 289f  308b 3800
0x81808794: 25_hssrx_max_gain_path_idx_res[08]    40af 488a  5074
5801  6040 6802  7000 7800
0x818087c4: 31_hssrx_dfe_tap[00]                   fffe 8181  0000
0000  0030 0030  3030 3030
0x818087c4: 31_hssrx_dfe_tap[08]                   3030 3030  3030
0000
0x818087e8: 3A_hssrx_ac_cpl_cur_src_adj[00]        0043 0043  0043
0043
0x818087ec: 3B_hssrx_dcd_ctl[00]                   7c53 5c00  7c00
5c00  7c00
0x818087f0: 3C_hssrx_dcc_ctl[00]                   0d00 0d00  0d41
0d00
0x818087f4: 3D_hssrx_qcc_ctl[00]                   6986 6900

```

xfipcs, fec, aec, & aet registers

=====

```

0x81c58400: xfipcs_reg          [00] 00002040 00000080 00000000
00000000  00000001 00000008 00000000 00000000
0x81c58420: xfipcs_reg          [08] 00008c01 00000000 00000000
00000000  00000000 00000000 00000000 00000000
0x81c58440: xfipcs_reg          [16] 00000000 00000000 00000000
00000000  00000040 00000000 00000000 00000000
0x81c58460: xfipcs_reg          [24] 00000000 00000000 00000000
00000000  00000000 00000000 00000000 00000000
0x81c58480: xfipcs_reg          [32] 00000004 00000000 00000000
00000000  00000000 00000000 00000000 00000000
0x81c58620: fec_32g_128g_reg    [08] 00000000 00000000 00000000
00000000  00000000 00000000 00000000
0x81c58648: fec_32g_128g_reg    [18] 00000000 00000000 00000000
00000000  00000000 00000000 00000000 00000000
0x81c58a00: aec_reg             [00] 00000000 00000000 00000000
00000000  00000000 00000000 00000000
0x81c58c00: aet_reg             [00] 00000000 00000000 00000000
00000000  00000000

```

bbc registers

=====

```

0x81c59800: bbc_trc             0      0      0      0      0      0      0

```

| | | | | | | | |
|------------------------------------|----------|---|---|---|---|----------------------|---|
| 0 | | | | | | | |
| 0x81c59840: bbc_trc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c59880: bbc_trc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c598c0: bbc_trc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c59900: bbc_trc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c59804: bbc_mbc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c59844: bbc_mbc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c59884: bbc_mbc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c598c4: bbc_mbc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c59904: bbc_mbc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c59a00: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c59a20: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c59a40: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c59a60: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c59a80: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c59c00: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c59c20: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c59c40: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c59c60: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c59c80: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c59d00: bbc_fbpc | 00000000 | | | | | 0x81c59d04: bbc_csc | |
| 00000000 | | | | | | | |
| 0x81c59d08: bbc_rcc_inc | 00000000 | | | | | 0x81c59d0c: | |
| bbc_rqc_inc | 00000000 | | | | | | |
| 0x81c59d10: bbc_fbpc_inc | 00000000 | | | | | 0x81c59d14: | |
| bbc_tmc_inc | 00000000 | | | | | | |
| 0x81c59d18: bbc_threshold | 00080100 | | | | | 0x81c59d1c: | |
| bbc_counter_clr | 00000000 | | | | | | |
| 0x81c59d20: bbc_debug_en | 00000000 | | | | | 0x81c59d24: bbc_ctrl | |
| 00200020 | | | | | | | |
| 0x81c59d28: bbc_rqc_rcc_thresh | 00000055 | | | | | 0x81c59d34: | |
| bbc_bb_sc_n | 00000000 | | | | | | |
| 0x81c59d38: bbc_crd_reco_debug | 00000000 | | | | | 0x81c59d3c: | |
| bbc_crd_reco_debug_data | 00000000 | | | | | | |
| 0x81c59d40: bbc_multi_frm_loss_cnt | 00000000 | | | | | 0x81c59d44: | |

```

bbc_multi_rdy_loss_cnt 00000000
0x81c59d48: bbc_1frm_loss_recov_cnt 00000000 0x81c59d4c:
bbc_1rdy_loss_recov_cnt 00000000
0x81c59d58: bbc_int_status 00000000 0x81c59d5c:
bbc_int_set 00000000
0x81c59d60: bbc_int_first 00000000 0x81c59d64:
bbc_frm_rdy_rx_err_addr 00000000
0x81c59d68: bbc_frm_rdy_tx_err_addr 00000000 0x81c59d6c:
bbc_trc_mbc_err_addr 00000000
0x81c59d70: bbc_frm_rdy_rx_dbl_ecc 00000000 0x81c59d74:
bbc_frm_rdy_tx_dbl_ecc 00000000
0x81c59d78: bbc_trc_mbc_dbl_ecc 00000000
0x81c59d7c: bbc_fsm_status 00001011 0x81c59d80:
bbc_force_err 00000000
0x81c59d84: bbc_crdt_avail0 ffffffff 0x81c59d88:
bbc_crdt_avail1 000000ff
0x81c59d8c: bbc_scratch 00000000

```

FPS registers

=====

```

0x81c58004: fps_er_enc_in 00000000 0x81c58008:
fps_er_crc 00000000
0x81c5800c: fps_er_trunc 00000000 0x81c58010:
fps_er_toolong 00000000
0x81c58014: fps_er_bad_eof 00000000 0x81c58018:
fps_er_enc_out 00000000
0x81c5801c: fps_er_bad_os 00000000 0x81c58020:
fps_er_flush 00000000
0x81c58024: fps_er_ifg 00000000 0x81c58038:
fps_er_crc_good_eof 00000000
0x81c5803c: fps_inv_arb 00000000 0x81c58040:
fps_slow_sts_status 00000000
0x81c58044: fps_tx_frm_cnt 00000000 0x81c58048:
fps_rx_frm_cnt 00000000
0x81c58050: fps_tx_word_cnt_hi 00000000 0x81c5804c:
fps_tx_word_cnt_lo 00000000
0x81c58058: fps_rx_word_cnt_hi 00000000 0x81c58054:
fps_rx_word_cnt_lo 00000000

```

BAL registers

=====

```

0x81c5f000: bal_desired_buf 00000000 0x81c5f004:
bal_alloc_buf 00000000
0x81c5f008: bal_busy_buf 00000000 0x81c5f00c:
bal_usable_buf 00000000
0x81c5f010: bal_max_bor_buf 00000000
0x81c5f014: bal_busy_buf_thresh 00000002

```

TXQ registers

=====

```

0x81c5b004: txq_phys_port_ctl 00430000
0x81c5b050: txq_link_skew 00000000
0x81c5b068: txq_cr_lk_dttm_intr_sts [00] 00000000 00000000
0x81c5b070: txq_cr_lk_dttm_intr_en [00] 00000000 00000000

```


0x81c5b024: txq_disc_frm_trap_cnt 00000014

FDS registers

=====

| | | |
|------------------------------------|----------|-------------|
| 0x81c5c000: fds_rxf_ctl | 00000002 | 0x81c5c004: |
| fds_rxf_wait_thresh 00000909 | | |
| 0x81c5c018: fds_rxf_first_error | 00000000 | 0x81c5c01c: |
| fds_rxf_first_error_info00000000 | | |
| 0x81c5c020: fds_rxf_inout_pkt_cnt | 00000000 | |
| 0x81c5c008: fds_rxf_err_int_status | 00000000 | 0x81c5c024: |
| fds_rxf_fifo_status 00888888 | | |
| 0x81c5d000: fds_txf_ctl | 0000003a | 0x81c5d004: |
| fds_txf_wait_ifg_thresh 00a00106 | | |
| 0x81c5d008: fds_txf_err_int_status | 00000000 | 0x81c5d024: |
| fds_txf_fifo_status 00088888 | | |
| 0x81c5d02c: fds_txf_bbc_scs | 00000000 | |

Logical TXQ registers

=====

| | | |
|------------------------------------|---------------------------------|-------------|
| 0x81c5b000: txq_log_port_ctl | 00000002 | 0x81c5b008: |
| txq_port_status 00000000 | | |
| 0x81c5b00c: txq_todo_flags | [00] 00000000 00000000 | |
| 0x81c5b014: txq_spd_match_desc | [00] 00000000 00000000 00000000 | |
| 00000000 | | |
| 0x81c5b024: txq_spd_match_desc | [04] 00000014 | |
| 0x81c5b028: txq_vc_weight | [00] 01010101 01010101 01010101 | |
| 01010101 | | |
| 0x81c5b038: txq_vc_weight | [04] 01010101 01010101 01010101 | |
| 01010101 | | |
| 0x81c5b048: txq_vc_weight | [08] 01010101 00010101 | |
| 0x81c5b054: txq_cong_dttm_ctrl | 00000000 | |
| 0x81c5b058: txq_cong_dttm_intr_sts | [00] 00000000 00000000 | |
| 0x81c5b060: txq_cong_dttm_intr_en | [00] 00000000 00000000 | |
| 0x81c5b078: txq_bw_limit_en_reg | [00] 00000000 00000000 | |
| 0x81c5b080: txq_bw_gua_en_reg | [00] 00000000 00000000 | |
| 0x81c5b088: txq_vc_group | [00] 03030300 03030303 03030303 | |
| 03030303 | | |
| 0x81c5b098: txq_vc_group | [04] 03030303 03030303 03030303 | |
| 03030303 | | |
| 0x81c5b0a8: txq_vc_group | [08] 03030303 03030303 00000000 | |
| 00000000 | | |
| 0x81c5b0b0: txq_bw_thresh_group | [00] 00000000 00000000 00000000 | |
| 00000000 | | |
| 0x81c5b0c0: txq_bw_thresh_group | [04] 00000000 00000000 00000000 | |
| 00000000 | | |
| 0x81c5b0d0: txq_bw_thresh_group | [08] 00000000 00000000 00000000 | |
| 00000000 | | |
| 0x81c5b0e0: txq_bw_thresh_group | [12] 00000000 00000000 00000000 | |
| 00000000 | | |
| 0x81c5b0f0: txq_bw_thresh_group | [16] 00000000 00000000 00000000 | |
| 00000000 | | |
| 0x81c5b100: txq_bw_thresh_group | [20] 00000000 00000000 00000000 | |
| 00000000 | | |
| 0x81c5b110: txq_bw_thresh_group | [24] 00000000 00000000 00000000 | |

```

00000000
0x81c5b120: txq_bw_thresh_group    [28] 00000000 00000000 00000000
00000000
0x81c5b130: txq_bw_thresh_group    [32] 00000000 00000000 00000000
00000000
0x81c5b140: txq_bw_thresh_group    [36] 00000000 00000000 00000000
00000000

```

txq Congestion detection Statistics RAM

```

=====
0x810906e0: vc[0]      00000000      0x810906e4: vc[1]
00000000
0x810906e8: vc[2]      00000000      0x810906ec: vc[3]
00000000
0x810906f0: vc[4]      00000000      0x810906f4: vc[5]
00000000
0x810906f8: vc[6]      00000000      0x810906fc: vc[7]
00000000
0x81090700: vc[8]      00000000      0x81090704: vc[9]
00000000
0x81090708: vc[10]     00000000      0x8109070c: vc[11]
00000000
0x81090710: vc[12]     00000000      0x81090714: vc[13]
00000000
0x81090718: vc[14]     00000000      0x8109071c: vc[15]
00000000
0x81090720: vc[16]     00000000      0x81090724: vc[17]
00000000
0x81090728: vc[18]     00000000      0x8109072c: vc[19]
00000000
0x81090730: vc[20]     00000000      0x81090734: vc[21]
00000000
0x81090738: vc[22]     00000000      0x8109073c: vc[23]
00000000
0x81090740: vc[24]     00000000      0x81090744: vc[25]
00000000
0x81090748: vc[26]     00000000      0x8109074c: vc[27]
00000000
0x81090750: vc[28]     00000000      0x81090754: vc[29]
00000000
0x81090758: vc[30]     00000000      0x8109075c: vc[31]
00000000
0x81090760: vc[32]     00000000      0x81090764: vc[33]
00000000
0x81090768: vc[34]     00000000      0x8109076c: vc[35]
00000000
0x81090770: vc[36]     00000000      0x81090774: vc[37]
00000000
0x81090778: vc[38]     00000000      0x8109077c: vc[39]
00000000

```

Logical STS registers

=====

```

0x815848c4: sts_ftb_type1_miss      00000000
0x815848c8: sts_ftb_type2_miss      00000000
0x815848cc: sts_ftb_type6_miss      00000000
0x815848d0: sts_hard_zoning_miss    00000000
0x815848d4: sts_lun_zoning_miss     00000000
0x815848dc: sts_unroutable          00000000
0x815818f4: sts_rte_cl2             00000000      0x815818f8:
sts_rte_cl3                00000000      0x815818fc: sts_rte_link_ctl
00000000                  0x815848e8: sts_tx_timeout      00000000

```

Logical STS filter registers

=====

```

0x81584840: stsflt_trig      [00] 00000000 00000000 00000000
00000000
0x81584850: stsflt_trig      [04] 00000000 00000000 00000000
00000000
0x81584860: stsflt_trig      [08] 00000000 00000000 00000000
00000000
0x81584870: stsflt_trig      [12] 00000000 00000000 00000000
00000000
0x81584880: stsflt_trig      [16] 00000000 00000000 00000000
00000000
0x81584890: stsflt_trig      [20] 00000000 00000000 00000000
00000000
0x815848a0: stsflt_trig      [24] 00000000 00000000 00000000
00000000
0x815848b0: stsflt_trig      [28] 00000000 00000000 00000000
00000000
0x815848c0: stsflt_trig      [32]

```

Logical STS discard registers

=====

```

0x81581ffc: disc_mcast_wka      00000000      0x81582000:
disc_inv_did                00000000
0x81582004: disc_cl1_cl4          00000000      0x81582008:
disc_sid_chk_fail          00000000
0x8158200c: disc_inv_dom_egid_txpt 00000000      0x81582010:
disc_vft_hop_cnt_1         00000000
0x81582014: disc_classf          00000000      0x81582018:
disc_fcp_cdb_inv           00000000
0x8158201c: disc_vfid_trap_enabled 00000000      0x81582020:
disc_vfid_hdr_chk_fail     00000000
0x81582024: disc_shim_cksum_fail    00000000      0x81582028:
disc_fed_edit_cmd_err      00000000
0x8158202c: disc_ftb_vm_mode        00000000      0x81582030:
disc_ftb_agnt2_miss        00000000
0x81582034: disc_ecb_reserved       00000000      0x81582038:
disc_ecb_de_pad_err        00000000
0x8158203c: disc_ecb_de_tag_err     00000000      0x81582040:
disc_ecb_de_seq_err        00000000
0x81582044: disc_ecb_err             00000000      0x81582048:
disc_ftb_type4_match       00000000
0x8158204c: disc_fcp_rsp_ftb_type4 00000000      0x81582050:
disc_ftb_type5_match       00000000

```

| | | |
|------------------------------------|----------|-------------|
| 0x81582054: disc_ftb_type3_match | 00000000 | 0x81582058: |
| disc_els_ftb_type3 | 00000000 | |
| 0x8158205c: disc_ftb_type1_match | 00000000 | 0x81582060: |
| disc_els_rsp_ex_port | 00000000 | |
| 0x81582064: disc_inv_drp_dps | 00000000 | 0x81582068: |
| disc_did_lookup_miss | 00000000 | |
| 0x8158206c: disc_ftb_type2_match | 00000000 | 0x81582070: |
| disc_trpd_plogi_pdisc | 00000000 | |
| 0x81582074: disc_type2_lookup_miss | 00000000 | 0x81582078: |
| disc_ftb_type6_match | 00000000 | |
| 0x8158207c: disc_els_rep_ex_port | 00000000 | 0x81582080: |
| disc_els_sid_lkup_bit1 | 00000000 | |
| 0x81582084: disc_els_sid_lkup_bit0 | 00000000 | 0x81582088: |
| disc_bls_frm_trap_bit1 | 00000000 | |
| 0x8158208c: disc_ftb_token_err | 00000000 | 0x81582090: |
| disc_asic_internal_err | 00000000 | |
| 0x81582094: disc_hard_zone_miss | 00000000 | 0x81582098: |
| disc_lun_zone_miss | 00000000 | |
| 0x8158209c: discflt_frame_disc | 00000000 | 0x815820a0: |
| discflt_parity_err | 00000000 | |
| 0x815820a4: disc_frame_marked_du | 00000000 | 0x815820a8: |
| disc_frame_marked_to | 00000000 | |
| 0x815820ac: disc_lkup_rte_prty_err | 00000000 | |

portstatsshow 49

| | | | |
|-----------------------|---|--------------------------|---|
| stat_wtx | 0 | 4-byte words transmitted | |
| stat_wrx | 0 | 4-byte words received | |
| stat_ftx | 0 | Frames transmitted | |
| stat_frx | 0 | Frames received | |
| stat_c2_frx | 0 | Class 2 frames received | |
| stat_c3_frx | 0 | Class 3 frames received | |
| stat_lc_rx | 0 | Link control frames | |
| received | | | |
| stat_mc_rx | 0 | Multicast frames | |
| received | | | |
| stat_mc_to | 0 | Multicast timeouts | |
| stat_mc_tx | 0 | Multicast frames | |
| transmitted | | | |
| tim_txcrd_z | 0 | Time TX Credit Zero | |
| (2.5Us ticks) | | | |
| tim_txcrd_z_vc 0- 3: | 0 | 0 | 0 |
| tim_txcrd_z_vc 4- 7: | 0 | 0 | 0 |
| tim_txcrd_z_vc 8-11: | 0 | 0 | 0 |
| tim_txcrd_z_vc 12-15: | 0 | 0 | 0 |
| lat_tot_pkt_vc 0- 3: | 1 | 1 | 1 |
| lat_tot_pkt_vc 4- 7: | 1 | 1 | 1 |
| lat_tot_pkt_vc 8-11: | 1 | 1 | 1 |
| lat_tot_pkt_vc 12-15: | 1 | 1 | 1 |
| lat_hi_time_vc 0- 3: | 0 | 0 | 0 |
| lat_hi_time_vc 4- 7: | 0 | 0 | 0 |
| lat_hi_time_vc 8-11: | 0 | 0 | 0 |
| lat_hi_time_vc 12-15: | 0 | 0 | 0 |
| lat_lo_time_vc 0- 3: | 1 | 1 | 1 |

| | | | | | |
|------------------------------|-----------------------------|-------------------------|---|---|--------------|
| lat_lo_time_vc | 4- 7: | 1 | 1 | 1 | 1 |
| lat_lo_time_vc | 8-11: | 1 | 1 | 1 | 1 |
| lat_lo_time_vc | 12-15: | 1 | 1 | 1 | 1 |
| max_latency_vc | 0- 3: | 1 | 1 | 1 | 1 |
| max_latency_vc | 4- 7: | 1 | 1 | 1 | 1 |
| max_latency_vc | 8-11: | 1 | 1 | 1 | 1 |
| max_latency_vc | 12-15: | 1 | 1 | 1 | 1 |
| latency_dma_ts | 09-09-2024 UTC Mon 08:47:25 | | | | TXQ |
| Latency DMA TimeStamp | | | | | |
| fec_cor_detected | 0 | Count of blocks that | | | |
| were corrected by FEC | | | | | |
| fec_uncor_detected | 0 | Count of blocks that | | | |
| were left uncorrected by FEC | | | | | |
| er_enc_in | 0 | Encoding errors inside | | | |
| of frames | | | | | |
| er_crc | 0 | Frames with CRC errors | | | |
| er_trunc | 0 | Frames shorter than | | | |
| minimum | | | | | |
| er_toolong | 0 | Frames longer than | | | |
| maximum | | | | | |
| er_bad_eof | 0 | Frames with bad end-of- | | | |
| frame | | | | | |
| er_enc_out | 0 | Encoding error outside | | | |
| of frames | | | | | |
| er_bad_os | 0 | Invalid ordered set | | | |
| er_pcs_blk | 0 | PCS block errors | | | |
| er_rx_c3_timeout | 0 | Class 3 receive frames | | | |
| discarded due to timeout | | | | | |
| er_tx_c3_timeout | 0 | Class 3 transmit frames | | | |
| discarded due to timeout | | | | | |
| er_unroutable | 0 | Frames that are | | | |
| unroutable | | | | | |
| er_unreachable | 0 | Frame with unreachable | | | |
| destination | | | | | |
| er_other_discard | 0 | Other discards | | | |
| er_type1_miss | 0 | frames with FTB type 1 | | | |
| miss | | | | | |
| er_type2_miss | 0 | frames with FTB type 2 | | | |
| miss | | | | | |
| er_type6_miss | 0 | frames with FTB type 6 | | | |
| miss | | | | | |
| er_zone_miss | 0 | frames with hard zoning | | | |
| miss | | | | | |
| er_lun_zone_miss | 0 | frames with LUN zoning | | | |
| miss | | | | | |
| er_crc_good_eof | 0 | Crc error with good eof | | | |
| er_inv_arb | 0 | Invalid ARB | | | |
| er_single_credit_loss | 0 | Single vcrdy/frame loss | | | |
| on link | | | | | |
| er_multi_credit_loss | 0 | Multiple vcrdy/frame | | | |
| loss on link | | | | | |
| other_credit_loss | 0 | Link timeout/complete | | | |
| credit loss | | | | | |
| phy_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | | | | Timestamp of |


```

stat64_rateTxFrame      0          Tx frame rate (fr/sec)
stat64_rateRxFrame      0          Rx frame rate (fr/sec)
stat64_rateTxPeakFrame  0          Tx peak frame rate (fr/sec)
stat64_rateRxPeakFrame  0          Rx peak frame rate (fr/sec)
stat64_rateTxWord       0          Tx Word rate (words/sec)
stat64_rateRxWord       0          Rx Word rate (words/sec)
stat64_rateTxPeakWord   0          Tx peak Word rate (words/sec)
stat64_rateRxPeakWord   0          Rx peak Word rate (words/sec)
stat64_PRJTFrames      0          top_int : Number of PRJT frames
returned to this port
                                0          bottom_int : Number of PRJT
frames returned to this port
stat64_PBSYFrames      0          top_int : Number of PBSY frames
returned to this port
                                0          bottom_int : Number of PBSY
frames returned to this port
stat64_inputBuffersFull 0          top_int : Number of occurrences
when all input buffers full
                                0          bottom_int : Number of
occurrences when all input buffers full
stat64_rxClass1Frames   0          top_int : Number of class 1
frames received
                                0          bottom_int : Number of class 1
frames received
stat64_aveTxFrameSize   0          Average Tx Frame size
stat64_aveRxFrameSize   0          Average Rx Frame size
Lr_in                   0          top_int
                                0          bottom_int
Ols_in                   0          top_int
                                0          bottom_int
Lr_out                   0          top_int
                                0          bottom_int
Ols_out                   0          top_int
                                0          bottom_int
Link_failure             0          top_int
                                0          bottom_int
Invalid_CRC              0          top_int
                                0          bottom_int
Invalid_word             0          top_int
                                0          bottom_int
Protocol_err            0          top_int
                                0          bottom_int
Loss_of_sig              0          top_int
                                0          bottom_int
Loss_of_sync            0          top_int
                                0          bottom_int
er_bad_os                0          top_int : Invalid ordered set
                                0          bottom_int: Invalid ordered set

```

```

portrouteshow 49
port address ID: 0x013100
external unicast routing table:
    0: Embedded

```

255: Embedded
 internal unicast routing table:
 0: Embedded

portcamshow 49

```
-----
Port  SID used  DID used  SID entries  DID entries
49    0         0        000000     000000
-----
```

ptbufshow, ptcridtshow, ptdatashow, ptstatsshow 49

```
S:
S:VF Enable:          1
S:
S:C4 Global Variable:
S:-----
```

```
-----
S:trace_stop:        0
S:
S:C4 Phy Data Pointers: c4_phyp = 0xb6ac9040
S:-----
```

```
-----
S:tnodep              0xbb837a80      pt
   0x4302800b
S:proto_phyp          0xb8807ea0      phy_cfg
0xb6aca080
S:c4_chp              0x97e28000      c4_lgcp
0x97f74000
S:c4_phy_regp         0x81c58000      proc_dir
0xb8516a00
S:-----
```

```
-----
S:magic_id            0xc4345678      num_port_timer    12
S:prev_if_id          0x4302000b      S:ftx              0
   tov              0
S:initialized          0          port_idx           11
S:ui_idx              49          slot_no
   0
S:blade_idx           11          sw_usr_ports       400
S:unused              0          intr_debounced
   0
S:aec_status          0x0          reason_code
   0
S:debug               0x00000004      debug_trc_line     0
S:rxbuf_list_head     0xffffffff      rxbuf_list_tail
0xffffffff
S:isAePort            0          port_misc_data
   0
S:num_fault1_rx_disc  0          num_fault2_rx_disc 0
S:p_ll_i_cause0       0          p_sig_regained     0
S:p_sync_regained     0          enc_out
   0x0
S:cached_fps_status   0          cached_sts_status  0
S:cached_er_crc_good_eof 0
```



```

S:cached_er_bad_os      0          cached_er_too_long      0
S:cached_er_trunc      0
cached_tot_er_crc_good_eof  0
S:num_pt_excess_intr   0          num_no_fid              0
S:num_fault1_cnt       0          num_fault2_cnt
  0
S:num_fault_lip        0          num_fault_lli          0
S:num_fault_rx_fifo    0          num_fault_hss          0
S:num_fault_bwait      0          lli_intr_prim
  0
S:num_sw_link_to       0
be_link_err_mon_count   0
S:ecb_enc_enabled      0          ecb_comp_enabled
  0
S:ecb_rsv_enc          0          ecb_rsv_comp           0
S:ecb_enc_bm           0x0        ecb_key_index
0xffffffff
S:fab_idx              4
S:num_be_lto           0          lto_count_reset_intvl
  0
S:lr_count_reset_intvl 0          num_be_lr
  0
S:num_fault_qsfp       0          check_lto
  0
S:credit_loaded        0          num_credit_overrun
  0
S:fec_enabled          0x0        fec_los_to_flag        0x0
S:phy_stats_clear_ts   1725611419 pcs_err_online
  0
S:pcs_err_light_det    0          pcs_err_ignore
  0
S:pcs_blk_err          0          pcs_hiber               0
S:phy_port_status     0          ecb_enc_lr_count
  0
S:dport_mode           0          avoid_lto_det          0
S:sn_debounced        0x0        sn_started_kr_reqd     0
S:major_timer_started  0x0        ready_bm                0x0
S:parln_1_bm           0x0        parln_0_bm              0x0
S:be_los_of_sync_event_intvl
be_los_of_sync_event   0
S:errataPtenable_cntr  0          errataPoll_cntr
  0
S:jda_rx_sig_loss_det  0          jda_rx_sig_loss_cnt
  0
S:encrypt_blk_error    0
S:
S:      c4_trunk
S:=====
S:mark_ts              0x0        deskew                  0x0
S:master_phyp          0x0
S:
S:adelay[00]: 0x00000000 0x00000000 0x00000000 0x00000000
S:adelay[04]: 0x00000000 0x00000000 0x00000000 0x00000000
S:

```

```

S:      c4_buf
S:=====
S:tx_csc          0          rx_csc
      0
S:ld_vc_credits  0          tx_flag          0x0
S:alloc_buffers  0          req_buffers      0
S:est_buffers    20         ld_use_est  0
S:bb_sc_n        0          rx_bb_sc_n
      0
S:data_cr        5          nondata_cr
      6
S:cr_enable      0
S:ld_nondata_cr  6          tnodep
0xbb837b60
S:tx_credits[0]  0  0  0  0  0  0  0  0
S:tx_credits[8]  0  0  0  0  0  0  0  0
S:tx_credits[16]  0  0  0  0  0  0  0  0  0
S:tx_credits[24]  0  0  0  0  0  0  0  0  0
S:tx_credits[32]  0  0  0  0  0  0  0  0  0
S:rx_credits[0]  0  0  0  0  0  0  0  0
S:rx_credits[8]  0  0  0  0  0  0  0  0
S:rx_credits[16]  0  0  0  0  0  0  0  0  0
S:rx_credits[24]  0  0  0  0  0  0  0  0  0
S:rx_credits[32]  0  0  0  0  0  0  0  0  0
S:tx_mbc[0]      0  0  0  0  0  0  0  0
S:tx_mbc[8]      0  0  0  0  0  0  0  0
S:tx_mbc[16]     0  0  0  0  0  0  0  0
S:tx_mbc[24]     0  0  0  0  0  0  0  0
S:tx_mbc[32]     0  0  0  0  0  0  0  0
S:rx_mbc[0]      0  0  0  0  0  0  0  0
S:rx_mbc[8]      0  0  0  0  0  0  0  0
S:rx_mbc[16]     0  0  0  0  0  0  0  0
S:rx_mbc[24]     0  0  0  0  0  0  0  0
S:rx_mbc[32]     0  0  0  0  0  0  0  0
S:
S:C4 Chip Variables: c4_phyp->c4_chp = 0x97e28000
S:-----
-----
S:version = 2.1
S:magic_id       0xc4234567  init_state      0x8
S:reset_reg_mem  0x1
S:ch_int0_en_bm  0x0          intr0_cause     0x0
S:ch_int1_en_bm  0x0          intr1_cause     0x0
S:ch_int2_en_bm  0x0          intr2_cause     0x0
S:ch             0x43010080  ch_cfg
0xb7013ba0
S:raslog_hdl.hndl 0x0          obj_halted     0x0
S:c4_chip_regp    0x80000000  c4_fpg_regp
0x81800000
S:num_chip_timer  0x5
S:hi_task_bm      0x0          lo_task_bm     0x0
S:c4_deferq.q_head 0x0          c4_deferq.q_tail 0x0
S:c4_tmrq.q_head  0x0          c4_tmrq.q_tail 0x0
slot_no          0

```

```

S:chip_inst          0          chip_idx          0
S:pll_initialized    1
pll_serdes_initialized 1
S:init_tries         0          init_ptEnableBM
0xba01b488
S:tick_polling      0xb980c9c0    sec_polling
0xb980c960
S:bb_fid            129
S:ecb_key_bm[0]     0x0          ecb_key_bm[1]     0x0
S:ecb_key_bm[2]     0x0          ecb_key_bm[3]     0x0
S:is_chip_enc_enabled
is_chip_comp_enabled 0x0
S:ftb_rsrcp->ftb_flags 0x0          act_rsrcp->act_flag 0x1
S:lue_rsrcp->lue_flags[0] 0x0          lue_rsrcp->
>lue_flags[1] 0x0
S:c4_phyp[00]: 0xb6ab0000 0xb6ab2080 0xb6ab4100 0xb6ab6180
S:c4_phyp[04]: 0xb6ab9040 0xb6abb0c0 0xb6abd140 0xb6ac0000
S:c4_phyp[08]: 0xb6ac2080 0xb6ac4100 0xb6ac6180 0xb6ac9040
S:c4_phyp[12]: 0xb6acb0c0 0xb6acd140 0xb6ad0000 0xb6ad2080
S:c4_phyp[16]: 0xb6ad4100 0xb6ad6180 0xb6ad9040 0xb6adb0c0
S:c4_phyp[20]: 0xb6add140 0xb6ae0000 0xb6ae2080 0xb6ae4100
S:c4_phyp[24]: 0xb6ae6180 0xb6ae9040 0xb6aeb0c0 0xb6aed140
S:c4_phyp[28]: 0xb6af0000 0xb6af2080 0xb6af4100 0xb6af6180
S:c4_phyp[32]: 0xb6af9040 0xb6afb0c0 0xb6afd140 0xb6b00000
S:c4_phyp[36]: 0xb6b02080 0xb6b04100 0xb6b06180 0xb6b09040
S:c4_phyp[40]: 0xb6b0b0c0 0xb6b0d140 0xb6b10000 0xb6b12080
S:c4_phyp[44]: 0xb6b14100 0xb6b16180 0xb6b19040 0xb6b1b0c0
S:c4_phyp[48]: 0xb6b1d140 0xb6b20000 0xb6b22080 0xb6b24100
S:c4_phyp[52]: 0xb6b26180 0xb6b29040 0xb6b2b0c0 0xb6b2d140
S:c4_phyp[56]: 0xb6b30000 0xb6b32080 0xb6b34100 0xb6b36180
S:c4_phyp[60]: 0xb6b39040 0xb6b3b0c0 0xb6b3d140 0xb6b40000
S:c4_lgcp[00]: 0x97f48000 0x97f4c000 0x97f50000 0x97f54000
S:c4_lgcp[04]: 0x97f58000 0x97f5c000 0x97f60000 0x97f64000
S:c4_lgcp[08]: 0x97f68000 0x97f6c000 0x97f70000 0x97f74000
S:c4_lgcp[12]: 0x97f78000 0x97f7c000 0x97f80000 0x97f84000
S:c4_lgcp[16]: 0x97f88000 0x97f8c000 0x97f90000 0x97f94000
S:c4_lgcp[20]: 0x97f98000 0x97f9c000 0x97fa0000 0x97fa4000
S:c4_lgcp[24]: 0x97fa8000 0x97fac000 0x97fb0000 0x97fb4000
S:c4_lgcp[28]: 0x97fb8000 0x97fbc000 0x97fc0000 0x97fc4000
S:c4_lgcp[32]: 0x97fc8000 0x97fcc000 0x97fd0000 0x97fd4000
S:c4_lgcp[36]: 0x97fd8000 0x97fdc000 0x97fe0000 0x97fe4000
S:c4_lgcp[40]: 0x97fe8000 0x97fec000 0x97ff0000 0x97ff4000
S:c4_lgcp[44]: 0x97ff8000 0x97ffc000 0x8e000000 0x8e004000
S:c4_lgcp[48]: 0x8e008000 0x8e00c000 0x8e010000 0x8e014000
S:c4_lgcp[52]: 0x8e018000 0x8e01c000 0x8e020000 0x8e024000
S:c4_lgcp[56]: 0x8e028000 0x8e02c000 0x8e030000 0x8e034000
S:c4_lgcp[60]: 0x8e038000 0x8e03c000 0x8e040000 0x8e044000
S:chip_timers[00]: 0xb980c720 0xb980c780 0xb980c7e0 0xb980c840
S:chip_timers[04]: 0xb980c8a0 0xb980c900
S:disc_trap_enable_required 0x0          rxlp_disc_log_stop
0x0
S:curr_rxlp_frm_cnt 0x0          curr_rxlp_disc_frm_cnt 0x0
S:sw_disc_frm_cnt   0x0          last_disc_frm_cnt     0x0
S:txq_nopop_pr_cnt 0x0          pollErrataDfe_ptBM

```

```

0xba01b4b0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][0]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][1] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][2]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][0] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][1]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][2] 0x0
S:
S:C4 Logical Port Variables
S:-----
-----
S:c4_lgc_regp      0x81c58000
S:c4_phyp:
S:      0xb6ac9040      0x0      0x0      0x0

S:      0x0      0x0      0x0      0x0

S:master_phyp      0xb6ac9040      if_id
0x4302000b
S:min_phyp      0x0      max_phyp      0x0
S:num_phy_ports      1      lgc_num      11
S:num_iu_to      0      sw_txq_bm
      0
S:port_fid      129      unused      0
S:port_group      1      lgc_stats_clear_ts
      1725611419
S:domain_tbl_sel      0      area_tbl_sel
      0
S:egid_tbl_sel      0
S:serv_lo_bm      0x0
S:
S:Proto Phy Variables:
S:-----
-----
S:magic_id      0xc4123456      asic_phyp
0xb6ac9040
S:port_id      0x4302800b      phy_cfg
      0xb6aca080
S:upsm_hdl      0xb8012d20      physm_hdl
0xb8012aa0
S:ov_snsn_hdl      0xb8012960      sw_snsn_hdl
0xb8012a00
S:ov_lksm_hdl      0xb8012b40      sw_lksm_hdl
0xb8012be0
S:trksm_hdl      0xb8012c80      lr_flag      0x0
S:lr_active      0x0      qsfm_txxr_rate_sel
      0x0
S:
S:UPSM      UP00: UPST_PORT_DISABLED      --> UP00: UPST_PORT_DISABLED
S:SNSM(OV)  SN00: OV_SNST_STOPPED      --> SN00: OV_SNST_STOPPED
S:SNSM(SW)  SW00: SW_SNST_STAGE_WS      --> SW00: SW_SNST_STAGE_WS
S:PHYSM      PP00: PHYST_STOPPED      --> PP00: PHYST_STOPPED
S:LKSM(OV)  LK00: OV_LKST_INACTIVE      --> LK00: OV_LKST_INACTIVE
S:LKSM(SW)  SW13: INACTIVE      --> SW13: INACTIVE

```

```

S:TRKSM      TRK0: TRKST_INIT      --> TRK0: TRKST_INIT
S:
S:physm variables:
S:-----
-----
S:proto_phy  0xb8807ea0      physm_hdl
0xb8012aa0
S:force_offline      0      copper      0
S:fault_reason      0: UNKNOWN
S:phy_media_present      0
S:
S:sns variables:
S:-----
-----
S:speed      0xff      proto_phy
0xb8807ea0
S:hw_sn_tries_left      0x0      sw_sn_tries_left      0x0
S:curr_txsp_count      0x0
S:tx_max      0x0      curr_tx_indx
0x0
S:curr_tx      0x0      curr_rxsp_count
0x0
S:rx_max      0x0      curr_rx_indx
0x0
S:curr_rx      0x0      rx_mem
0x0
S:rxsp_rec_count      0x0
S:nc_start      0x0      tx_start      0x0
S:sync_start      0x0      sync_present      0x0
S:diag_auto      0x0      diag_speed      0xff
S:striped_wd_tov      3000      hw_wd_tov
3000
S:step      0x0      qsf28_speed_mode
0x0
S:qsf28_mode0_hw_sn_tries_left      0x0
S:qsf28_mode1_hw_sn_tries_left      0x0
S:
S:lks variables:
S:-----
-----
S:proto_phy  0xb8807ea0      ov_lks_hdl
0xb8012b40
sw_lks_hdl      0xb8012be0
num_lf1      0
S:hw_link_tries_left      0      sw_link_tries_left      0
S:buf_ptype      0x0      stored_entry_state      0x6
S:handshake_owner      0x0      mark_unsent
0x0
S:busybuf_stuck      0x0      lr_wait      0x0
S:
S:trks variables:
S:-----
-----
S:Not a trunk port

```

```

S:
S:upsm variables:
S:-----
-----
S:proto_phyp          0xb8807ea0      upsm_hdl
0xb8012d20
S:bb_credits          0              port_beacon          0
S:port_diag_flag      0              force_offline
0
S:port_fault_rsn      0: PORT_NO_FAULT
S:retry_init_rsn      0: UNKNOWN
S:limit_reason        0              linit_result         0
S:ie_fctl_mode        0              fec_in_sync_tries_left 0
S:retry_sn_fail_init  0
retry_link_fail_init  0
S:excess_lr_count     0
S:
S:c4_ch_cfg
S:-----
-----
S:c4_desc_ring_size   256           292           256           256           292
292           2           292           292
S:thresh_def          0              16            1              0
S:intr_tries          500           cmem_pattern
0xdeadbeef
S:cmem_pattern_upwd   2              cmem_init_time      16
S:cmem_init_tries     5
S:ctrl_par_thresh     2              data_par_thresh
4
S:cam_par_thresh      4              buf_loss_thresh
12
S:crit_par_thresh     2              non_crit_par_thresh
6
S:pci_abort_thresh    10            pci_err_thresh      5
S:excess_chintr_thresh 8              sw_err_thresh       20
S:err_sample_period   300           intr_sleep
20000
S:frame_timeout       2500           proxy_dev            16384
S:vf_route            81920          qos                  2048
S:stats 2048          f_redirect         2048
S:rsp_trap            2048           lun_zoning           20480
S:area_mode           0              ftb_max_loop[0]     0
S:ftb_max_loop[1]     6              ftb_max_loop[2]     9
S:ftb_max_loop[3]     10             ftb_max_loop[4]     10
S:ftb_max_loop[5]     5              ftb_max_loop[6]     6
S:ftb_seg_size[0]     0              ftb_seg_size[1]
16384
S:ftb_seg_size[2]     65536          ftb_seg_size[3]
16384
S:ftb_seg_size[4]     16384          ftb_seg_size[5]
65536
S:ftb_seg_size[6]     16384          ftb_seg_base[0]     0
S:ftb_seg_base[1]     0              ftb_seg_base[2]
65536

```

```

S:ftb_seg_base[3]      16384      ftb_seg_base[4]
32768
S:ftb_seg_base[5]      131072     ftb_seg_base[6]
49152
asic_err_monitor_period1      300
asic_err_monitor_period2      86400
zone_chk_to_poll_period 25
zone_chk_class2_reject_tov      220
S:
S:c4_phy_cfg
S:-----
-----
S:version = 2.1
S:pt      0x4302800b      fab_ptr
0x9a800000
S:fabattr      0x9a8000d4      fab_iop
      0x9a800050
S:cfgbm      0xbb8378c4      port_ctrl
0xb6aca098
S:pcap.pcap_bm      0x8d215547      pcap.pcap2_bm
0x2588289
S:pcap.pcap3_bm      0x1bebe0c
ui_idx      49      S:slot_no
      0
is_icl      0      S:sw_usr_ports      400
S:neg_speed      0 0 0 0 0
S:my_domain      0x1      port_mode      0x0
S:hw_sn_maxtries      100      sw_sn_maxtries
      0
S:hw_link_maxtries      10      sw_link_maxtries      5
S:rx_cyc_tov      28      rttov      300
S:bufrdy_tov      300      busybuf_tov      286
S:mark_tov      300      lksm_tov      3000
S:buf_dealloc_wait      4      hw_wd_tov      3000
S:hw_lk_train_tov      540      hw_lk_test_tov
      150
S:syswait_tx_12_lips      1      lip_rx_tov      55
S:al_time_tov      15      lp_tov      2000
S:intr_tries_port      500      intr_mod_debounce
      250
S:intr_lsrflt_debounce 500      intr_efifo_debounce      100
S:port_no_fid      3      excess_ptintr_thresh      8
S:port_fault1_thresh      100      port_fault1_spur_thresh 250
S:port_fault1_disc_thresh      500
port_fault1_disc_spur_thresh 1000
S:port_fault2_thresh      5      losync_tov      100
S:port_sw_link_to      15      en_8g_scramble
      1
frc_hw_sn_mode      0x1
S:enc_poll_thresh      0      fec_enable
      0
S:fec_in_sync_to      50      fec_in_sync_try_max
      4
S:port_be_lto_threshold      100      port_be_lr_threshold

```

```

                2
S:be_cr_in_sync_to          5
port_credit_overrun_thresh          10
S:jda_sfp_losig_tov        400
jda_sfp_losig_try_max        30
S:striped_wd_tov          3000
no_sync_debounce          1200
S:
S:      fab_iop
S:=====
S:fab_iop->interop_mode 0x0          fab_iop->lab_mode          0x0
S:fab_iop->fl_bbc          0x0          fab_iop->fl_fan
          0x0
S:fab_iop->fl_cls          0x4          fab_iop->fl_rscn
          0x0
S:fab_iop->domain_id_offset 0x60          fab_iop-
>mcdt_fabric_mode          0x0
S:fab_iop->mcdt_default_zone          0x0          fab_iop-
>mcdt_safe_zone          0x0
S:
S:      port_ctrl
S:=====
S:port_ctrl.port_type      1          port_ctrl.port_grp          1
S:port_ctrl.port_number 49          port_ctrl.vc_mode          1
S:
S:      port_ctrl.lcap
S:=====
S:has_serdes              0          has_media              1
S:topology                1          skip_nego              0
S:skip_pnego              0          skip_init_event        0
S:en_shim                  0          speed_neg
          1
S:loop_back              0          num_speeds              5
S:fec_enable              0
S:
S:      port_ctrl.speed_list array
S:=====
S:speed_list[0].auto_neg  1          speed_list[0].lnk_speed  0x0000000a
S:speed_list[1].auto_neg  1          speed_list[1].lnk_speed  0x00000008
S:speed_list[2].auto_neg  1          speed_list[2].lnk_speed  0x00000006
S:speed_list[3].auto_neg  1          speed_list[3].lnk_speed  0x00000005
S:speed_list[4].auto_neg  1          speed_list[4].lnk_speed  0x00000003
S:speed_list[5].auto_neg  0          speed_list[5].lnk_speed  0x00000000
S:
S:      port_ctrl.cm
S:=====
S:port_ctrl.cm.num_vcs      8
S:port_ctrl.cm.min_bufs     8
S:port_ctrl.cm.cr_shar_bufs 0
S:port_ctrl.vc_alloc
S:port_ctrl.vc_alloc        2 0 1 1 1 1 1 1
S:port_ctrl.vc_alloc        0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.norm_vc_alloc

```



```

S:port_ctrl.norm_vc_alloc      4 0 5 5 5 5 1 1
S:port_ctrl.norm_vc_alloc      0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.cm.skip_bb_credit      0
S:port_ctrl.cm.use_shim_based_sublist      0
S:
S:      port_ctrl.serdes_set
S:=====
S:serdes_type      0x8
S:serdes_data_t.ibm_hss_serdes.tx_drive_power      0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b_sign      0x1
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b      0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_a      0x0
S:serdes_data_t.ibm_hss_serdes.rxeq      0x0
S:
S:      cfgbm
S:=====
S:old_distance      0x0      gport_lockdown      0x0
S:tport      0x1      speed      0x0
S:disable_eport      0x0      fcacc      0x0
S:lport_lockdown      0x0      priv_lport_lockdown
0x0
S:vcxlt_linit      0x0      delay_flogi      0x0
S:isl_interop      0x0      distance      0x0
S:BufStarvFlag      0x0      credit_sharing      0x0
S:lport_halfduplex      0x0      lport_fairness      0x0
S:soft_neg      0x0      asn_frc_hwretry      0x0
S:cr_recov      0x0      fport_buffers      0x0
S:export      0x0      export_mode
0x0
S:csctl_en      0x0      mirror_port      0x0
S:fault_delay      0x0      non_dfe      0x0
S:fec_configured*(0=ENAB)      0      fec_tts
0
S:port_persistently_disabled (permanently) 0 (0)
S:
S:      cfg property
S:=====
S:priv_pcfg_bm      0x00000000      lgcl_pcfg_bm
0xbb837904
S:fport_buffer      0x00000000
S:
S:
S:C4 Discard Cntrs: rxlp_stats = 0xb6ac93f0
S:-----
-----
S:disc_mcast_wka      0x0      disc_inv_did      0x0
S:disc_cl1_cl4      0x0      disc_sid_chk_fail      0x0
S:disc_inv_dom_egid_txpt      0x0      disc_vft_hop_cnt_1
0x0
S:disc_classf      0x0      disc_fcp_cdb_inv      0x0
S:disc_vfid_trap_enabled      0x0
disc_vfid_hdr_chk_fail 0x0
S:disc_shim_cksum_fail 0x0      disc_fed_edit_cmd_err 0x0

```

```

S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err 0x0
S:disc_ftb_vm_mode    0x0          disc_ftb_agnt2_miss   0x0
S:disc_ecb_de_pad_err 0x0          disc_ecb_de_tag_err   0x0
S:disc_ecb_de_seq_err 0x0          disc_ecb_err           0x0
S:disc_ftb_type4_match 0x0        disc_fcp_rsp_ftb_type4 0x0
S:disc_fcp_rsp_ftb_type4 0x0        disc_ftb_type5_match  0x0
S:disc_ftb_type3_match 0x0        disc_els_ftb_type3    0x0
S:disc_ftb_type1_match 0x0        disc_els_rsp_ex_port  0x0
S:disc_inv_drp_dps    0x0          disc_did_lookup_miss  0x0
S:disc_ftb_type2_match 0x0        disc_trpd_plogi_pdisc 0x0
S:disc_type2_lookup_miss 0x0        disc_ftb_type6_match  0x0
S:disc_els_rep_ex_port 0x0        disc_els_sid_lkup_bit1 0x0
S:disc_els_sid_lkup_bit0 0x0
disc_bls_frm_trap_bit1 0x0
S:disc_ftb_token_err 0x0          disc_asic_internal_err 0x0
S:disc_hard_zone_miss 0x0        disc_lun_zone_miss    0x0
S:discflt_frame_disc 0x0          discflt_parity_err    0x0
S:disc_frame_marked_du 0x0        disc_frame_marked_to  0x0
E:Connection type: FE
E:Port type: E_port
E:Trunk port: No
E:Configured Speed: AUTO_SPEED_NEGO
E:Max Capable Speed: 32G
E:Current SNSM Speed: UNDEFINED
E:Hardware TX Speed: 32G (0x00000004)
E:Hardware RX Speed: 32G (0x00000040)
E:
E:Interrupts: 0          Link_failure: 0
Loss_of_sync: 0          Loss_of_sig: 0
E:Lli: 0                Invalid_word: 0
E:trapped_frm: 0         fwd_status_ok: 0
E:fwd_timeout: 0         fwd_tx_unavail: 0
E:fwd_unroutable: 0      fwd_zone_out: 0
E:fwd_other_err: 0       frm_err_discard: 0
E:Fltr listA: 0          Fltr listB: 0
E:Zone trap fwd: 0       Zone trap disc: 0
E:shim_csum: 0           RTE_perr: 0
E:Invalid_crc: 0         Delim_err: 0
E:Protocol_err: 0
E:Lr_in: 0               Lr_out: 0
E:Ols_in: 0              Ols_out: 0

```

filterportshow 49

FILTER DATA

```

Shadow settings:
Filter Enable: 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000

```

Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass: 0x00000000

Real settings:

Enable RAM: 0x00000000, 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000

Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass RAM: 0x00000000

Shadowed filters:

Filter 0: Not Installed (MIRROR1)(LISTA)
c4_fldenable[0] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[0] = 0x00000000,c4_fltr_config[0] = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
c4_fldenable[1] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[1] = 0x00000000,c4_fltr_config[1] = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
c4_fldenable[2] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[2] = 0x00000000,c4_fltr_config[2] = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
c4_fldenable[3] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[3] = 0x00000000,c4_fltr_config[3] = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
c4_fldenable[4] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[4] = 0x00000000,c4_fltr_config[4] = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
c4_fldenable[5] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[5] = 0x00000000,c4_fltr_config[5] = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
c4_fldenable[6] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[6] = 0x00000000,c4_fltr_config[6] = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
c4_fldenable[7] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[7] = 0x00000000,c4_fltr_config[7] = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
c4_fldenable[8] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[8] = 0x00000000,c4_fltr_config[8] = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
c4_fldenable[9] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[9] = 0x00000000,c4_fltr_config[9] = 0x00000000

Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
c4_fldenable[10] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[10] = 0x00000000,c4_fltr_config[10] =
0x00000000
Filter 11: Not Installed (SIM)(LISTA)
c4_fldenable[11] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[11] = 0x00000000,c4_fltr_config[11] =
0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
c4_fldenable[12] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[12] = 0x00000000,c4_fltr_config[12] =
0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
c4_fldenable[13] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[13] = 0x00000000,c4_fltr_config[13] =
0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
c4_fldenable[14] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[14] = 0x00000000,c4_fltr_config[14] =
0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
c4_fldenable[15] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[15] = 0x00000000,c4_fltr_config[15] =
0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
c4_fldenable[16] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[16] = 0x00000000,c4_fltr_config[16] =
0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
c4_fldenable[17] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[17] = 0x00000000,c4_fltr_config[17] =
0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
c4_fldenable[18] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[18] = 0x00000000,c4_fltr_config[18] =
0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
c4_fldenable[19] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[19] = 0x00000000,c4_fltr_config[19] =
0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
c4_fldenable[20] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[20] = 0x00000000,c4_fltr_config[20] =

```
0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
    c4_fldenable[21] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[21] = 0x00000000,c4_fltr_config[21] =
0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
    c4_fldenable[22] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[22] = 0x00000000,c4_fltr_config[22] =
0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
    c4_fldenable[23] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[23] = 0x00000000,c4_fltr_config[23] =
0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
    c4_fldenable[24] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[24] = 0x00000000,c4_fltr_config[24] =
0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
    c4_fldenable[25] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[25] = 0x00000000,c4_fltr_config[25] =
0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
    c4_fldenable[26] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[26] = 0x00000000,c4_fltr_config[26] =
0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
    c4_fldenable[27] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[27] = 0x00000000,c4_fltr_config[27] =
0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
    c4_fldenable[28] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[28] = 0x00000000,c4_fltr_config[28] =
0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
    c4_fldenable[29] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[29] = 0x00000000,c4_fltr_config[29] =
0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    c4_fldenable[30] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[30] = 0x00000000,c4_fltr_config[30] =
0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    c4_fldenable[31] = 0x00000000 0x00000000 0x00000000
0x00000000
```

```
c4_fldnegate[31] = 0x00000000,c4_fltr_config[31] =
0x00000000
```

Real filters:

```
Filter 0: Not Installed (MIRROR1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 11: Not Installed (SIM)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
```

Filter 12: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 13: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 14: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 15: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 16: Not Installed (PERF1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 17: Not Installed (PERF2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 18: Not Installed (PERF3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 19: Not Installed (PERF4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 20: Not Installed (PERF5)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 21: Not Installed (PERF6)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 22: Not Installed (PERF7)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 23: Not Installed (PERF8)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 24: Not Installed (PERF9)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 25: Not Installed (PERF10)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,


```
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
```

```
Filter dirty indicator: 0x00000000
Performance filters: 0
Port Mirror filters: 0 (0x0)
```

FIELD DATA

Shadowed fields:

```
fldoffset[0] = 0x00, fldmask[0] = 0x00, fldvalue_dyna[0]: 0x00 0x00
0x00 0x00
fldcontrol[0].inuse = 0x0 fldcontrol[0].refcnt = 0x00 0x00 0x00
0x00
fldoffset[1] = 0x00, fldmask[1] = 0x00, fldvalue_dyna[1]: 0x00 0x00
0x00 0x00
fldcontrol[1].inuse = 0x0 fldcontrol[1].refcnt = 0x00 0x00 0x00
0x00
fldoffset[2] = 0x00, fldmask[2] = 0x00, fldvalue_dyna[2]: 0x00 0x00
0x00 0x00
fldcontrol[2].inuse = 0x0 fldcontrol[2].refcnt = 0x00 0x00 0x00
0x00
fldoffset[3] = 0x00, fldmask[3] = 0x00, fldvalue_dyna[3]: 0x00 0x00
0x00 0x00
fldcontrol[3].inuse = 0x0 fldcontrol[3].refcnt = 0x00 0x00 0x00
0x00
fldoffset[4] = 0x00, fldmask[4] = 0x00, fldvalue_dyna[4]: 0x00 0x00
```

```
0x00 0x00
fldcontrol[4].inuse = 0x0  fldcontrol[4].refcnt = 0x00 0x00 0x00
0x00
fldoffset[5] = 0x00, fldmask[5] = 0x00, fldvalue_dyna[5]:0x00 0x00
0x00 0x00
fldcontrol[5].inuse = 0x0  fldcontrol[5].refcnt = 0x00 0x00 0x00
0x00
fldoffset[6] = 0x00, fldmask[6] = 0x00, fldvalue_dyna[6]:0x00 0x00
0x00 0x00
fldcontrol[6].inuse = 0x0  fldcontrol[6].refcnt = 0x00 0x00 0x00
0x00
fldoffset[7] = 0x00, fldmask[7] = 0x00, fldvalue_dyna[7]:0x00 0x00
0x00 0x00
fldcontrol[7].inuse = 0x0  fldcontrol[7].refcnt = 0x00 0x00 0x00
0x00
fldoffset[8] = 0x00, fldmask[8] = 0x00, fldvalue_dyna[8]:0x00 0x00
0x00 0x00
fldcontrol[8].inuse = 0x0  fldcontrol[8].refcnt = 0x00 0x00 0x00
0x00
fldoffset[9] = 0x00, fldmask[9] = 0x00, fldvalue_dyna[9]:0x00 0x00
0x00 0x00
fldcontrol[9].inuse = 0x0  fldcontrol[9].refcnt = 0x00 0x00 0x00
0x00
fldoffset[10] = 0x00, fldmask[10] = 0x00, fldvalue_dyna[10]:0x00 0x00
0x00 0x00
fldcontrol[10].inuse = 0x0  fldcontrol[10].refcnt = 0x00 0x00 0x00
0x00
fldoffset[11] = 0x00, fldmask[11] = 0x00, fldvalue_dyna[11]:0x00 0x00
0x00 0x00
fldcontrol[11].inuse = 0x0  fldcontrol[11].refcnt = 0x00 0x00 0x00
0x00
fldoffset[12] = 0x00, fldmask[12] = 0x00, fldvalue_dyna[12]:0x00 0x00
0x00 0x00
fldcontrol[12].inuse = 0x0  fldcontrol[12].refcnt = 0x00 0x00 0x00
0x00
fldoffset[13] = 0x00, fldmask[13] = 0x00, fldvalue_dyna[13]:0x00 0x00
0x00 0x00
fldcontrol[13].inuse = 0x0  fldcontrol[13].refcnt = 0x00 0x00 0x00
0x00
fldoffset[14] = 0x00, fldmask[14] = 0x00, fldvalue_dyna[14]:0x00 0x00
0x00 0x00
fldcontrol[14].inuse = 0x0  fldcontrol[14].refcnt = 0x00 0x00 0x00
0x00
fldoffset[15] = 0x00, fldmask[15] = 0x00, fldvalue_dyna[15]:0x00 0x00
0x00 0x00
fldcontrol[15].inuse = 0x0  fldcontrol[15].refcnt = 0x00 0x00 0x00
0x00
fldoffset[16] = 0x00, fldmask[16] = 0x00, fldvalue_dyna[16]:0x00 0x00
0x00 0x00
fldcontrol[16].inuse = 0x0  fldcontrol[16].refcnt = 0x00 0x00 0x00
0x00
fldoffset[17] = 0x00, fldmask[17] = 0x00, fldvalue_dyna[17]:0x00 0x00
0x00 0x00
fldcontrol[17].inuse = 0x0  fldcontrol[17].refcnt = 0x00 0x00 0x00
```

```
0x00
fldoffset[18] = 0x00, fldmask[18] = 0x00, fldvalue_dyna[18]:0x00 0x00
0x00 0x00
fldcontrol[18].inuse = 0x0 fldcontrol[18].refcnt = 0x00 0x00 0x00
0x00
fldoffset[19] = 0x00, fldmask[19] = 0x00, fldvalue_dyna[19]:0x00 0x00
0x00 0x00
fldcontrol[19].inuse = 0x0 fldcontrol[19].refcnt = 0x00 0x00 0x00
0x00
```

Real fields:

```
fldoffset RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000
fldmask RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000
fld value4 RAM:
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
Field dirty indicator: 0x00000000
```

```
FDB reference count fdb: 0 [0 0 0 0 ]
FDB reference count fdb: 1 [0 0 0 0 ]
FDB reference count fdb: 2 [0 0 0 0 ]
FDB reference count fdb: 3 [0 0 0 0 ]
FDB reference count fdb: 4 [0 0 0 0 ]
FDB reference count fdb: 5 [0 0 0 0 ]
FDB reference count fdb: 6 [0 0 0 0 ]
FDB reference count fdb: 7 [0 0 0 0 ]
FDB reference count fdb: 8 [0 0 0 0 ]
FDB reference count fdb: 9 [0 0 0 0 ]
FDB reference count fdb: 10 [0 0 0 0 ]
FDB reference count fdb: 11 [0 0 0 0 ]
FDB reference count fdb: 12 [0 0 0 0 ]
FDB reference count fdb: 13 [0 0 0 0 ]
FDB reference count fdb: 14 [0 0 0 0 ]
```

FDB reference count fdb: 15 [0 0 0 0]
FDB reference count fdb: 16 [0 0 0 0]
FDB reference count fdb: 17 [0 0 0 0]
FDB reference count fdb: 18 [0 0 0 0]
FDB reference count fdb: 19 [0 0 0 0]

Filter counters:

Filter counter 0: 0 (MIRROR1)
Filter counter 1: 0 (MIRROR2)
Filter counter 2: 0 (MIRROR3)
Filter counter 3: 0 (MIRROR4)
Filter counter 4: 0 (AEPORT_NON_MIRR_DROP)
Filter counter 5: 0 (ZONING TRAP)
Filter counter 6: 0 (FCR_EXPORT_DC)
Filter counter 7: 0 (TIN TRAP)
Filter counter 8: 0 (FICON CUP)
Filter counter 9: 0 (FICON CUP DST)
Filter counter 10: 0 (WELL KNOWN ADDR)
Filter counter 11: 0 (SIM)
Filter counter 12: 0 (UNUSED)
Filter counter 13: 0 (UNUSED)
Filter counter 14: 0 (UNUSED)
Filter counter 15: 0 (UNUSED)
Filter counter 16: 0 (PERF1)
Filter counter 17: 0 (PERF2)
Filter counter 18: 0 (PERF3)
Filter counter 19: 0 (PERF4)
Filter counter 20: 0 (PERF5)
Filter counter 21: 0 (PERF6)
Filter counter 22: 0 (PERF7)
Filter counter 23: 0 (PERF8)
Filter counter 24: 0 (PERF9)
Filter counter 25: 0 (PERF10)
Filter counter 26: 0 (PERF11)
Filter counter 27: 0 (PERF12)
Filter counter 28: 0 (OPM1)
Filter counter 29: 0 (OPM2)
Filter counter 30: 0 (IPM1)
Filter counter 31: 0 (IPM2)

ACL DATA

Logical port 11: Hard Zoning disabled, Soft Zoning disabled
Zone type: WWN Zoning
Frames with hard zone miss: 0

*** Please use filterportshow on user port 56 to display ACL hash
tables and Mirroring resources of thischip.
***We show this data only for the first physical port which is an
external port.

portFcPortCmdShow --slot 0 50 3
doing portFcPortCmdShow: arg1 = 3, arg2 = -2

```

portshow 50
portDisableReason: None
portCFlags: 0x0
portFlags: 0x4021          PRESENT U_PORT DISABLED LED
LocalSwcFlags: 0x0
portType: 26.0
POD Port: Need license to enable the port
portState: 2      Offline
Protocol: FC
portPhys: 2      No_Module      portScn: 2      Offline
port generation number: 0
state transition count: 0

```

```

portId: 013200
portIfId: 43020009
portWwn: 20:32:d8:1f:cc:2c:99:90
portWwn of device(s) connected:
16b Area list:
Distance: normal
portSpeed: N32Gbps

```

```

FEC: Inactive
Credit Recovery: Inactive
LE domain: 0
Peer beacon: Off
FC Fastwrite: OFF
Interrupts: 0          Link_failure: 0          Frjt:
0
Unknown: 0          Loss_of_sync: 0          Fbsy:
0
Lli: 0          Loss_of_sig: 0
Proc_rqrd: 0          Protocol_err: 0
Timed_out: 0          Invalid_word: 0
Tx_unavail: 0          Invalid_crc: 0
Delim_err: 0          Address_err: 0
Lr_in: 0          Ols_in: 0
Lr_out: 0          Ols_out: 0

```

```

portloginshow 50
Type PID      World Wide Name      credit df_sz cos
=====

```

```

portloginshow 50 -history
Type PID      World Wide Name      logout time
=====

```

```

portregshow 50

LED registers
=====
0x81c4a000: c4_led_status      00000000      0x81c4a004:

```

c4_led_ctl 00000000

FPL registers

=====

| | | |
|---------------------------------|----------|-------------|
| 0x81c48200: fpl_port_config | 23490000 | |
| 0x81c4820c: fpl_port_id_ctl | 00000000 | 0x81c48210: |
| fpl_port_id_addr | 00013200 | |
| 0x81c48214: fpl_port_speed | 00000004 | 0x81c4821c: |
| fpl_lli_ctl | 00000903 | |
| 0x81c48228: fpl_lli_os_ctl | bc95b5b5 | 0x81c4822c: |
| fpl_lli_send_word | bc95b5b5 | |
| 0x81c48230: fpl_lli_mark_rx | 00000000 | 0x81c48234: |
| fpl_lli_rnd_trip_time | 00000000 | |
| 0x81c48238: fpl_lli_ns_status | 80070007 | 0x81c4823c: |
| fpl_lli_intr_status | 80070007 | |
| 0x81c48244: fpl_lli_def | 00000000 | 0x81c48254: |
| fpl_lli_intr_enable_clr | 00100000 | |
| 0x81c48258: fpl_err_intr_status | 00000000 | 0x81c48260: |
| fpl_err_intr_enable_clr | 00000000 | |
| 0x81c48268: fpl_err_first_error | 00000000 | 0x81c4826c: |
| fpl_speed_neg_ctl | 00000000 | |
| 0x81c48270: fpl_speed_neg_stat | 00000000 | 0x81c48274: |
| fpl_softasn_ctl | 0000000f | |
| 0x81c48278: fpl_link_init_ctl | 00000000 | 0x81c4827c: |
| fpl_link_init_stat | 00000000 | |
| 0x81c48280: fpl_aec_ctl | 00051060 | 0x81c48284: |
| fpl_aec_ctl2 | 04009f60 | |
| 0x81c48288: fpl_pcs_ctl | 00000160 | 0x81c4828c: |
| fpl_fec_ctl | 00000441 | |
| 0x81c48290: fpl_fec_cor | 00000000 | 0x81c48294: |
| fpl_fec_uncor | 00000000 | |
| 0x81c48298: fpl_hss_link_ctl | 0031f040 | 0x81c4829c: |
| fpl_afifo_link_ctl | 00000a86 | |
| 0x81c482a0: fpl_echo_lb_ctl | 0000028c | 0x81c482a4: |
| fpl_scratch | 00000121 | |
| 0x81c482a8: fpl_debug | 00030005 | 0x81c482ac: |
| fpl_misc_debug | 00001800 | |
| 0x00000000: SW_shadow_reg | 00000000 | 0x00000000: |
| SW_c4_phyp->cfgptr | 00030000 | |

per-fpg (per octet) registers

=====

| | | |
|-------------------------------------|----------|-------------|
| 0x8180b82c: fpg_serdes_ctla0 | 81a37be7 | 0x8180b830: |
| fpg_serdes_ctla1 | 81a37be7 | |
| 0x8180b834: fpg_serdes_ctlb0 | 81a1c3c3 | 0x8180b838: |
| fpg_serdes_ctlb1 | 81a1c3c3 | |
| 0x8180b83c: fpg_serdes_xgmii_1ms | 00067c28 | 0x8180b840: |
| fpg_serdes_regtimctl | 40e47946 | |
| 0x8180b844: fpg_serdes_asnrsttimctl | 00000102 | |

HSS PLL registers

=====

| | | |
|--|----------|-------------|
| 0x81809400: 00_hssplla_vco_coarse_cal0 | 00000000 | 0x81809404: |
| 01_hssplla_vco_coarse_cal1 | 00000014 | |

| | | |
|---|----------|-------------|
| 0x81809408: 02_hssplla_vco_coarse_cal2 | 00000000 | 0x8180940c: |
| 03_hssplla_vco_coarse_cal3 | 00000000 | |
| 0x81809410: 04_hssplla_vco_coarse_cal4 | 00000000 | 0x81809424: |
| 09_hssplla_power_ctl | 00000000 | |
| 0x81809428: 0A_hssplla_charge_pump_ctl | 00000004 | 0x81809438: |
| 0E_hssplla_pll_misc_ctl | 00000000 | |
| 0x8180943c: 0F_hssplla_pclk_ctl | 000000f8 | 0x81809440: |
| 10_hssplla_eyem_intv_ctl | 00000000 | |
| 0x81809444: 11_hssplla_eyem_intv_lim1 | 00000000 | 0x81809448: |
| 12_hssplla_eyem_intv_lim2 | 00000000 | |
| 0x8180944c: 13_hssplla_eyem_intv_lim3 | 00000000 | 0x81809450: |
| 14_hssplla_eyem_intv_lim4 | 00000000 | |
| 0x818094f0: 3C_hssplla_macro_tst_ctl4 | 00000000 | 0x818094f4: |
| 3D_hssplla_macro_tst_ctl3 | 00000000 | |
| 0x818094f8: 3E_hssplla_macro_tst_ctl2 | 00000000 | 0x818094fc: |
| 3F_hssplla_macro_tst_ctl1 | 00000000 | |
| 0x81809500: 00_hsspll_b_vco_coarse_cal0 | 0000000a | 0x81809504: |
| 01_hsspll_b_vco_coarse_cal1 | 00000014 | |
| 0x81809508: 02_hsspll_b_vco_coarse_cal2 | 00000000 | 0x8180950c: |
| 03_hsspll_b_vco_coarse_cal3 | 00000000 | |
| 0x81809510: 04_hsspll_b_vco_coarse_cal4 | 00000000 | 0x81809524: |
| 09_hsspll_b_power_ctl | 00000000 | |
| 0x81809528: 0A_hsspll_b_charge_pump_ctl | 00000004 | 0x81809538: |
| 0E_hsspll_b_pll_misc_ctl | 00000000 | |
| 0x8180953c: 0F_hsspll_b_pclk_ctl | 000000f8 | 0x81809540: |
| 10_hsspll_b_eyem_intv_ctl | 00000000 | |
| 0x81809544: 11_hsspll_b_eyem_intv_lim1 | 00000000 | 0x81809548: |
| 12_hsspll_b_eyem_intv_lim2 | 00000000 | |
| 0x8180954c: 13_hsspll_b_eyem_intv_lim3 | 00000000 | 0x81809550: |
| 14_hsspll_b_eyem_intv_lim4 | 00000000 | |
| 0x818095f0: 3C_hsspll_b_macro_tst_ctl4 | 00000000 | 0x818095f4: |
| 3D_hsspll_b_macro_tst_ctl3 | 00000000 | |
| 0x818095f8: 3E_hsspll_b_macro_tst_ctl2 | 00000000 | 0x818095fc: |
| 3F_hsspll_b_macro_tst_ctl1 | 00000000 | |

HSS TX registers

=====

| | | |
|--------------------------------------|----------|-------------|
| 0x81808100: 00_hsstx_cfg_mode_PHY | 00009f48 | 0x81808104: |
| 01_hsstx_test_ctl | 00000000 | |
| 0x81808108: 02_hsstx_coeff_ctl_INV | 00000000 | 0x8180810c: |
| 03_hsstx_drv_mode_ctl | 00000000 | |
| 0x81808110: 04_hsstx_drv_ovrd_ctl | 00000010 | 0x81808114: |
| 05_hsstx_dclk_align_ovrd | 00000080 | |
| 0x81808118: 06_hsstx_imp_cal_ovrd | 00000c0c | 0x8180811c: |
| 07_hsstx_dclk_drift_tol | 00000004 | |
| 0x81808120: 08_hsstx_tap0_coeff_TUNE | 00000000 | 0x81808124: |
| 09_hsstx_tap1_coeff_TUNE | 00000003 | |
| 0x81808128: 0A_hsstx_tap2_coeff_TUNE | 00000018 | 0x8180812c: |
| 0B_hsstx_tap3_coeff_TUNE | 0000000d | |
| 0x81808134: 0D_hsstx_pol_INV | 00000004 | 0x81808138: |
| 0E_hsstx_ae_cmd | 00000000 | |
| 0x8180813c: 0F_hsstx_ae_stat | 00000000 | 0x81808140: |
| 10_hsstx_ae_tap0_TUNE | 00000000 | |
| 0x81808144: 11_hsstx_ae_tap1_TUNE | 00000000 | 0x81808148: |

| | | | |
|---|----------|-------------|--|
| 12_hsstx_ae_tap2_TUNE | 00000028 | | |
| 0x8180814c: 13_hsstx_ae_tap3_TUNE | 00000000 | 0x81808154: | |
| 15_hsstx_app_tune | 0000120e | | |
| 0x81808158: 16_hsstx_analog_diag | 00000000 | 0x81808160: | |
| 18_hsstx_4x_seg_app | 0000aafa | | |
| 0x81808164: 19_hsstx_2x_seg_app | 00000000 | 0x81808168: | |
| 1A_hsstx_1x_seg_app | 0000ff5d | | |
| 0x8180816c: 1B_hsstx_seg_4x_term_app | 00000000 | 0x81808170: | |
| 1C_hsstx_seg_2x1x_term_app | 00000f00 | | |
| 0x81808174: 1D_hsstx_tap_sign_app | 00000004 | 0x81808178: | |
| 1E_hsstx_ext_addr_data | 00000001 | | |
| 0x8180817c: 1F_hsstx_ext_addr_addr | 00000000 | 0x81808180: | |
| 20_hsstx_pat_buf_bytes_1_0 | 00000000 | | |
| 0x81808184: 21_hsstx_pat_buf_bytes_3_2 | 00000000 | 0x81808188: | |
| 22_hsstx_pat_buf_bytes_5_4 | 00000000 | | |
| 0x8180818c: 23_hsstx_pat_buf_bytes_7_6 | 00000000 | 0x8180819c: | |
| 27_hsstx_8023az_ctl | 00000000 | | |
| 0x818081a0: 28_hsstx_dcc_ctl | 000060c0 | 0x818081a4: | |
| 29_hsstx_dcc_ovrd | 00001000 | | |
| 0x818081a8: 2A_hsstx_dcc_app | 00000090 | 0x818081ac: | |
| 2B_hsstx_dcc_timeout | 0000ffff | | |
| 0x818081c0: 30_hsstx_tap_sign_ovrd | 00000000 | 0x818081c8: | |
| 32_hsstx_seg_4x_ovrd | 00000000 | | |
| 0x818081cc: 33_hsstx_seg_2x_ovrd | 00000000 | 0x818081d0: | |
| 34_hsstx_seg_1x_ovrd | 00000000 | | |
| 0x818081d8: 36_hsstx_tap_seg_4x_term_ovrd | 00000000 | 0x818081dc: | |
| 37_hsstx_tap_seg_2x_term_ovrd | 00000000 | | |
| 0x818081e0: 38_hsstx_tap_seg_1x_term_ovrd | 00000000 | 0x818081ec: | |
| 3B_hsstx_mac_test_ctl5 | 00000000 | | |
| 0x818081f0: 3C_hsstx_mac_test_ctl4 | 00000000 | 0x818081f4: | |
| 3D_hsstx_mac_test_ctl3 | 00000000 | | |
| 0x818081f8: 3E_hsstx_mac_test_ctl2 | 00000000 | 0x818081fc: | |
| 3F_hsstx_mac_test_ctl1 | 000000c6 | | |

HSS RX registers

=====

| | | | |
|---------------------------------------|----------|-------------|--|
| 0x81808300: 00_hssrx_cfg_mode_PHY | 00009e78 | 0x81808304: | |
| 01_hssrx_test_ctl | 00000000 | | |
| 0x81808308: 02_hssrx_phs_rot_ctl | 0000cb80 | 0x8180830c: | |
| 03_hssrx_phs_rot_ofs_ctl | 00000610 | | |
| 0x81808310: 04_hssrx_phs_rot_posn1 | 00001d3c | 0x81808314: | |
| 05_hssrx_phs_rot_posn2 | 0000002d | | |
| 0x81808318: 06_hssrx_phs_rot_sta_ofs1 | 00000000 | 0x8180831c: | |
| 07_hssrx_phs_rot_sta_ofs2 | 0000001f | | |
| 0x81808320: 08_hssrx_dfe_ctl_PHY | 00002002 | 0x81808324: | |
| 09_hssrx_dfe_smpl_snap1 | 00000000 | | |
| 0x81808328: 0A_hssrx_dfe_smpl_snap2 | 00008000 | 0x8180832c: | |
| 0B_hssrx_vga_ctl1 | 000041d9 | | |
| 0x81808330: 0C_hssrx_vga_ctl2 | 00007aa0 | 0x81808334: | |
| 0D_hssrx_vga_ctl3 | 000009e4 | | |
| 0x81808338: 0E_hssrx_pwr_mgmt_ctl | 0000001f | 0x8180833c: | |
| 0F_hssrx_iqamp_ctl1 | 00000018 | | |
| 0x81808340: 10_hssrx_iqamp_ctl2 | 00000003 | 0x81808344: | |
| 11_hssrx_dacap_dacan_sel | 00000003 | | |

| | | |
|--|----------------|-------------|
| 0x81808348: 12_hssrx_dacap_dacan | 0000fefe | 0x8180834c: |
| 13_hssrx_daca_min | 00000000 | |
| 0x81808350: 14_hssrx_adac_ctl | 00000000 | 0x81808354: |
| 15_hssrx_ac_cp_ctl | 000031c3 | |
| 0x81808358: 16_hssrx_ac_cp_val | 0000004f | 0x8180835c: |
| 17_hssrx_dfe_h1h2h3_lcl_off_ch | 00000014 | |
| 0x81808360: 18_hssrx_dfe_h1h2h3_lcl_off_val | 00000000 | 0x81808364: |
| 19_hssrx_peaked_intg | 000000ff | |
| 0x81808368: 1A_hssrx_cdr_analog_sw | 0000ce00 | 0x8180836c: |
| 1B_hssrx_peaking_amp_init_c_PHY | 00000000 | |
| 0x81808370: 1C_hssrx_dac_dpc | 00000040 | 0x81808374: |
| 1D_hssrx_ddc | 00000000 | |
| 0x81808378: 1E_hssrx_int_stat_PHY | 00000c0f | 0x8180837c: |
| 1F_hssrx_dfe_func_ctl1_PHY | 0000ffff | |
| 0x81808380: 20_hssrx_dfe_func_ctl2_INV | 00007ebf | 0x81808384: |
| 21_hssrx_ofs_ch_dcc_qcc_idx | 00002000 | |
| 0x81808388: 22_hssrx_dfe_ofs_val | 00007f7d | 0x8180838c: |
| 23_hssrx_h_coeff_bist | 00000401 | |
| 0x81808390: 24_hssrx_ac_cap_bist | 00000000 | 0x81808394: |
| 25_hssrx_max_gain_path_idx_res | 00007800 | |
| 0x81808398: 26_hssrx_loff_ctl | 00000055 | 0x8180839c: |
| 27_hssrx_sigdet_ctl | 00002380 | |
| 0x818083a0: 28_hssrx_ana_ctl_sw | 00000000 | 0x818083a4: |
| 29_hssrx_intg_dac_ofs | 0000dcd5 | |
| 0x818083a8: 2A_hssrx_eye_ctl | 00000000 | 0x818083ac: |
| 2B_hssrx_eye_met | 00000004 | |
| 0x818083b0: 2C_hssrx_eye_met_err_cnt | 00000000 | 0x818083b4: |
| 2D_hssrx_eye_met_pdf_eyec | 00000000 | |
| 0x818083b8: 2E_hssrx_eye_met_pat_len | 0000007f | 0x818083bc: |
| 2F_hssrx_dfe_func_ctl3 | 0000dfff | |
| 0x818083c0: 30_hssrx_dfe_tap_ctl_idx_ptr | 00000008 | 0x818083c4: |
| 31_hssrx_dfe_tap | 00003030 | |
| 0x818083c8: 32_hssrx_lte_ctl_TUNE | 00001601 | 0x818083e4: |
| 39_hssrx_int_stat2 | 000041ff | |
| 0x818083e8: 3A_hssrx_ac_cpl_cur_src_adj | 00000042 | 0x818083ec: |
| 3B_hssrx_dcd_ctl | 00007c48 | |
| 0x818083f0: 3C_hssrx_dcc_ctl | 00000d41 | 0x818083f4: |
| 3D_hssrx_qcc_ctl | 00006944 | |
| 0x818083f8: 3E_hssrx_mac_test_ctl2 | 00000000 | 0x818083fc: |
| 3F_hssrx_mac_test_ctl1 | 00000000 | |
| 0x81808348: 12_hssrx_dacap_dacan[02] | 00fe fefe | |
| 0x81808360: 18_hssrx_dfe_h1h2h3_lcl_off_va[00] | 0000 0000 0000 | |
| 0000 0000 0000 0000 0000 | | |
| 0x81808360: 18_hssrx_dfe_h1h2h3_lcl_off_va[08] | 0000 0000 0000 | |
| 0000 0000 0000 0000 0000 | | |
| 0x81808360: 18_hssrx_dfe_h1h2h3_lcl_off_va[16] | 0000 0000 0000 | |
| 0000 0000 | | |
| 0x81808388: 22_hssrx_dfe_ofs_val[00][00] | 7f7d 0000 130b | |
| 7f7f 0509 7f7f | | |
| 0x81808388: 22_hssrx_dfe_ofs_val[03][00] | 7e7b 0000 0108 | |
| 007f 7e02 0000 | | |
| 0x81808388: 22_hssrx_dfe_ofs_val[06][00] | 0502 0000 057d | |
| 0000 0105 0000 | | |
| 0x81808388: 22_hssrx_dfe_ofs_val[09][00] | 7d01 0000 777c | |

```

0100 7a7d 0000
0x81808388: 22_hssrx_dfe_ofs_val[12][00] 0779 7f00 000b
7f7f 7d05 007f
0x81808388: 22_hssrx_dfe_ofs_val[15][00] 097f 0000 7d7f
0000 7f7d 0000
0x81808388: 22_hssrx_dfe_ofs_val[18][00] 037d 7f00 7b7d
0000 0079 0000
0x81808388: 22_hssrx_dfe_ofs_val[21][00] 0079 0000 0079
0000 0079 0000
0x81808388: 22_hssrx_dfe_ofs_val[24][00] 7f0a 007f 057b
7f01 0500 0000
0x81808394: 25_hssrx_max_gain_path_idx_res[00] 005f 0851 1011
1896 20d0 289a 3086 3800
0x81808394: 25_hssrx_max_gain_path_idx_res[08] 40d0 4890 507b
5800 6040 6800 70fd 7800
0x818083c4: 31_hssrx_dfe_tap[00] fffe 8080 0000
0000 0030 0030 3030 3030
0x818083c4: 31_hssrx_dfe_tap[08] 3030 3030 3030
0000
0x818083e8: 3A_hssrx_ac_cpl_cur_src_adj[00] 0042 0042 0042
0042
0x818083ec: 3B_hssrx_dcd_ctl[00] 7c48 5c00 7c81
5c00 7c00
0x818083f0: 3C_hssrx_dcc_ctl[00] 0d41 0d43 0d41
0d41
0x818083f4: 3D_hssrx_qcc_ctl[00] 694b 6944

```

xfipcs, fec, aec, & aet registers

=====

```

0x81c48400: xfipcs_reg [00] 00002040 00000080 00000000
00000000 00000001 00000008 00000000 00000000
0x81c48420: xfipcs_reg [08] 00008c01 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c48440: xfipcs_reg [16] 00000000 00000000 00000000
00000000 00000040 00000000 00000000 00000000
0x81c48460: xfipcs_reg [24] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c48480: xfipcs_reg [32] 00000004 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c48620: fec_32g_128g_reg [08] 00000000 00000000 00000000
00000000 00000000 00000000 00000000
0x81c48648: fec_32g_128g_reg [18] 00000000 00000000 00000000
00000000 00000000 00000000 00000000
0x81c48a00: aec_reg [00] 00000000 00000000 00000000
00000000 00000000 00000000 00000000
0x81c48c00: aet_reg [00] 00000000 00000000 00000000
00000000 00000000

```

bbc registers

=====

```

0x81c49800: bbc_trc 0 0 0 0 0 0 0
0
0x81c49840: bbc_trc 0 0 0 0 0 0 0
0

```

| | | | | | | | |
|---|----------|---|---|---|---|---|----------------------|
| 0x81c49880: bbc_trc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81c498c0: bbc_trc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81c49900: bbc_trc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81c49804: bbc_mbc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81c49844: bbc_mbc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81c49884: bbc_mbc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81c498c4: bbc_mbc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81c49904: bbc_mbc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81c49a00: bbc_rcc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81c49a20: bbc_rcc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81c49a40: bbc_rcc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81c49a60: bbc_rcc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81c49a80: bbc_rcc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81c49c00: bbc_rqc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81c49c20: bbc_rqc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81c49c40: bbc_rqc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81c49c60: bbc_rqc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81c49c80: bbc_rqc 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x81c49d00: bbc_fbpc 00000000 | 00000000 | | | | | | 0x81c49d04: bbc_csc |
| 0x81c49d08: bbc_rcc_inc bbc_rqc_inc 00000000 | 00000000 | | | | | | 0x81c49d0c: |
| 0x81c49d10: bbc_fbpc_inc bbc_tmc_inc 00000000 | 00000000 | | | | | | 0x81c49d14: |
| 0x81c49d18: bbc_threshold bbc_counter_clr 00000000 | 00080100 | | | | | | 0x81c49d1c: |
| 0x81c49d20: bbc_debug_en 00200020 | 00000000 | | | | | | 0x81c49d24: bbc_ctrl |
| 0x81c49d28: bbc_rqc_rcc_thresh bbc_bb_sc_n 00000000 | 00000055 | | | | | | 0x81c49d34: |
| 0x81c49d38: bbc_crd_reco_debug bbc_crd_reco_debug_data 00000000 | 00000000 | | | | | | 0x81c49d3c: |
| 0x81c49d40: bbc_multi_frm_loss_cnt bbc_multi_rdy_loss_cnt 00000000 | 00000000 | | | | | | 0x81c49d44: |
| 0x81c49d48: bbc_1frm_loss_recov_cnt bbc_1rdy_loss_recov_cnt 00000000 | 00000000 | | | | | | 0x81c49d4c: |

| | | |
|-------------------------------------|----------|-------------|
| 0x81c49d58: bbc_int_status | 00000000 | 0x81c49d5c: |
| bbc_int_set | 00000000 | |
| 0x81c49d60: bbc_int_first | 00000000 | 0x81c49d64: |
| bbc_frm_rdy_rx_err_addr | 00000000 | |
| 0x81c49d68: bbc_frm_rdy_tx_err_addr | 00000000 | 0x81c49d6c: |
| bbc_trc_mbc_err_addr | 00000000 | |
| 0x81c49d70: bbc_frm_rdy_rx_dbl_ecc | 00000000 | 0x81c49d74: |
| bbc_frm_rdy_tx_dbl_ecc | 00000000 | |
| 0x81c49d78: bbc_trc_mbc_dbl_ecc | 00000000 | |
| 0x81c49d7c: bbc_fsm_status | 00001011 | 0x81c49d80: |
| bbc_force_err | 00000000 | |
| 0x81c49d84: bbc_crdr_avail0 | ffffffff | 0x81c49d88: |
| bbc_crdr_avail1 | 000000ff | |
| 0x81c49d8c: bbc_scratch | 00000000 | |

FPS registers

=====

| | | |
|--------------------------------|----------|-------------|
| 0x81c48004: fps_er_enc_in | 00000000 | 0x81c48008: |
| fps_er_crc | 00000000 | |
| 0x81c4800c: fps_er_trunc | 00000000 | 0x81c48010: |
| fps_er_toolong | 00000000 | |
| 0x81c48014: fps_er_bad_eof | 00000000 | 0x81c48018: |
| fps_er_enc_out | 00000000 | |
| 0x81c4801c: fps_er_bad_os | 00000000 | 0x81c48020: |
| fps_er_flush | 00000000 | |
| 0x81c48024: fps_er_ifg | 00000000 | 0x81c48038: |
| fps_er_crc_good_eof | 00000000 | |
| 0x81c4803c: fps_inv_arb | 00000000 | 0x81c48040: |
| fps_slow_sts_status | 00000000 | |
| 0x81c48044: fps_tx_frm_cnt | 00000000 | 0x81c48048: |
| fps_rx_frm_cnt | 00000000 | |
| 0x81c48050: fps_tx_word_cnt_hi | 00000000 | 0x81c4804c: |
| fps_tx_word_cnt_lo | 00000000 | |
| 0x81c48058: fps_rx_word_cnt_hi | 00000000 | 0x81c48054: |
| fps_rx_word_cnt_lo | 00000000 | |

BAL registers

=====

| | | |
|---------------------------------|----------|-------------|
| 0x81c4f000: bal_desired_buf | 00000000 | 0x81c4f004: |
| bal_alloc_buf | 00000000 | |
| 0x81c4f008: bal_busy_buf | 00000000 | 0x81c4f00c: |
| bal_usable_buf | 00000000 | |
| 0x81c4f010: bal_max_bor_buf | 00000000 | |
| 0x81c4f014: bal_busy_buf_thresh | 00000002 | |

TXQ registers

=====

| | | |
|-------------------------------------|------------------------|--|
| 0x81c4b004: txq_phys_port_ctl | 00410000 | |
| 0x81c4b050: txq_link_skew | 00000000 | |
| 0x81c4b068: txq_cr_lk_dttm_intr_sts | [00] 00000000 00000000 | |
| 0x81c4b070: txq_cr_lk_dttm_intr_en | [00] 00000000 00000000 | |
| 0x81c4b024: txq_disc_frm_trap_cnt | 00000014 | |

FDS registers

```

=====
0x81c4c000: fds_rxf_ctl          00000002    0x81c4c004:
fds_rxf_wait_thresh      00000909
0x81c4c018: fds_rxf_first_error    00000000    0x81c4c01c:
fds_rxf_first_error_info00000000
0x81c4c020: fds_rxf_inout_pkt_cnt    00000000
0x81c4c008: fds_rxf_err_int_status 00000000    0x81c4c024:
fds_rxf_fifo_status      00888888
0x81c4d000: fds_txf_ctl          0000003a    0x81c4d004:
fds_txf_wait_ifg_thresh 00a00106
0x81c4d008: fds_txf_err_int_status 00000000    0x81c4d024:
fds_txf_fifo_status      00088888
0x81c4d02c: fds_txf_bbc_scs          00000000

```

Logical TXQ registers

```

=====
0x81c4b000: txq_log_port_ctl          00000002    0x81c4b008:
txq_port_status          00000000
0x81c4b00c: txq_todo_flags            [00] 00000000 00000000
0x81c4b014: txq_spd_match_desc        [00] 00000000 00000000 00000000
00000000
0x81c4b024: txq_spd_match_desc        [04] 00000014
0x81c4b028: txq_vc_weight            [00] 01010101 01010101 01010101
01010101
0x81c4b038: txq_vc_weight            [04] 01010101 01010101 01010101
01010101
0x81c4b048: txq_vc_weight            [08] 01010101 00010101
0x81c4b054: txq_cong_dttm_ctrl        00000000
0x81c4b058: txq_cong_dttm_intr_sts    [00] 00000000 00000000
0x81c4b060: txq_cong_dttm_intr_en    [00] 00000000 00000000
0x81c4b078: txq_bw_limit_en_reg       [00] 00000000 00000000
0x81c4b080: txq_bw_gua_en_reg         [00] 00000000 00000000
0x81c4b088: txq_vc_group              [00] 03030300 03030303 03030303
03030303
0x81c4b098: txq_vc_group              [04] 03030303 03030303 03030303
03030303
0x81c4b0a8: txq_vc_group              [08] 03030303 03030303 00000000
00000000
0x81c4b0b0: txq_bw_thresh_group       [00] 00000000 00000000 00000000
00000000
0x81c4b0c0: txq_bw_thresh_group       [04] 00000000 00000000 00000000
00000000
0x81c4b0d0: txq_bw_thresh_group       [08] 00000000 00000000 00000000
00000000
0x81c4b0e0: txq_bw_thresh_group       [12] 00000000 00000000 00000000
00000000
0x81c4b0f0: txq_bw_thresh_group       [16] 00000000 00000000 00000000
00000000
0x81c4b100: txq_bw_thresh_group       [20] 00000000 00000000 00000000
00000000
0x81c4b110: txq_bw_thresh_group       [24] 00000000 00000000 00000000
00000000
0x81c4b120: txq_bw_thresh_group       [28] 00000000 00000000 00000000
00000000

```

0x81c4b130: txq_bw_thresh_group [32] 00000000 00000000 00000000
00000000
0x81c4b140: txq_bw_thresh_group [36] 00000000 00000000 00000000
00000000

txq Congestion detection Statistics RAM

```
=====
0x810905a0: vc[0]          00000000          0x810905a4: vc[1]
00000000
0x810905a8: vc[2]          00000000          0x810905ac: vc[3]
00000000
0x810905b0: vc[4]          00000000          0x810905b4: vc[5]
00000000
0x810905b8: vc[6]          00000000          0x810905bc: vc[7]
00000000
0x810905c0: vc[8]          00000000          0x810905c4: vc[9]
00000000
0x810905c8: vc[10]         00000000          0x810905cc: vc[11]
00000000
0x810905d0: vc[12]         00000000          0x810905d4: vc[13]
00000000
0x810905d8: vc[14]         00000000          0x810905dc: vc[15]
00000000
0x810905e0: vc[16]         00000000          0x810905e4: vc[17]
00000000
0x810905e8: vc[18]         00000000          0x810905ec: vc[19]
00000000
0x810905f0: vc[20]         00000000          0x810905f4: vc[21]
00000000
0x810905f8: vc[22]         00000000          0x810905fc: vc[23]
00000000
0x81090600: vc[24]         00000000          0x81090604: vc[25]
00000000
0x81090608: vc[26]         00000000          0x8109060c: vc[27]
00000000
0x81090610: vc[28]         00000000          0x81090614: vc[29]
00000000
0x81090618: vc[30]         00000000          0x8109061c: vc[31]
00000000
0x81090620: vc[32]         00000000          0x81090624: vc[33]
00000000
0x81090628: vc[34]         00000000          0x8109062c: vc[35]
00000000
0x81090630: vc[36]         00000000          0x81090634: vc[37]
00000000
0x81090638: vc[38]         00000000          0x8109063c: vc[39]
00000000
```

Logical STS registers

```
=====
0x81584744: sts_ftb_type1_miss 00000000
0x81584748: sts_ftb_type2_miss 00000000
0x8158474c: sts_ftb_type6_miss 00000000
```

```

0x81584750: sts_hard_zoning_miss      00000000
0x81584754: sts_lun_zoning_miss              00000000
0x8158475c: sts_unroutable                    00000000
0x81581774: sts_rte_cl2                        00000000      0x81581778:
sts_rte_cl3                          00000000      0x8158177c: sts_rte_link_ctl
00000000      0x81584768: sts_tx_timeout          00000000

```

Logical STS filter registers

=====

```

0x815846c0: stsflt_trig [00] 00000000 00000000 00000000
00000000
0x815846d0: stsflt_trig [04] 00000000 00000000 00000000
00000000
0x815846e0: stsflt_trig [08] 00000000 00000000 00000000
00000000
0x815846f0: stsflt_trig [12] 00000000 00000000 00000000
00000000
0x81584700: stsflt_trig [16] 00000000 00000000 00000000
00000000
0x81584710: stsflt_trig [20] 00000000 00000000 00000000
00000000
0x81584720: stsflt_trig [24] 00000000 00000000 00000000
00000000
0x81584730: stsflt_trig [28] 00000000 00000000 00000000
00000000
0x81584740: stsflt_trig [32]

```

Logical STS discard registers

=====

```

0x81581d14: disc_mcast_wka      00000000      0x81581d18:
disc_inv_did          00000000
0x81581d1c: disc_cl1_cl4        00000000      0x81581d20:
disc_sid_chk_fail    00000000
0x81581d24: disc_inv_dom_egid_txpt 00000000      0x81581d28:
disc_vft_hop_cnt_1   00000000
0x81581d2c: disc_classf          00000000      0x81581d30:
disc_fcp_cdb_inv     00000000
0x81581d34: disc_vfid_trap_enabled 00000000      0x81581d38:
disc_vfid_hdr_chk_fail 00000000
0x81581d3c: disc_shim_cksum_fail  00000000      0x81581d40:
disc_fed_edit_cmd_err 00000000
0x81581d44: disc_ftb_vm_mode      00000000      0x81581d48:
disc_ftb_agnt2_miss   00000000
0x81581d4c: disc_ecb_reserved     00000000      0x81581d50:
disc_ecb_depad_err    00000000
0x81581d54: disc_ecb_de_tag_err    00000000      0x81581d58:
disc_ecb_de_seq_err   00000000
0x81581d5c: disc_ecb_err          00000000      0x81581d60:
disc_ftb_type4_match   00000000
0x81581d64: disc_fcp_rsp_ftb_type4 00000000      0x81581d68:
disc_ftb_type5_match   00000000
0x81581d6c: disc_ftb_type3_match   00000000      0x81581d70:
disc_els_ftb_type3     00000000
0x81581d74: disc_ftb_type1_match   00000000      0x81581d78:

```

```

disc_els_rsp_ex_port      00000000
0x81581d7c: disc_inv_drp_dps      00000000      0x81581d80:
disc_did_lookup_miss      00000000
0x81581d84: disc_ftb_type2_match      00000000      0x81581d88:
disc_trpd_plogi_pdisc     00000000
0x81581d8c: disc_type2_lookup_miss      00000000      0x81581d90:
disc_ftb_type6_match      00000000
0x81581d94: disc_els_rep_ex_port      00000000      0x81581d98:
disc_els_sid_lkup_bit1    00000000
0x81581d9c: disc_els_sid_lkup_bit0      00000000      0x81581da0:
disc_bls_frm_trap_bit1    00000000
0x81581da4: disc_ftb_token_err      00000000      0x81581da8:
disc_asic_internal_err    00000000
0x81581dac: disc_hard_zone_miss      00000000      0x81581db0:
disc_lun_zone_miss        00000000
0x81581db4: discflt_frame_disc      00000000      0x81581db8:
discflt_parity_err        00000000
0x81581dbc: disc_frame_marked_du      00000000      0x81581dc0:
disc_frame_marked_to      00000000
0x81581dc4: disc_lkup_rte_prty_err    00000000

```

portstatsshow 50

```

stat_wtx      0      4-byte words transmitted
stat_wrx      0      4-byte words received
stat_ftx      0      Frames transmitted
stat_frx      0      Frames received
stat_c2_frx   0      Class 2 frames received
stat_c3_frx   0      Class 3 frames received
stat_lc_rx    0      Link control frames
received
stat_mc_rx    0      Multicast frames
received
stat_mc_to    0      Multicast timeouts
stat_mc_tx    0      Multicast frames
transmitted
tim_txcrd_z   0      Time TX Credit Zero
(2.5Us ticks)
tim_txcrd_z_vc 0- 3: 0      0      0      0
tim_txcrd_z_vc 4- 7: 0      0      0      0
tim_txcrd_z_vc 8-11: 0     0      0      0
tim_txcrd_z_vc 12-15: 0    0      0      0
lat_tot_pkt_vc 0- 3: 1      1      1      1
lat_tot_pkt_vc 4- 7: 1      1      1      1
lat_tot_pkt_vc 8-11: 1     1      1      1
lat_tot_pkt_vc 12-15: 1    1      1      1
lat_hi_time_vc 0- 3: 0      0      0      0
lat_hi_time_vc 4- 7: 0      0      0      0
lat_hi_time_vc 8-11: 0     0      0      0
lat_hi_time_vc 12-15: 0    0      0      0
lat_lo_time_vc 0- 3: 1      1      1      1
lat_lo_time_vc 4- 7: 1      1      1      1
lat_lo_time_vc 8-11: 1     1      1      1
lat_lo_time_vc 12-15: 1    1      1      1

```


| | | | | |
|------------------------------|------------|---------|-------------------------|--------------|
| max_latency_vc 0- 3: | 1 | 1 | 1 | 1 |
| max_latency_vc 4- 7: | 1 | 1 | 1 | 1 |
| max_latency_vc 8-11: | 1 | 1 | 1 | 1 |
| max_latency_vc 12-15: | 1 | 1 | 1 | 1 |
| latency_dma_ts | 09-09-2024 | UTC Mon | 08:47:25 | TXQ |
| Latency DMA TimeStamp | | | | |
| fec_cor_detected | 0 | | Count of blocks that | |
| were corrected by FEC | | | | |
| fec_uncor_detected | 0 | | Count of blocks that | |
| were left uncorrected by FEC | | | | |
| er_enc_in | 0 | | Encoding errors inside | |
| of frames | | | | |
| er_crc | 0 | | Frames with CRC errors | |
| er_trunc | 0 | | Frames shorter than | |
| minimum | | | | |
| er_toolong | 0 | | Frames longer than | |
| maximum | | | | |
| er_bad_eof | 0 | | Frames with bad end-of- | |
| frame | | | | |
| er_enc_out | 0 | | Encoding error outside | |
| of frames | | | | |
| er_bad_os | 0 | | Invalid ordered set | |
| er_pcs_blk | 0 | | PCS block errors | |
| er_rx_c3_timeout | 0 | | Class 3 receive frames | |
| discarded due to timeout | | | | |
| er_tx_c3_timeout | 0 | | Class 3 transmit frames | |
| discarded due to timeout | | | | |
| er_unroutable | 0 | | Frames that are | |
| unroutable | | | | |
| er_unreachable | 0 | | Frame with unreachable | |
| destination | | | | |
| er_other_discard | 0 | | Other discards | |
| er_type1_miss | 0 | | frames with FTB type 1 | |
| miss | | | | |
| er_type2_miss | 0 | | frames with FTB type 2 | |
| miss | | | | |
| er_type6_miss | 0 | | frames with FTB type 6 | |
| miss | | | | |
| er_zone_miss | 0 | | frames with hard zoning | |
| miss | | | | |
| er_lun_zone_miss | 0 | | frames with LUN zoning | |
| miss | | | | |
| er_crc_good_eof | 0 | | Crc error with good eof | |
| er_inv_arb | 0 | | Invalid ARB | |
| er_single_credit_loss | 0 | | Single vcrdy/frame loss | |
| on link | | | | |
| er_multi_credit_loss | 0 | | Multiple vcrdy/frame | |
| loss on link | | | | |
| other_credit_loss | 0 | | Link timeout/complete | |
| credit loss | | | | |
| phy_stats_clear_ts | 09-06-2024 | UTC Fri | 08:30:19 | Timestamp of |
| phy_port stats clear | | | | |
| lgc_stats_clear_ts | 09-06-2024 | UTC Fri | 08:30:19 | Timestamp of |
| lgc_port stats clear | | | | |

```

fec_corrected_rate      0          FEC Corrected blocks per
second

portstats64show 50
stat64_wtx      0          top_int : 4-byte words transmitted
                0          bottom_int : 4-byte words transmitted
stat64_wrx      0          top_int : 4-byte words received
                0          bottom_int : 4-byte words received
stat64_ftx      0          top_int : Frames transmitted
                0          bottom_int : Frames transmitted
stat64_frx      0          top_int : Frames received
                0          bottom_int : Frames received
stat64_c2_frx   0          top_int : Class 2 frames received
                0          bottom_int : Class 2 frames received
stat64_c3_frx   0          top_int : Class 3 frames received
                0          bottom_int : Class 3 frames received
stat64_lc_rx    0          top_int : Link control frames received
                0          bottom_int : Link control frames
received
stat64_mc_rx    0          top_int : Multicast frames received
                0          bottom_int : Multicast frames received
stat64_mc_to    0          top_int : Multicast timeouts
                0          bottom_int : Multicast timeouts
stat64_mc_tx    0          top_int : Multicast frames transmitted
                0          bottom_int : Multicast frames
transmitted
tim64_rdy_pri   0          top_int : Time R_RDY high priority
                0          bottom_int : Time R_RDY high priority
tim64_txcrd_z   0          top_int : Time BB_credit zero
                0          bottom_int : Time BB_credit zero
er64_enc_in     0          top_int : Encoding errors inside of
frames
                0          bottom_int : Encoding errors inside of
frames
er64_crc        0          top_int : Frames with CRC errors
                0          bottom_int : Frames with CRC errors
er64_trunc      0          top_int : Frames shorter than minimum
                0          bottom_int : Frames shorter than minimum
er64_toolong    0          top_int : Frames longer than maximum
                0          bottom_int : Frames longer than maximum
er64_bad_eof    0          top_int : Frames with bad end-of-frame
                0          bottom_int : Frames with bad end-of-
frame
er64_enc_out    0          top_int : Encoding error outside of
frames
                0          bottom_int : Encoding error outside of
frames
er64_disc_c3    0          top_int : Class 3 frames discarded
                0          bottom_int : Class 3 frames discarded
er64_pcs_blk    0          top_int : PCS block errors
                0          bottom_int : PCS block errors
stat64_rateTxFrame      0          Tx frame rate (fr/sec)
stat64_rateRxFrame      0          Rx frame rate (fr/sec)
stat64_rateTxPeakFrame  0          Tx peak frame rate (fr/sec)

```

```

stat64_rateRxPeakFrame 0          Rx peak frame rate (fr/sec)
stat64_rateTxWord      0          Tx Word rate (words/sec)
stat64_rateRxWord      0          Rx Word rate (words/sec)
stat64_rateTxPeakWord  0          Tx peak Word rate (words/sec)
stat64_rateRxPeakWord  0          Rx peak Word rate (words/sec)
stat64_PRJTFrames      0          top_int : Number of PRJT frames
returned to this port      0          bottom_int : Number of PRJT
frames returned to this port
stat64_PBSYFrames      0          top_int : Number of PBSY frames
returned to this port      0          bottom_int : Number of PBSY
frames returned to this port
stat64_inputBuffersFull 0          top_int : Number of occurrences
when all input buffers full 0          bottom_int : Number of
occurrences when all input buffers full
stat64_rxClass1Frames  0          top_int : Number of class 1
frames received          0          bottom_int : Number of class 1
frames received
stat64_aveTxFrameSize  0          Average Tx Frame size
stat64_aveRxFrameSize  0          Average Rx Frame size
Lr_in                   0          top_int
                           0          bottom_int
Ols_in                  0          top_int
                           0          bottom_int
Lr_out                  0          top_int
                           0          bottom_int
Ols_out                 0          top_int
                           0          bottom_int
Link_failure            0          top_int
                           0          bottom_int
Invalid_CRC             0          top_int
                           0          bottom_int
Invalid_word            0          top_int
                           0          bottom_int
Protocol_err            0          top_int
                           0          bottom_int
Loss_of_sig             0          top_int
                           0          bottom_int
Loss_of_sync            0          top_int
                           0          bottom_int
er_bad_os               0          top_int : Invalid ordered set
                           0          bottom_int: Invalid ordered set

```

```

portrouteshow 50
port address ID: 0x013200
external unicast routing table:
  0: Embedded
 255: Embedded
internal unicast routing table:
  0: Embedded

```

portcamshow 50

```
-----  
Port  SID used  DID used  SID entries  DID entries  
50    0         0        000000      000000  
-----
```

ptbufshow, ptcreditshow, ptdatashow, ptstatsshow 50

S:

S:VF Enable: 1

S:

S:C4 Global Variable:

S:-----

S:trace_stop: 0

S:

S:C4 Phy Data Pointers: c4_phyp = 0xb6ac4100

S:-----

S:tnodep 0xbb835540 pt

0x43028009

S:proto_phyp 0xb88077e0 phy_cfg

0xb6ac5140

S:c4_chp 0x97e28000 c4_lgcp

0x97f6c000

S:c4_phy_regp 0x81c48000 proc_dir

0xb8515be0

S:-----

S:magic_id 0xc4345678 num_port_timer 12

S:prev_if_id 0x43020009 S:ftx 0

0

S:initialized 0 port_idx 9

S:ui_idx 50 slot_no

0

S:blade_idx 9 sw_usr_ports 400

S:unused 0 intr_debounced

0

S:aec_status 0x0 reason_code

0

S:debug 0x00000004 debug_trc_line 0

S:rxbuf_list_head 0xffffffff rxbuf_list_tail

0xffffffff

S:isAePort 0 port_misc_data

0

S:num_fault1_rx_disc 0 num_fault2_rx_disc 0

S:p_ll_i_cause0 0 p_sig_regained 0

S:p_sync_regained 0 enc_out

0x0

S:cached_fps_status 0 cached_sts_status 0

S:cached_er_crc_good_eof 0

S:cached_er_bad_os 0 cached_er_too_long 0

S:cached_er_trunc 0

cached_tot_er_crc_good_eof 0

```

S:num_pt_excess_intr      0          num_no_fid          0
S:num_fault1_cnt          0          num_fault2_cnt
0
S:num_fault_lip           0          num_fault_lli        0
S:num_fault_rx_fifo      0          num_fault_hss        0
S:num_fault_bwait        0          lli_intr_prim
0
S:num_sw_link_to         0
be_link_err_mon_count    0
S:ecb_enc_enabled        0          ecb_comp_enabled
0
S:ecb_rsv_enc            0          ecb_rsv_comp         0
S:ecb_enc_bm            0x0        ecb_key_index
0xffffffff
S:fab_idx                4
S:num_be_lto             0          lto_count_reset_intvl
0
S:lr_count_reset_intvl   0          num_be_lr
0
S:num_fault_qsfm         0          check_lto
0
S:credit_loaded          0          num_credit_overrun
0
S:fec_enabled            0x0        fec_los_to_flag      0x0
S:phy_stats_clear_ts     0          pcs_err_online
1725611419
S:pcs_err_light_det      0          pcs_err_ignore
0
S:pcs_blk_err            0          pcs_hiber             0
S:phy_port_status        0          ecb_enc_lr_count
0
S:dport_mode             0          avoid_lto_det        0
S:sn_debounced          0x0        sn_started_kr_reqd   0
S:major_timer_started    0x0        ready_bm             0x0
S:parln_1_bm            0x0        parln_0_bm          0x0
S:be_los_of_sync_event_intvl
be_los_of_sync_event    0
S:errataPtenable_cntr   0          errataPoll_cntr
0
S:jda_rx_sig_loss_det    0          jda_rx_sig_loss_cnt
0
S:encrypt_blk_error      0
S:
S:      c4_trunk
S:=====
S:mark_ts                0x0        deskew              0x0
S:master_phyp            0x0
S:
S:adelay[00]: 0x00000000 0x00000000 0x00000000 0x00000000
S:adelay[04]: 0x00000000 0x00000000 0x00000000 0x00000000
S:
S:      c4_buf
S:=====
S:tx_csc                 0          rx_csc

```

```

      0
S:ld_vc_credits      0          tx_flag          0x0
S:alloc_buffers     0          req_buffers      0
S:est_buffers       20         ld_use_est       0
S:bb_sc_n           0          rx_bb_sc_n
      0
S:data_cr            5          nondata_cr
      6
S:cr_enable         0
S:ld_nondata_cr     6          tnodep
0xbb835620
S:tx_credits[0] 0    0    0    0    0    0    0    0
S:tx_credits[8] 0    0    0    0    0    0    0    0
S:tx_credits[16]    0    0    0    0    0    0    0    0    0
S:tx_credits[24]    0    0    0    0    0    0    0    0    0
S:tx_credits[32]    0    0    0    0    0    0    0    0    0
S:rx_credits[0] 0    0    0    0    0    0    0    0
S:rx_credits[8] 0    0    0    0    0    0    0    0
S:rx_credits[16]    0    0    0    0    0    0    0    0    0
S:rx_credits[24]    0    0    0    0    0    0    0    0    0
S:rx_credits[32]    0    0    0    0    0    0    0    0    0
S:tx_mbc[0] 0    0    0    0    0    0    0    0
S:tx_mbc[8] 0    0    0    0    0    0    0    0
S:tx_mbc[16] 0    0    0    0    0    0    0    0
S:tx_mbc[24] 0    0    0    0    0    0    0    0
S:tx_mbc[32] 0    0    0    0    0    0    0    0
S:rx_mbc[0] 0    0    0    0    0    0    0    0
S:rx_mbc[8] 0    0    0    0    0    0    0    0
S:rx_mbc[16] 0    0    0    0    0    0    0    0
S:rx_mbc[24] 0    0    0    0    0    0    0    0
S:rx_mbc[32] 0    0    0    0    0    0    0    0
S:
S:C4 Chip Variables: c4_phyp->c4_chp = 0x97e28000
S:-----
-----
S:version = 2.1
S:magic_id          0xc4234567    init_state        0x8
S:reset_reg_mem    0x1
S:ch_int0_en_bm    0x0          intr0_cause       0x0
S:ch_int1_en_bm    0x0          intr1_cause       0x0
S:ch_int2_en_bm    0x0          intr2_cause       0x0
S:ch                0x43010080    ch_cfg
0xb7013ba0
S:raslog_hdl.hndl  0x0          obj_halted        0x0
S:c4_chip_regp     0x80000000    c4_fpg_regp
0x81800000
S:num_chip_timer   0x5
S:hi_task_bm       0x0          lo_task_bm        0x0
S:c4_deferq.q_head 0x0          c4_deferq.q_tail  0x0
S:c4_tmrq.q_head   0x0          c4_tmrq.q_tail    0x0
slot_no            0
S:chip_inst        0          chip_idx          0
S:pll_initialized  1
pll_serdes_initialized 1

```

```

S:init_tries          0          init_ptEnableBM
0xba01b488
S:tick_polling      0xb980c9c0      sec_polling
0xb980c960
S:bb_fid              129
S:ecb_key_bm[0]      0x0          ecb_key_bm[1]      0x0
S:ecb_key_bm[2]      0x0          ecb_key_bm[3]      0x0
S:is_chip_enc_enabled
is_chip_comp_enabled 0x0
S:ftb_rsrcp->ftb_flags 0x0          act_rsrcp->act_flag 0x1
S:lue_rsrcp->lue_flags[0] 0x0          lue_rsrcp-
>lue_flags[1] 0x0
S:c4_phyp[00]: 0xb6ab0000 0xb6ab2080 0xb6ab4100 0xb6ab6180
S:c4_phyp[04]: 0xb6ab9040 0xb6abb0c0 0xb6abd140 0xb6ac0000
S:c4_phyp[08]: 0xb6ac2080 0xb6ac4100 0xb6ac6180 0xb6ac9040
S:c4_phyp[12]: 0xb6acb0c0 0xb6acd140 0xb6ad0000 0xb6ad2080
S:c4_phyp[16]: 0xb6ad4100 0xb6ad6180 0xb6ad9040 0xb6adb0c0
S:c4_phyp[20]: 0xb6add140 0xb6ae0000 0xb6ae2080 0xb6ae4100
S:c4_phyp[24]: 0xb6ae6180 0xb6ae9040 0xb6aeb0c0 0xb6aed140
S:c4_phyp[28]: 0xb6af0000 0xb6af2080 0xb6af4100 0xb6af6180
S:c4_phyp[32]: 0xb6af9040 0xb6afb0c0 0xb6afd140 0xb6b00000
S:c4_phyp[36]: 0xb6b02080 0xb6b04100 0xb6b06180 0xb6b09040
S:c4_phyp[40]: 0xb6b0b0c0 0xb6b0d140 0xb6b10000 0xb6b12080
S:c4_phyp[44]: 0xb6b14100 0xb6b16180 0xb6b19040 0xb6b1b0c0
S:c4_phyp[48]: 0xb6b1d140 0xb6b20000 0xb6b22080 0xb6b24100
S:c4_phyp[52]: 0xb6b26180 0xb6b29040 0xb6b2b0c0 0xb6b2d140
S:c4_phyp[56]: 0xb6b30000 0xb6b32080 0xb6b34100 0xb6b36180
S:c4_phyp[60]: 0xb6b39040 0xb6b3b0c0 0xb6b3d140 0xb6b40000
S:c4_lgcp[00]: 0x97f48000 0x97f4c000 0x97f50000 0x97f54000
S:c4_lgcp[04]: 0x97f58000 0x97f5c000 0x97f60000 0x97f64000
S:c4_lgcp[08]: 0x97f68000 0x97f6c000 0x97f70000 0x97f74000
S:c4_lgcp[12]: 0x97f78000 0x97f7c000 0x97f80000 0x97f84000
S:c4_lgcp[16]: 0x97f88000 0x97f8c000 0x97f90000 0x97f94000
S:c4_lgcp[20]: 0x97f98000 0x97f9c000 0x97fa0000 0x97fa4000
S:c4_lgcp[24]: 0x97fa8000 0x97fac000 0x97fb0000 0x97fb4000
S:c4_lgcp[28]: 0x97fb8000 0x97fbc000 0x97fc0000 0x97fc4000
S:c4_lgcp[32]: 0x97fc8000 0x97fcc000 0x97fd0000 0x97fd4000
S:c4_lgcp[36]: 0x97fd8000 0x97fdc000 0x97fe0000 0x97fe4000
S:c4_lgcp[40]: 0x97fe8000 0x97fec000 0x97ff0000 0x97ff4000
S:c4_lgcp[44]: 0x97ff8000 0x97ffc000 0x8e000000 0x8e004000
S:c4_lgcp[48]: 0x8e008000 0x8e00c000 0x8e010000 0x8e014000
S:c4_lgcp[52]: 0x8e018000 0x8e01c000 0x8e020000 0x8e024000
S:c4_lgcp[56]: 0x8e028000 0x8e02c000 0x8e030000 0x8e034000
S:c4_lgcp[60]: 0x8e038000 0x8e03c000 0x8e040000 0x8e044000
S:chip_timers[00]: 0xb980c720 0xb980c780 0xb980c7e0 0xb980c840
S:chip_timers[04]: 0xb980c8a0 0xb980c900
S:disc_trap_enable_required 0x0          rxlp_disc_log_stop
0x0
S:curr_rxlp_frm_cnt 0x0          curr_rxlp_disc_frm_cnt 0x0
S:sw_disc_frm_cnt 0x0          last_disc_frm_cnt 0x0
S:txq_nopop_pr_cnt 0x0          pollErrataDfe_ptBM
0xba01b4b0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][0] 0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][1] 0x0

```

```

S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][2]          0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][0] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][1]          0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][2] 0x0
S:
S:C4 Logical Port Variables
S:-----
-----
S:c4_lgc_regp          0x81c48000
S:c4_phyp:
S:      0xb6ac4100      0x0          0x0          0x0

S:      0x0          0x0          0x0          0x0

S:master_phyp          0xb6ac4100      if_id
0x43020009
S:min_phyp          0x0          max_phyp          0x0
S:num_phy_ports      1          lgc_num          9
S:num_iu_to          0          sw_txq_bm
0
S:port_fid          129          unused          0
S:port_group          1          lgc_stats_clear_ts
1725611419
S:domain_tbl_sel          0          area_tbl_sel
0
S:egid_tbl_sel          0
S:serv_lo_bm          0x0
S:
S:Proto Phy Variables:
S:-----
-----
S:magic_id          0xc4123456      asic_phyp
0xb6ac4100
S:port_id          0x43028009      phy_cfg
0xb6ac5140
S:upsm_hdl          0xb80121e0      physm_hdl
0xb8011f00
S:ov_snsn_hdl          0xb8011dc0      sw_snsn_hdl
0xb8011e60
S:ov_lksm_hdl          0xb8012000      sw_lksm_hdl
0xb80120a0
S:trksm_hdl          0xb8012140      lr_flag          0x0
S:lr_active          0x0          qsfp_txx_rate_sel
0x0

S:
S:UPSM      UP00: UPST_PORT_DISABLED      --> UP00: UPST_PORT_DISABLED
S:SNSM(OV)  SN00: OV_SNST_STOPPED      --> SN00: OV_SNST_STOPPED
S:SNSM(SW)  SW00: SW_SNST_STAGE_WS      --> SW00: SW_SNST_STAGE_WS
S:PHYSM      PP00: PHYST_STOPPED      --> PP00: PHYST_STOPPED
S:LKSM(OV)  LK00: OV_LKST_INACTIVE      --> LK00: OV_LKST_INACTIVE
S:LKSM(SW)  SW13: INACTIVE      --> SW13: INACTIVE
S:TRKSM      TRK0: TRKST_INIT      --> TRK0: TRKST_INIT
S:
S:physm variables:

```



```

S:-----
-----
S:proto_phyph          0xb88077e0      physm_hdl
0xb8011f00
S:force_offline        0              copper              0
S:fault_reason         0: UNKNOWN
S:phy_media_present    0
S:
S:snsn variables:
S:-----
-----
S:speed                0xff          proto_phyph
0xb88077e0
S:hw_sn_tries_left    0x0           sw_sn_tries_left    0x0
S:curr_txsp_count     0x0           curr_tx_indx
S:tx_max              0x0
0x0
S:curr_tx             0x0           curr_rxsp_count
0x0
S:rx_max              0x0           curr_rx_indx
0x0
S:curr_rx             0x0           rx_mem
0x0
S:rxsp_rec_count      0x0
S:nc_start            0x0           tx_start             0x0
S:sync_start          0x0           sync_present         0x0
S:diag_auto           0x0           diag_speed           0xff
S:striped_wd_tov      3000         hw_wd_tov
3000
S:step                0x0           qsfp28_speed_mode
0x0
S:qsfp_mode0_hw_sn_tries_left 0x0
S:qsfp_mode1_hw_sn_tries_left 0x0
S:
S:lksm variables:
S:-----
-----
S:proto_phyph          0xb88077e0      ov_lksm_hdl
0xb8012000
sw_lksm_hdl          0xb80120a0
num_lf1              0
S:hw_link_tries_left  0              sw_link_tries_left  0
S:buf_ptype           0x0           stored_entry_state   0x6
S:handshake_owner     0x0           mark_unsent
0x0
S:busybuf_stuck       0x0           lr_wait              0x0
S:
S:trksm variables:
S:-----
-----
S:Not a trunk port
S:
S:upsm variables:
S:-----

```

```

-----
S:proto_phyph          0xb88077e0      upsm_hdl
0xb80121e0
S:bb_credits           0              port_beacon      0
S:port_diag_flag      0              0                force_offline
0
S:port_fault_rsn      0: PORT_NO_FAULT
S:retry_init_rsn      0: UNKNOWN
S:limit_reason         0              linit_result     0
S:ie_fctl_mode        0              fec_in_sync_tries_left 0
S:retry_sn_fail_init  0
retry_link_fail_init  0
S:excess_lr_count     0
S:
S:c4_ch_cfg
S:-----
-----
S:c4_desc_ring_size   256           292             256           256           292
292           2           292           292
S:thresh_def          0              16              1              0
S:intr_tries          500           cmem_pattern
0xdeadbeef
S:cmem_pattern_upwd   2              cmem_init_time   16
S:cmem_init_tries     5
S:ctrl_par_thresh     2              data_par_thresh
4
S:cam_par_thresh      4              buf_loss_thresh
12
S:crit_par_thresh     2              non_crit_par_thresh
6
S:pci_abort_thresh    10            pci_err_thresh   5
S:excess_chintr_thresh 8              sw_err_thresh    20
S:err_sample_period   300           intr_sleep
20000
S:frame_timeout       2500           proxy_dev        16384
S:vf_route            81920          qos              2048
S:stats 2048          f_redirect      2048
S:rsp_trap            2048           lun_zoning       20480
S:area_mode           0              ftb_max_loop[0] 0
S:ftb_max_loop[1]     6              ftb_max_loop[2] 9
S:ftb_max_loop[3]     10             ftb_max_loop[4] 10
S:ftb_max_loop[5]     5              ftb_max_loop[6] 6
S:ftb_seg_size[0]     0              ftb_seg_size[1] 16384
S:ftb_seg_size[2]     65536          ftb_seg_size[3] 16384
S:ftb_seg_size[4]     16384          ftb_seg_size[5] 65536
S:ftb_seg_size[6]     16384          ftb_seg_base[0] 0
S:ftb_seg_base[1]     0              ftb_seg_base[2] 65536
S:ftb_seg_base[3]     16384          ftb_seg_base[4] 32768
S:ftb_seg_base[5]     131072         ftb_seg_base[6]

```

49152

asic_err_monitor_period1 300
asic_err_monitor_period2 86400
zone_chk_to_poll_period 25
zone_chk_class2_reject_tov 220

S:

S:c4_phy_cfg

S:-----

S:version = 2.1

S:pt 0x43028009 fab_ptr

0x9a800000

S:fabattr 0x9a8000d4 fab_iop

0x9a800050

S:cfgbm 0xbb835384 port_ctrl

0xb6ac5158

S:pcap.pcap_bm 0x8d215547 pcap.pcap2_bm

0x2588289

S:pcap.pcap3_bm 0x1bebe0c

ui_idx 50 S:slot_no

0

is_icl 0 S:sw_usr_ports 400

S:neg_speed 0 0 0 0 0 0

S:my_domain 0x1 port_mode 0x0

S:hw_sn_maxtries 100 sw_sn_maxtries

0

S:hw_link_maxtries 10 sw_link_maxtries 5

S:rx_cyc_tov 28 rttov 300

S:bufrdy_tov 300 busybuf_tov 286

S:mark_tov 300 lksm_tov 3000

S:buf_dealloc_wait 4 hw_wd_tov 3000

S:hw_lk_train_tov 540 hw_lk_test_tov

150

S:syswait_tx_12_lips 1 lip_rx_tov 55

S:al_time_tov 15 lp_tov 2000

S:intr_tries_port 500 intr_mod_debounce

250

S:intr_lsrflt_debounce 500 intr_efifo_debounce 100

S:port_no_fid 3 excess_ptintr_thresh 8

S:port_fault1_thresh 100 port_fault1_spur_thresh 250

S:port_fault1_disc_thresh 500

port_fault1_disc_spur_thresh 1000

S:port_fault2_thresh 5 losync_tov 100

S:port_sw_link_to 15 en_8g_scramble

1

frc_hw_sn_mode 0x1

S:enc_poll_thresh 0 fec_enable

0

S:fec_in_sync_to 50 fec_in_sync_try_max

4

S:port_be_lto_threshold 100 port_be_lr_threshold

2

S:be_cr_in_sync_to 5

port_credit_overrun_thresh 10


```

S:port_ctrl.cm.skip_bb_credit          0
S:port_ctrl.cm.use_shim_based_sublist  0
S:
S:    port_ctrl.serdes_set
S:=====
S:serdes_type                          0x8
S:serdes_data_t.ibm_hss_serdes.tx_drive_power      0x1
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b_sign  0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b      0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_a      0x0
S:serdes_data_t.ibm_hss_serdes.rxeq                0x0
S:
S:    cfgbm
S:=====
S:old_distance          0x0          gport_lockdown      0x0
S:tport                0x1          speed                  0x0
S:disable_eport        0x0          fcacc                0x0
S:lport_lockdown      0x0          0x0                  priv_lport_lockdown
0x0
S:vcxlt_linit          0x0          delay_flogi          0x0
S:isl_interop          0x0          distance              0x0
S:BufStarvFlag        0x0          credit_sharing       0x0
S:lport_halfduplex    0x0          lport_fairness       0x0
S:soft_neg            0x0          asn_frc_hwretry      0x0
S:cr_recov            0x0          fport_buffers        0x0
S:export              0x0          0x0                  export_mode
0x0
S:csctl_en            0x0          mirror_port          0x0
S:fault_delay         0x0          non_dfe              0x0
S:fec_configured*(0=ENAB)  0          0                    fec_tts
0
S:port_persistently_disabled (permanently) 0 (0)
S:
S:    cfg property
S:=====
S:priv_pcfg_bm        0x00000000    lgcl_pcfg_bm
0xbb8353c4
S:fport_buffer        0x00000000
S:
S:
S:C4 Discard Cntrs: rxlp_stats = 0xb6ac44b0
S:-----
-----
S:disc_mcast_wka      0x0          disc_inv_did         0x0
S:disc_cl1_cl4        0x0          disc_sid_chk_fail    0x0
S:disc_inv_dom_egid_txpt 0x0          0x0                  disc_vft_hop_cnt_1
0x0
S:disc_classf         0x0          0x0                  disc_fcp_cdb_inv     0x0
S:disc_vfid_trap_enabled 0x0          0x0
disc_vfid_hdr_chk_fail 0x0
S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err 0x0
S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err 0x0
S:disc_ftb_vm_mode    0x0          disc_ftb_agnt2_miss   0x0
S:disc_ecb_de_pad_err 0x0          disc_ecb_de_tag_err   0x0

```

```

S:disc_ecb_de_seq_err 0x0          disc_ecb_err          0x0
S:disc_ftb_type4_match 0x0        disc_fcp_rsp_ftb_type4 0x0
S:disc_fcp_rsp_ftb_type4 0x0      disc_ftb_type5_match
  0x0
S:disc_ftb_type3_match 0x0        disc_els_ftb_type3    0x0
S:disc_ftb_type1_match 0x0        disc_els_rsp_ex_port  0x0
S:disc_inv_drp_dps     0x0        disc_did_lookup_miss  0x0
S:disc_ftb_type2_match 0x0        disc_trpd_plogi_pdisc 0x0
S:disc_type2_lookup_miss 0x0     disc_ftb_type6_match
  0x0
S:disc_els_rep_ex_port 0x0        disc_els_sid_lkup_bit1 0x0
S:disc_els_sid_lkup_bit0 0x0
disc_bls_frm_trap_bit1 0x0
S:disc_ftb_token_err 0x0         disc_asic_internal_err 0x0
S:disc_hard_zone_miss 0x0        disc_lun_zone_miss    0x0
S:discflt_frame_disc 0x0         discflt_parity_err    0x0
S:disc_frame_marked_du 0x0       disc_frame_marked_to  0x0
E:Connection type: FE
E:Port type: E_port
E:Trunk port: No
E:Configured Speed: AUTO_SPEED_NEGO
E:Max Capable Speed: 32G
E:Current SNSM Speed: UNDEFINED
E:Hardware TX Speed: 32G (0x00000004)
E:Hardware RX Speed: 32G (0x00000040)
E:
E:Interrupts: 0          Link_failure: 0
Loss_of_sync: 0         Loss_of_sig: 0
E:Lli: 0                Invalid_word: 0
E:trapped_frm: 0        fwd_status_ok: 0
E:fwd_timeout: 0        fwd_tx_unavail: 0
E:fwd_unroutable: 0     fwd_zone_out: 0
E:fwd_other_err: 0      frm_err_discard: 0
E:Fltr listA: 0         Fltr listB: 0
E:Zone trap fwd: 0      Zone trap disc: 0
E:shim_csum: 0          RTE_perr: 0
E:Invalid_crc: 0        Delim_err: 0
E:Protocol_err: 0
E:Lr_in: 0              Lr_out: 0
E:Ols_in: 0             Ols_out: 0

```

filterportshow 50

FILTER DATA

```

Shadow settings:
  Filter Enable: 0x00000000
  Redir RAM[0]: 0x00000000
  Redir RAM[1]: 0x00000000
  Redir RAM[2]: 0x00000000
  Redir RAM[3]: 0x00000000
  Redir RAM[4]: 0x00000000
  Redir RAM[5]: 0x00000000

```

Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass: 0x00000000

Real settings:

Enable RAM: 0x00000000, 0x00000000

Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000

Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass RAM: 0x00000000

Shadowed filters:

Filter 0: Not Installed (MIRROR1)(LISTA)
c4_fldenable[0] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[0] = 0x00000000,c4_fltr_config[0] = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
c4_fldenable[1] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[1] = 0x00000000,c4_fltr_config[1] = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
c4_fldenable[2] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[2] = 0x00000000,c4_fltr_config[2] = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
c4_fldenable[3] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[3] = 0x00000000,c4_fltr_config[3] = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
c4_fldenable[4] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[4] = 0x00000000,c4_fltr_config[4] = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
c4_fldenable[5] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[5] = 0x00000000,c4_fltr_config[5] = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
c4_fldenable[6] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[6] = 0x00000000,c4_fltr_config[6] = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
c4_fldenable[7] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[7] = 0x00000000,c4_fltr_config[7] = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
c4_fldenable[8] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[8] = 0x00000000,c4_fltr_config[8] = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
c4_fldenable[9] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[9] = 0x00000000,c4_fltr_config[9] = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
c4_fldenable[10] = 0x00000000 0x00000000 0x00000000
0x00000000


```
    c4_fldnegate[10] = 0x00000000,c4_fltr_config[10] =
0x00000000
Filter 11: Not Installed (SIM)(LISTA)
    c4_fldenable[11] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[11] = 0x00000000,c4_fltr_config[11] =
0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
    c4_fldenable[12] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[12] = 0x00000000,c4_fltr_config[12] =
0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
    c4_fldenable[13] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[13] = 0x00000000,c4_fltr_config[13] =
0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
    c4_fldenable[14] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[14] = 0x00000000,c4_fltr_config[14] =
0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
    c4_fldenable[15] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[15] = 0x00000000,c4_fltr_config[15] =
0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
    c4_fldenable[16] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[16] = 0x00000000,c4_fltr_config[16] =
0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
    c4_fldenable[17] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[17] = 0x00000000,c4_fltr_config[17] =
0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
    c4_fldenable[18] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[18] = 0x00000000,c4_fltr_config[18] =
0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
    c4_fldenable[19] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[19] = 0x00000000,c4_fltr_config[19] =
0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
    c4_fldenable[20] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[20] = 0x00000000,c4_fltr_config[20] =
0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
    c4_fldenable[21] = 0x00000000 0x00000000 0x00000000
```

```
0x00000000
    c4_fldnegate[21] = 0x00000000,c4_fltr_config[21] =
0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
    c4_fldenable[22] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[22] = 0x00000000,c4_fltr_config[22] =
0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
    c4_fldenable[23] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[23] = 0x00000000,c4_fltr_config[23] =
0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
    c4_fldenable[24] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[24] = 0x00000000,c4_fltr_config[24] =
0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
    c4_fldenable[25] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[25] = 0x00000000,c4_fltr_config[25] =
0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
    c4_fldenable[26] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[26] = 0x00000000,c4_fltr_config[26] =
0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
    c4_fldenable[27] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[27] = 0x00000000,c4_fltr_config[27] =
0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
    c4_fldenable[28] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[28] = 0x00000000,c4_fltr_config[28] =
0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
    c4_fldenable[29] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[29] = 0x00000000,c4_fltr_config[29] =
0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    c4_fldenable[30] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[30] = 0x00000000,c4_fltr_config[30] =
0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    c4_fldenable[31] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[31] = 0x00000000,c4_fltr_config[31] =
0x00000000
```

Real filters:

Filter 0: Not Installed (MIRROR1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 1: Not Installed (MIRROR2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 2: Not Installed (MIRROR3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 3: Not Installed (MIRROR4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 5: Not Installed (ZONING TRAP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 7: Not Installed (TIN TRAP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 8: Not Installed (FICON CUP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 9: Not Installed (FICON CUP DST)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 11: Not Installed (SIM)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 12: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,

```
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
```

```
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
```

Filter dirty indicator: 0x00000000

Performance filters: 0

Port Mirror filters: 0 (0x0)

FIELD DATA

Shadowed fields:

```
fldoffset[0] = 0x00, fldmask[0] = 0x00, fldvalue_dyna[0]: 0x00 0x00
0x00 0x00
fldcontrol[0].inuse = 0x0  fldcontrol[0].refcnt = 0x00 0x00 0x00
0x00
fldoffset[1] = 0x00, fldmask[1] = 0x00, fldvalue_dyna[1]: 0x00 0x00
0x00 0x00
fldcontrol[1].inuse = 0x0  fldcontrol[1].refcnt = 0x00 0x00 0x00
0x00
fldoffset[2] = 0x00, fldmask[2] = 0x00, fldvalue_dyna[2]: 0x00 0x00
0x00 0x00
fldcontrol[2].inuse = 0x0  fldcontrol[2].refcnt = 0x00 0x00 0x00
0x00
fldoffset[3] = 0x00, fldmask[3] = 0x00, fldvalue_dyna[3]: 0x00 0x00
0x00 0x00
fldcontrol[3].inuse = 0x0  fldcontrol[3].refcnt = 0x00 0x00 0x00
0x00
fldoffset[4] = 0x00, fldmask[4] = 0x00, fldvalue_dyna[4]: 0x00 0x00
0x00 0x00
fldcontrol[4].inuse = 0x0  fldcontrol[4].refcnt = 0x00 0x00 0x00
0x00
```

```
fldoffset[5] = 0x00, fldmask[5] = 0x00, fldvalue_dyna[5]:0x00 0x00
0x00 0x00
fldcontrol[5].inuse = 0x0  fldcontrol[5].refcnt = 0x00 0x00 0x00
0x00
fldoffset[6] = 0x00, fldmask[6] = 0x00, fldvalue_dyna[6]:0x00 0x00
0x00 0x00
fldcontrol[6].inuse = 0x0  fldcontrol[6].refcnt = 0x00 0x00 0x00
0x00
fldoffset[7] = 0x00, fldmask[7] = 0x00, fldvalue_dyna[7]:0x00 0x00
0x00 0x00
fldcontrol[7].inuse = 0x0  fldcontrol[7].refcnt = 0x00 0x00 0x00
0x00
fldoffset[8] = 0x00, fldmask[8] = 0x00, fldvalue_dyna[8]:0x00 0x00
0x00 0x00
fldcontrol[8].inuse = 0x0  fldcontrol[8].refcnt = 0x00 0x00 0x00
0x00
fldoffset[9] = 0x00, fldmask[9] = 0x00, fldvalue_dyna[9]:0x00 0x00
0x00 0x00
fldcontrol[9].inuse = 0x0  fldcontrol[9].refcnt = 0x00 0x00 0x00
0x00
fldoffset[10] = 0x00, fldmask[10] = 0x00, fldvalue_dyna[10]:0x00 0x00
0x00 0x00
fldcontrol[10].inuse = 0x0  fldcontrol[10].refcnt = 0x00 0x00 0x00
0x00
fldoffset[11] = 0x00, fldmask[11] = 0x00, fldvalue_dyna[11]:0x00 0x00
0x00 0x00
fldcontrol[11].inuse = 0x0  fldcontrol[11].refcnt = 0x00 0x00 0x00
0x00
fldoffset[12] = 0x00, fldmask[12] = 0x00, fldvalue_dyna[12]:0x00 0x00
0x00 0x00
fldcontrol[12].inuse = 0x0  fldcontrol[12].refcnt = 0x00 0x00 0x00
0x00
fldoffset[13] = 0x00, fldmask[13] = 0x00, fldvalue_dyna[13]:0x00 0x00
0x00 0x00
fldcontrol[13].inuse = 0x0  fldcontrol[13].refcnt = 0x00 0x00 0x00
0x00
fldoffset[14] = 0x00, fldmask[14] = 0x00, fldvalue_dyna[14]:0x00 0x00
0x00 0x00
fldcontrol[14].inuse = 0x0  fldcontrol[14].refcnt = 0x00 0x00 0x00
0x00
fldoffset[15] = 0x00, fldmask[15] = 0x00, fldvalue_dyna[15]:0x00 0x00
0x00 0x00
fldcontrol[15].inuse = 0x0  fldcontrol[15].refcnt = 0x00 0x00 0x00
0x00
fldoffset[16] = 0x00, fldmask[16] = 0x00, fldvalue_dyna[16]:0x00 0x00
0x00 0x00
fldcontrol[16].inuse = 0x0  fldcontrol[16].refcnt = 0x00 0x00 0x00
0x00
fldoffset[17] = 0x00, fldmask[17] = 0x00, fldvalue_dyna[17]:0x00 0x00
0x00 0x00
fldcontrol[17].inuse = 0x0  fldcontrol[17].refcnt = 0x00 0x00 0x00
0x00
fldoffset[18] = 0x00, fldmask[18] = 0x00, fldvalue_dyna[18]:0x00 0x00
0x00 0x00
```

```
fldcontrol[18].inuse = 0x0 fldcontrol[18].refcnt = 0x00 0x00 0x00
0x00
fldoffset[19] = 0x00, fldmask[19] = 0x00, fldvalue_dyna[19]:0x00 0x00
0x00 0x00
fldcontrol[19].inuse = 0x0 fldcontrol[19].refcnt = 0x00 0x00 0x00
0x00
```

Real fields:

```
fldoffset RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000
fldmask RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000
fld value4 RAM:
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
Field dirty indicator: 0x00000000
```

```
FDB reference count fdb: 0 [0 0 0 0 ]
FDB reference count fdb: 1 [0 0 0 0 ]
FDB reference count fdb: 2 [0 0 0 0 ]
FDB reference count fdb: 3 [0 0 0 0 ]
FDB reference count fdb: 4 [0 0 0 0 ]
FDB reference count fdb: 5 [0 0 0 0 ]
FDB reference count fdb: 6 [0 0 0 0 ]
FDB reference count fdb: 7 [0 0 0 0 ]
FDB reference count fdb: 8 [0 0 0 0 ]
FDB reference count fdb: 9 [0 0 0 0 ]
FDB reference count fdb: 10 [0 0 0 0 ]
FDB reference count fdb: 11 [0 0 0 0 ]
FDB reference count fdb: 12 [0 0 0 0 ]
FDB reference count fdb: 13 [0 0 0 0 ]
FDB reference count fdb: 14 [0 0 0 0 ]
FDB reference count fdb: 15 [0 0 0 0 ]
FDB reference count fdb: 16 [0 0 0 0 ]
FDB reference count fdb: 17 [0 0 0 0 ]
```

FDB reference count fdb: 18 [0 0 0 0]
FDB reference count fdb: 19 [0 0 0 0]

Filter counters:

Filter counter 0: 0 (MIRROR1)
Filter counter 1: 0 (MIRROR2)
Filter counter 2: 0 (MIRROR3)
Filter counter 3: 0 (MIRROR4)
Filter counter 4: 0 (AEPORT_NON_MIRR_DROP)
Filter counter 5: 0 (ZONING TRAP)
Filter counter 6: 0 (FCR_EXPORT_DC)
Filter counter 7: 0 (TIN TRAP)
Filter counter 8: 0 (FICON CUP)
Filter counter 9: 0 (FICON CUP DST)
Filter counter 10: 0 (WELL KNOWN ADDR)
Filter counter 11: 0 (SIM)
Filter counter 12: 0 (UNUSED)
Filter counter 13: 0 (UNUSED)
Filter counter 14: 0 (UNUSED)
Filter counter 15: 0 (UNUSED)
Filter counter 16: 0 (PERF1)
Filter counter 17: 0 (PERF2)
Filter counter 18: 0 (PERF3)
Filter counter 19: 0 (PERF4)
Filter counter 20: 0 (PERF5)
Filter counter 21: 0 (PERF6)
Filter counter 22: 0 (PERF7)
Filter counter 23: 0 (PERF8)
Filter counter 24: 0 (PERF9)
Filter counter 25: 0 (PERF10)
Filter counter 26: 0 (PERF11)
Filter counter 27: 0 (PERF12)
Filter counter 28: 0 (OPM1)
Filter counter 29: 0 (OPM2)
Filter counter 30: 0 (IPM1)
Filter counter 31: 0 (IPM2)

ACL DATA

Logical port 9: Hard Zoning disabled, Soft Zoning disabled
Zone type: WWN Zoning
Frames with hard zone miss: 0

*** Please use filterportshow on user port 56 to display ACL hash tables and Mirroring resources of thischip.
***We show this data only for the first physical port which is an external port.

portFcPortCmdShow --slot 0 51 3
doing portFcPortCmdShow: arg1 = 3, arg2 = -2

portshow 51
portDisableReason: None
portCFlags: 0x0


```

portFlags: 0x4021          PRESENT U_PORT DISABLED LED
LocalSwcFlags: 0x0
portType: 26.0
POD Port: Need license to enable the port
portState: 2    Offline
Protocol: FC
portPhys: 2    No_Module      portScn: 2    Offline
port generation number: 0
state transition count: 0

```

```

portId: 013300
portIfId: 4302000a
portWwn: 20:33:d8:1f:cc:2c:99:90
portWwn of device(s) connected:
16b Area list:
Distance: normal
portSpeed: N32Gbps

```

```

FEC: Inactive
Credit Recovery: Inactive
LE domain: 0
Peer beacon: Off
FC Fastwrite: OFF

```

```

Interrupts: 0          Link_failure: 0          Frjt:
0
Unknown: 0          Loss_of_sync: 0          Fbsy:
0
Lli: 0          Loss_of_sig: 0
Proc_rqrd: 0          Protocol_err: 0
Timed_out: 0          Invalid_word: 0
Tx_unavail: 0          Invalid_crc: 0
Delim_err: 0          Address_err: 0
Lr_in: 0          Ols_in: 0
Lr_out: 0          Ols_out: 0

```

```

portloginshow 51
Type  PID      World Wide Name      credit df_sz cos
=====

```

```

portloginshow 51 -history
Type  PID      World Wide Name      logout time
=====

```

```

portregshow 51

```

```

LED registers
=====
0x81c52000: c4_led_status      00000000      0x81c52004:
c4_led_ctl      00000000

```

```

FPL registers

```

```

=====
0x81c50200: fpl_port_config          23490000
0x81c5020c: fpl_port_id_ctl                00000000    0x81c50210:
fpl_port_id_addr          00013300
0x81c50214: fpl_port_speed                00000004    0x81c5021c:
fpl_lli_ctl              00000903
0x81c50228: fpl_lli_os_ctl                bc95b5b5    0x81c5022c:
fpl_lli_send_word        bc95b5b5
0x81c50230: fpl_lli_mark_rx              00000000    0x81c50234:
fpl_lli_rnd_trip_time    00000000
0x81c50238: fpl_lli_ns_status            80070007    0x81c5023c:
fpl_lli_intr_status      80070007
0x81c50244: fpl_lli_def                  00000000    0x81c50254:
fpl_lli_intr_enable_clr  00100000
0x81c50258: fpl_err_intr_status          00000000    0x81c50260:
fpl_err_intr_enable_clr  00000000
0x81c50268: fpl_err_first_error          00000000    0x81c5026c:
fpl_speed_neg_ctl        00000000
0x81c50270: fpl_speed_neg_stat           00000000    0x81c50274:
fpl_softasn_ctl          0000000f
0x81c50278: fpl_link_init_ctl            00000000    0x81c5027c:
fpl_link_init_stat        00000000
0x81c50280: fpl_aec_ctl                  00051060    0x81c50284:
fpl_aec_ctl2             04009f60
0x81c50288: fpl_pcs_ctl                  00000160    0x81c5028c:
fpl_fec_ctl              00000441
0x81c50290: fpl_fec_cor                  00000000    0x81c50294:
fpl_fec_uncor            00000000
0x81c50298: fpl_hss_link_ctl            0031f040    0x81c5029c:
fpl_afifo_link_ctl        00000a86
0x81c502a0: fpl_echo_lb_ctl             0000028c    0x81c502a4:
fpl_scratch              00000121
0x81c502a8: fpl_debug                    00030005    0x81c502ac:
fpl_misc_debug           00001800
0x00000000: SW_shadow_reg                00000000    0x00000000:
SW_c4_phyp->cfgptr        00030000

```

per-fpg (per octet) registers

```

=====
0x8180b82c: fpg_serdes_ctla0            81a37be7    0x8180b830:
fpg_serdes_ctla1          81a37be7
0x8180b834: fpg_serdes_ctlb0            81a1c3c3    0x8180b838:
fpg_serdes_ctlb1          81a1c3c3
0x8180b83c: fpg_serdes_xgmii_1ms        00067c28    0x8180b840:
fpg_serdes_regtimctl      40e47946
0x8180b844: fpg_serdes_asnrsttimctl    00000102

```

HSS PLL registers

```

=====
0x81809400: 00_hssplla_vco_coarse_cal0    00000000    0x81809404:
01_hssplla_vco_coarse_cal1    00000014
0x81809408: 02_hssplla_vco_coarse_cal2    00000000    0x8180940c:
03_hssplla_vco_coarse_cal3    00000000
0x81809410: 04_hssplla_vco_coarse_cal4    00000000    0x81809424:

```

| | | | |
|--|----------|-------------|--|
| 09_hssplla_power_ctl | 00000000 | | |
| 0x81809428: 0A_hssplla_charge_pump_ctl | 00000004 | 0x81809438: | |
| 0E_hssplla_pll_misc_ctl | 00000000 | | |
| 0x8180943c: 0F_hssplla_pclk_ctl | 000000f8 | 0x81809440: | |
| 10_hssplla_eyem_intv_ctl | 00000000 | | |
| 0x81809444: 11_hssplla_eyem_intv_lim1 | 00000000 | 0x81809448: | |
| 12_hssplla_eyem_intv_lim2 | 00000000 | | |
| 0x8180944c: 13_hssplla_eyem_intv_lim3 | 00000000 | 0x81809450: | |
| 14_hssplla_eyem_intv_lim4 | 00000000 | | |
| 0x818094f0: 3C_hssplla_macro_tst_ctl4 | 00000000 | 0x818094f4: | |
| 3D_hssplla_macro_tst_ctl3 | 00000000 | | |
| 0x818094f8: 3E_hssplla_macro_tst_ctl2 | 00000000 | 0x818094fc: | |
| 3F_hssplla_macro_tst_ctl1 | 00000000 | | |
| 0x81809500: 00_hssppll_vco_coarse_cal0 | 0000000a | 0x81809504: | |
| 01_hssppll_vco_coarse_cal1 | 00000014 | | |
| 0x81809508: 02_hssppll_vco_coarse_cal2 | 00000000 | 0x8180950c: | |
| 03_hssppll_vco_coarse_cal3 | 00000000 | | |
| 0x81809510: 04_hssppll_vco_coarse_cal4 | 00000000 | 0x81809524: | |
| 09_hssppll_power_ctl | 00000000 | | |
| 0x81809528: 0A_hssppll_charge_pump_ctl | 00000004 | 0x81809538: | |
| 0E_hssppll_pll_misc_ctl | 00000000 | | |
| 0x8180953c: 0F_hssppll_pclk_ctl | 000000f8 | 0x81809540: | |
| 10_hssppll_eyem_intv_ctl | 00000000 | | |
| 0x81809544: 11_hssppll_eyem_intv_lim1 | 00000000 | 0x81809548: | |
| 12_hssppll_eyem_intv_lim2 | 00000000 | | |
| 0x8180954c: 13_hssppll_eyem_intv_lim3 | 00000000 | 0x81809550: | |
| 14_hssppll_eyem_intv_lim4 | 00000000 | | |
| 0x818095f0: 3C_hssppll_macro_tst_ctl4 | 00000000 | 0x818095f4: | |
| 3D_hssppll_macro_tst_ctl3 | 00000000 | | |
| 0x818095f8: 3E_hssppll_macro_tst_ctl2 | 00000000 | 0x818095fc: | |
| 3F_hssppll_macro_tst_ctl1 | 00000000 | | |

HSS TX registers

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| | | | |
|--------------------------------------|----------|-------------|--|
| 0x81808400: 00_hsstx_cfg_mode_PHY | 00009f48 | 0x81808404: | |
| 01_hsstx_test_ctl | 00000000 | | |
| 0x81808408: 02_hsstx_coeff_ctl_INV | 00000000 | 0x8180840c: | |
| 03_hsstx_drv_mode_ctl | 00000000 | | |
| 0x81808410: 04_hsstx_drv_ovrd_ctl | 00000010 | 0x81808414: | |
| 05_hsstx_dclk_align_ovrd | 00000080 | | |
| 0x81808418: 06_hsstx_imp_cal_ovrd | 00000c0c | 0x8180841c: | |
| 07_hsstx_dclk_drift_tol | 00000004 | | |
| 0x81808420: 08_hsstx_tap0_coeff_TUNE | 00000000 | 0x81808424: | |
| 09_hsstx_tap1_coeff_TUNE | 00000003 | | |
| 0x81808428: 0A_hsstx_tap2_coeff_TUNE | 00000018 | 0x8180842c: | |
| 0B_hsstx_tap3_coeff_TUNE | 0000000d | | |
| 0x81808434: 0D_hsstx_pol_INV | 0000000a | 0x81808438: | |
| 0E_hsstx_ae_cmd | 00000000 | | |
| 0x8180843c: 0F_hsstx_ae_stat | 00000000 | 0x81808440: | |
| 10_hsstx_ae_tap0_TUNE | 00000000 | | |
| 0x81808444: 11_hsstx_ae_tap1_TUNE | 00000000 | 0x81808448: | |
| 12_hsstx_ae_tap2_TUNE | 00000028 | | |
| 0x8180844c: 13_hsstx_ae_tap3_TUNE | 00000000 | 0x81808454: | |
| 15_hsstx_app_tune | 0000120e | | |

| | | |
|---|----------|-------------|
| 0x81808458: 16_hsstx_analog_diag | 00000000 | 0x81808460: |
| 18_hsstx_4x_seg_app | 0000aafa | |
| 0x81808464: 19_hsstx_2x_seg_app | 00000000 | 0x81808468: |
| 1A_hsstx_1x_seg_app | 0000ff5d | |
| 0x8180846c: 1B_hsstx_seg_4x_term_app | 00000000 | 0x81808470: |
| 1C_hsstx_seg_2x1x_term_app | 00000f00 | |
| 0x81808474: 1D_hsstx_tap_sign_app | 0000000a | 0x81808478: |
| 1E_hsstx_ext_addr_data | 00000001 | |
| 0x8180847c: 1F_hsstx_ext_addr_addr | 00000000 | 0x81808480: |
| 20_hsstx_pat_buf_bytes_1_0 | 00000000 | |
| 0x81808484: 21_hsstx_pat_buf_bytes_3_2 | 00000000 | 0x81808488: |
| 22_hsstx_pat_buf_bytes_5_4 | 00000000 | |
| 0x8180848c: 23_hsstx_pat_buf_bytes_7_6 | 00000000 | 0x8180849c: |
| 27_hsstx_8023az_ctl | 00000000 | |
| 0x818084a0: 28_hsstx_dcc_ctl | 000060c0 | 0x818084a4: |
| 29_hsstx_dcc_ovrd | 00001000 | |
| 0x818084a8: 2A_hsstx_dcc_app | 00000081 | 0x818084ac: |
| 2B_hsstx_dcc_timeout | 0000ffff | |
| 0x818084c0: 30_hsstx_tap_sign_ovrd | 00000000 | 0x818084c8: |
| 32_hsstx_seg_4x_ovrd | 00000000 | |
| 0x818084cc: 33_hsstx_seg_2x_ovrd | 00000000 | 0x818084d0: |
| 34_hsstx_seg_1x_ovrd | 00000000 | |
| 0x818084d8: 36_hsstx_tap_seg_4x_term_ovrd | 00000000 | 0x818084dc: |
| 37_hsstx_tap_seg_2x_term_ovrd | 00000000 | |
| 0x818084e0: 38_hsstx_tap_seg_1x_term_ovrd | 00000000 | 0x818084ec: |
| 3B_hsstx_mac_test_ctl5 | 00000000 | |
| 0x818084f0: 3C_hsstx_mac_test_ctl4 | 00000000 | 0x818084f4: |
| 3D_hsstx_mac_test_ctl3 | 00000000 | |
| 0x818084f8: 3E_hsstx_mac_test_ctl2 | 00000000 | 0x818084fc: |
| 3F_hsstx_mac_test_ctl1 | 000000c6 | |

HSS RX registers

=====

| | | |
|---------------------------------------|----------|-------------|
| 0x81808600: 00_hssrx_cfg_mode_PHY | 00009e78 | 0x81808604: |
| 01_hssrx_test_ctl | 00000000 | |
| 0x81808608: 02_hssrx_phs_rot_ctl | 0000cb80 | 0x8180860c: |
| 03_hssrx_phs_rot_ofs_ctl | 00000610 | |
| 0x81808610: 04_hssrx_phs_rot_posn1 | 00003f00 | 0x81808614: |
| 05_hssrx_phs_rot_posn2 | 00000031 | |
| 0x81808618: 06_hssrx_phs_rot_sta_ofs1 | 00000f1e | 0x8180861c: |
| 07_hssrx_phs_rot_sta_ofs2 | 0000001f | |
| 0x81808620: 08_hssrx_dfe_ctl_PHY | 00002002 | 0x81808624: |
| 09_hssrx_dfe_smpl_snap1 | 00000000 | |
| 0x81808628: 0A_hssrx_dfe_smpl_snap2 | 00008000 | 0x8180862c: |
| 0B_hssrx_vga_ctl1 | 00004005 | |
| 0x81808630: 0C_hssrx_vga_ctl2 | 00007aa0 | 0x81808634: |
| 0D_hssrx_vga_ctl3 | 000009e4 | |
| 0x81808638: 0E_hssrx_pwr_mgmt_ctl | 0000001f | 0x8180863c: |
| 0F_hssrx_iqamp_ctl1 | 00000018 | |
| 0x81808640: 10_hssrx_iqamp_ctl2 | 00000003 | 0x81808644: |
| 11_hssrx_dacap_dacan_sel | 00000003 | |
| 0x81808648: 12_hssrx_dacap_dacan | 0000ffff | 0x8180864c: |
| 13_hssrx_daca_min | 00000000 | |
| 0x81808650: 14_hssrx_adac_ctl | 000000ff | 0x81808654: |

| | | | |
|--|----------|-----------|-------------|
| 15_hssrx_ac_cp_ctl | 000031c3 | | |
| 0x81808658: 16_hssrx_ac_cp_val | | 00008055 | 0x8180865c: |
| 17_hssrx_dfe_h1h2h3_lcl_off_ch | 00000014 | | |
| 0x81808660: 18_hssrx_dfe_h1h2h3_lcl_off_val | 00000000 | | 0x81808664: |
| 19_hssrx_peaked_intg | 000000ff | | |
| 0x81808668: 1A_hssrx_cdr_analog_sw | | 0000ce00 | 0x8180866c: |
| 1B_hssrx_peaking_amp_init_c_PHY | 00000000 | | |
| 0x81808670: 1C_hssrx_dac_dpc | | 00000040 | 0x81808674: |
| 1D_hssrx_ddc | 00000000 | | |
| 0x81808678: 1E_hssrx_int_stat_PHY | | 00000c0f | 0x8180867c: |
| 1F_hssrx_dfe_func_ctl1_PHY | 0000ffff | | |
| 0x81808680: 20_hssrx_dfe_func_ctl2_INV | | 00007eff | 0x81808684: |
| 21_hssrx_ofs_ch_dcc_qcc_idx | 00002000 | | |
| 0x81808688: 22_hssrx_dfe_ofs_val | | 00007f07 | 0x8180868c: |
| 23_hssrx_h_coeff_bist | 00000401 | | |
| 0x81808690: 24_hssrx_ac_cap_bist | | 00000000 | 0x81808694: |
| 25_hssrx_max_gain_path_idx_res | 00007800 | | |
| 0x81808698: 26_hssrx_loff_ctl | | 00000054 | 0x8180869c: |
| 27_hssrx_sigdet_ctl | 00005180 | | |
| 0x818086a0: 28_hssrx_ana_ctl_sw | | 00000000 | 0x818086a4: |
| 29_hssrx_intg_dac_ofs | 0000aee0 | | |
| 0x818086a8: 2A_hssrx_eye_ctl | | 00000000 | 0x818086ac: |
| 2B_hssrx_eye_met | 00000004 | | |
| 0x818086b0: 2C_hssrx_eye_met_err_cnt | | 00000000 | 0x818086b4: |
| 2D_hssrx_eye_met_pdf_eyec | 00000000 | | |
| 0x818086b8: 2E_hssrx_eye_met_pat_len | | 0000007f | 0x818086bc: |
| 2F_hssrx_dfe_func_ctl3 | 0000dfff | | |
| 0x818086c0: 30_hssrx_dfe_tap_ctl_idx_ptr | | 00000008 | 0x818086c4: |
| 31_hssrx_dfe_tap | 00003030 | | |
| 0x818086c8: 32_hssrx_lte_ctl_TUNE | | 00001601 | 0x818086e4: |
| 39_hssrx_int_stat2 | 000041ff | | |
| 0x818086e8: 3A_hssrx_ac_cpl_cur_src_adj | | 00000040 | 0x818086ec: |
| 3B_hssrx_dcd_ctl | 00007c4c | | |
| 0x818086f0: 3C_hssrx_dcc_ctl | | 00000d41 | 0x818086f4: |
| 3D_hssrx_qcc_ctl | 0000698d | | |
| 0x818086f8: 3E_hssrx_mac_test_ctl2 | | 00000000 | 0x818086fc: |
| 3F_hssrx_mac_test_ctl1 | 00000000 | | |
| 0x81808648: 12_hssrx_dacap_dacan[02] | | 00fd fffd | |
| 0x81808660: 18_hssrx_dfe_h1h2h3_lcl_off_va[00] | | 0000 0000 | 0000 |
| 0000 0000 0000 0000 0000 | | | |
| 0x81808660: 18_hssrx_dfe_h1h2h3_lcl_off_va[08] | | 0000 0000 | 0000 |
| 0000 0000 0000 0000 0000 | | | |
| 0x81808660: 18_hssrx_dfe_h1h2h3_lcl_off_va[16] | | 0000 0000 | 0000 |
| 0000 0000 | | | |
| 0x81808688: 22_hssrx_dfe_ofs_val[00][00] | | 7f07 007f | 7b7b |
| 0000 077f 7f00 | | | |
| 0x81808688: 22_hssrx_dfe_ofs_val[03][00] | | 7d01 7f00 | 0179 |
| 0000 7a00 007f | | | |
| 0x81808688: 22_hssrx_dfe_ofs_val[06][00] | | 7a79 0000 | 7d05 |
| 007f 797a 0000 | | | |
| 0x81808688: 22_hssrx_dfe_ofs_val[09][00] | | 0908 7f7f | 7d00 |
| 0000 047d 0000 | | | |
| 0x81808688: 22_hssrx_dfe_ofs_val[12][00] | | 0504 0000 | 0309 |
| 0000 7f7b 0000 | | | |

```

0x81808688: 22_hssrx_dfe_ofs_val[15][00]          7f7c 0000 7e03
0000 057d 7f00
0x81808688: 22_hssrx_dfe_ofs_val[18][00]          7b09 0000 7f7b
0000 000b 007f
0x81808688: 22_hssrx_dfe_ofs_val[21][00]          000b 007f 000b
007f 000b 007f
0x81808688: 22_hssrx_dfe_ofs_val[24][00]          7b07 007f 0403
0000 0202 0000
0x81808694: 25_hssrx_max_gain_path_idx_res[00]    005a 083d 110f
18bc 210f 28ba 3099 3800
0x81808694: 25_hssrx_max_gain_path_idx_res[08]    40ef 48a5 5089
5800 6040 6800 70f9 7800
0x818086c4: 31_hssrx_dfe_tap[00]                  fffe 8080 0000
0000 0030 0030 3030 3030
0x818086c4: 31_hssrx_dfe_tap[08]                  3030 3030 3030
0000
0x818086e8: 3A_hssrx_ac_cpl_cur_src_adj[00]       0040 0040 0040
0040
0x818086ec: 3B_hssrx_dcd_ctl[00]                  7c4c 5c00 7c83
5c00 7c81
0x818086f0: 3C_hssrx_dcc_ctl[00]                  0d41 0d82 0d00
0d41
0x818086f4: 3D_hssrx_qcc_ctl[00]                  695c 698d

```

xfipcs, fec, aec, & aet registers

=====

```

0x81c50400: xfipcs_reg [00] 00002040 00000080 00000000
00000000 00000001 00000008 00000000 00000000
0x81c50420: xfipcs_reg [08] 00008c01 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c50440: xfipcs_reg [16] 00000000 00000000 00000000
00000000 00000040 00000000 00000000 00000000
0x81c50460: xfipcs_reg [24] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c50480: xfipcs_reg [32] 00000004 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c50620: fec_32g_128g_reg [08] 00000000 00000000 00000000
00000000 00000000 00000000 00000000
0x81c50648: fec_32g_128g_reg [18] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c50a00: aec_reg [00] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c50c00: aet_reg [00] 00000000 00000000 00000000
00000000 00000000

```

bbc registers

=====

```

0x81c51800: bbc_trc 0 0 0 0 0 0 0
0
0x81c51840: bbc_trc 0 0 0 0 0 0 0
0
0x81c51880: bbc_trc 0 0 0 0 0 0 0
0
0x81c518c0: bbc_trc 0 0 0 0 0 0 0

```

| | | | | | | | |
|-------------------------|-------------------------|----------|---|---|---|---|----------------------|
| 0 | | | | | | | |
| 0x81c51900: | bbc_trc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c51804: | bbc_mbc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c51844: | bbc_mbc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c51884: | bbc_mbc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c518c4: | bbc_mbc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c51904: | bbc_mbc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c51a00: | bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c51a20: | bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c51a40: | bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c51a60: | bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c51a80: | bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c51c00: | bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c51c20: | bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c51c40: | bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c51c60: | bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c51c80: | bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c51d00: | bbc_fbpc | 00000000 | | | | | 0x81c51d04: bbc_csc |
| 00000000 | | | | | | | |
| 0x81c51d08: | bbc_rcc_inc | 00000000 | | | | | 0x81c51d0c: |
| bbc_rqc_inc | 00000000 | | | | | | |
| 0x81c51d10: | bbc_fbpc_inc | 00000000 | | | | | 0x81c51d14: |
| bbc_tmc_inc | 00000000 | | | | | | |
| 0x81c51d18: | bbc_threshold | 00080100 | | | | | 0x81c51d1c: |
| bbc_counter_clr | 00000000 | | | | | | |
| 0x81c51d20: | bbc_debug_en | 00000000 | | | | | 0x81c51d24: bbc_ctrl |
| 00200020 | | | | | | | |
| 0x81c51d28: | bbc_rqc_rcc_thresh | 00000055 | | | | | 0x81c51d34: |
| bbc_bb_sc_n | 00000000 | | | | | | |
| 0x81c51d38: | bbc_crd_reco_debug | 00000000 | | | | | 0x81c51d3c: |
| bbc_crd_reco_debug_data | 00000000 | | | | | | |
| 0x81c51d40: | bbc_multi_frm_loss_cnt | 00000000 | | | | | 0x81c51d44: |
| bbc_multi_rdy_loss_cnt | 00000000 | | | | | | |
| 0x81c51d48: | bbc_1frm_loss_recov_cnt | 00000000 | | | | | 0x81c51d4c: |
| bbc_1rdy_loss_recov_cnt | 00000000 | | | | | | |
| 0x81c51d58: | bbc_int_status | 00000000 | | | | | 0x81c51d5c: |
| bbc_int_set | 00000000 | | | | | | |
| 0x81c51d60: | bbc_int_first | 00000000 | | | | | 0x81c51d64: |

```

bbc_frm_rdy_rx_err_addr 00000000
0x81c51d68: bbc_frm_rdy_tx_err_addr 00000000 0x81c51d6c:
bbc_trc_mbc_err_addr 00000000
0x81c51d70: bbc_frm_rdy_rx_dbl_ecc 00000000 0x81c51d74:
bbc_frm_rdy_tx_dbl_ecc 00000000
0x81c51d78: bbc_trc_mbc_dbl_ecc 00000000
0x81c51d7c: bbc_fsm_status 00001011 0x81c51d80:
bbc_force_err 00000000
0x81c51d84: bbc_crdt_avail0 ffffffff 0x81c51d88:
bbc_crdt_avail1 000000ff
0x81c51d8c: bbc_scratch 00000000

```

FPS registers

=====

```

0x81c50004: fps_er_enc_in 00000000 0x81c50008:
fps_er_crc 00000000
0x81c5000c: fps_er_trunc 00000000 0x81c50010:
fps_er_toolong 00000000
0x81c50014: fps_er_bad_eof 00000000 0x81c50018:
fps_er_enc_out 00000000
0x81c5001c: fps_er_bad_os 00000000 0x81c50020:
fps_er_flush 00000000
0x81c50024: fps_er_ifg 00000000 0x81c50038:
fps_er_crc_good_eof 00000000
0x81c5003c: fps_inv_arb 00000000 0x81c50040:
fps_slow_sts_status 00000000
0x81c50044: fps_tx_frm_cnt 00000000 0x81c50048:
fps_rx_frm_cnt 00000000
0x81c50050: fps_tx_word_cnt_hi 00000000 0x81c5004c:
fps_tx_word_cnt_lo 00000000
0x81c50058: fps_rx_word_cnt_hi 00000000 0x81c50054:
fps_rx_word_cnt_lo 00000000

```

BAL registers

=====

```

0x81c57000: bal_desired_buf 00000000 0x81c57004:
bal_alloc_buf 00000000
0x81c57008: bal_busy_buf 00000000 0x81c5700c:
bal_usable_buf 00000000
0x81c57010: bal_max_bor_buf 00000000
0x81c57014: bal_busy_buf_thresh 00000002

```

TXQ registers

=====

```

0x81c53004: txq_phys_port_ctl 00420000
0x81c53050: txq_link_skew 00000000
0x81c53068: txq_cr_lk_dttm_intr_sts [00] 00000000 00000000
0x81c53070: txq_cr_lk_dttm_intr_en [00] 00000000 00000000
0x81c53024: txq_disc_frm_trap_cnt 00000014

```

FDS registers

=====

```

0x81c54000: fds_rxf_ctl 00000002 0x81c54004:
fds_rxf_wait_thresh 00000909

```



```

0x81c54018: fds_rxf_first_error      00000000    0x81c5401c:
fds_rxf_first_error_info00000000
0x81c54020: fds_rxf_inout_pkt_cnt      00000000
0x81c54008: fds_rxf_err_int_status    00000000    0x81c54024:
fds_rxf_fifo_status      00888888
0x81c55000: fds_txf_ctl                0000003a    0x81c55004:
fds_txf_wait_ifg_thresh 00a00106
0x81c55008: fds_txf_err_int_status    00000000    0x81c55024:
fds_txf_fifo_status      00088888
0x81c5502c: fds_txf_bbc_scs          00000000

```

Logical TXQ registers

=====

```

0x81c53000: txq_log_port_ctl          00000002    0x81c53008:
txq_port_status          00000000
0x81c5300c: txq_todo_flags           [00] 00000000 00000000
0x81c53014: txq_spd_match_desc       [00] 00000000 00000000 00000000
00000000
0x81c53024: txq_spd_match_desc       [04] 00000014
0x81c53028: txq_vc_weight            [00] 01010101 01010101 01010101
01010101
0x81c53038: txq_vc_weight            [04] 01010101 01010101 01010101
01010101
0x81c53048: txq_vc_weight            [08] 01010101 00010101
0x81c53054: txq_cong_dttm_ctrl       00000000
0x81c53058: txq_cong_dttm_intr_sts  [00] 00000000 00000000
0x81c53060: txq_cong_dttm_intr_en   [00] 00000000 00000000
0x81c53078: txq_bw_limit_en_reg     [00] 00000000 00000000
0x81c53080: txq_bw_gua_en_reg       [00] 00000000 00000000
0x81c53088: txq_vc_group             [00] 03030300 03030303 03030303
03030303
0x81c53098: txq_vc_group             [04] 03030303 03030303 03030303
03030303
0x81c530a8: txq_vc_group             [08] 03030303 03030303 00000000
00000000
0x81c530b0: txq_bw_thresh_group     [00] 00000000 00000000 00000000
00000000
0x81c530c0: txq_bw_thresh_group     [04] 00000000 00000000 00000000
00000000
0x81c530d0: txq_bw_thresh_group     [08] 00000000 00000000 00000000
00000000
0x81c530e0: txq_bw_thresh_group     [12] 00000000 00000000 00000000
00000000
0x81c530f0: txq_bw_thresh_group     [16] 00000000 00000000 00000000
00000000
0x81c53100: txq_bw_thresh_group     [20] 00000000 00000000 00000000
00000000
0x81c53110: txq_bw_thresh_group     [24] 00000000 00000000 00000000
00000000
0x81c53120: txq_bw_thresh_group     [28] 00000000 00000000 00000000
00000000
0x81c53130: txq_bw_thresh_group     [32] 00000000 00000000 00000000
00000000
0x81c53140: txq_bw_thresh_group     [36] 00000000 00000000 00000000

```

00000000

txq Congestion detection Statistics RAM

=====

| | | |
|--------------------|----------|--------------------|
| 0x81090640: vc[0] | 00000000 | 0x81090644: vc[1] |
| 00000000 | | |
| 0x81090648: vc[2] | 00000000 | 0x8109064c: vc[3] |
| 00000000 | | |
| 0x81090650: vc[4] | 00000000 | 0x81090654: vc[5] |
| 00000000 | | |
| 0x81090658: vc[6] | 00000000 | 0x8109065c: vc[7] |
| 00000000 | | |
| 0x81090660: vc[8] | 00000000 | 0x81090664: vc[9] |
| 00000000 | | |
| 0x81090668: vc[10] | 00000000 | 0x8109066c: vc[11] |
| 00000000 | | |
| 0x81090670: vc[12] | 00000000 | 0x81090674: vc[13] |
| 00000000 | | |
| 0x81090678: vc[14] | 00000000 | 0x8109067c: vc[15] |
| 00000000 | | |
| 0x81090680: vc[16] | 00000000 | 0x81090684: vc[17] |
| 00000000 | | |
| 0x81090688: vc[18] | 00000000 | 0x8109068c: vc[19] |
| 00000000 | | |
| 0x81090690: vc[20] | 00000000 | 0x81090694: vc[21] |
| 00000000 | | |
| 0x81090698: vc[22] | 00000000 | 0x8109069c: vc[23] |
| 00000000 | | |
| 0x810906a0: vc[24] | 00000000 | 0x810906a4: vc[25] |
| 00000000 | | |
| 0x810906a8: vc[26] | 00000000 | 0x810906ac: vc[27] |
| 00000000 | | |
| 0x810906b0: vc[28] | 00000000 | 0x810906b4: vc[29] |
| 00000000 | | |
| 0x810906b8: vc[30] | 00000000 | 0x810906bc: vc[31] |
| 00000000 | | |
| 0x810906c0: vc[32] | 00000000 | 0x810906c4: vc[33] |
| 00000000 | | |
| 0x810906c8: vc[34] | 00000000 | 0x810906cc: vc[35] |
| 00000000 | | |
| 0x810906d0: vc[36] | 00000000 | 0x810906d4: vc[37] |
| 00000000 | | |
| 0x810906d8: vc[38] | 00000000 | 0x810906dc: vc[39] |
| 00000000 | | |

Logical STS registers

=====

| | |
|----------------------------------|----------|
| 0x81584804: sts_ftb_type1_miss | 00000000 |
| 0x81584808: sts_ftb_type2_miss | 00000000 |
| 0x8158480c: sts_ftb_type6_miss | 00000000 |
| 0x81584810: sts_hard_zoning_miss | 00000000 |
| 0x81584814: sts_lun_zoning_miss | 00000000 |
| 0x8158481c: sts_unroutable | 00000000 |

```

0x81581834: sts_rte_cl2          00000000    0x81581838:
sts_rte_cl3          00000000    0x8158183c: sts_rte_link_ctl
00000000            0x81584828: sts_tx_timeout      00000000

```

Logical STS filter registers

=====

```

0x81584780: stsflt_trig [00] 00000000 00000000 00000000
00000000
0x81584790: stsflt_trig [04] 00000000 00000000 00000000
00000000
0x815847a0: stsflt_trig [08] 00000000 00000000 00000000
00000000
0x815847b0: stsflt_trig [12] 00000000 00000000 00000000
00000000
0x815847c0: stsflt_trig [16] 00000000 00000000 00000000
00000000
0x815847d0: stsflt_trig [20] 00000000 00000000 00000000
00000000
0x815847e0: stsflt_trig [24] 00000000 00000000 00000000
00000000
0x815847f0: stsflt_trig [28] 00000000 00000000 00000000
00000000
0x81584800: stsflt_trig [32]

```

Logical STS discard registers

=====

```

0x81581e88: disc_mcast_wka          00000000    0x81581e8c:
disc_inv_did          00000000
0x81581e90: disc_cl1_cl4            00000000    0x81581e94:
disc_sid_chk_fail     00000000
0x81581e98: disc_inv_dom_egid_txpt 00000000    0x81581e9c:
disc_vft_hop_cnt_1    00000000
0x81581ea0: disc_classf             00000000    0x81581ea4:
disc_fcp_cdb_inv       00000000
0x81581ea8: disc_vfid_trap_enabled 00000000    0x81581eac:
disc_vfid_hdr_chk_fail 00000000
0x81581eb0: disc_shim_cksum_fail    00000000    0x81581eb4:
disc_fed_edit_cmd_err 00000000
0x81581eb8: disc_ftb_vm_mode        00000000    0x81581ebc:
disc_ftb_agnt2_miss    00000000
0x81581ec0: disc_ecb_reserved       00000000    0x81581ec4:
disc_ecb_de_pad_err    00000000
0x81581ec8: disc_ecb_de_tag_err     00000000    0x81581ecc:
disc_ecb_de_seq_err    00000000
0x81581ed0: disc_ecb_err            00000000    0x81581ed4:
disc_ftb_type4_match    00000000
0x81581ed8: disc_fcp_rsp_ftb_type4 00000000    0x81581edc:
disc_ftb_type5_match    00000000
0x81581ee0: disc_ftb_type3_match    00000000    0x81581ee4:
disc_els_ftb_type3     00000000
0x81581ee8: disc_ftb_type1_match    00000000    0x81581eec:
disc_els_rsp_ex_port    00000000
0x81581ef0: disc_inv_drp_dps        00000000    0x81581ef4:
disc_did_lookup_miss    00000000

```

```

0x81581ef8: disc_ftb_type2_match      00000000      0x81581efc:
disc_trpd_plogi_pdisc    00000000
0x81581f00: disc_type2_lookup_miss    00000000      0x81581f04:
disc_ftb_type6_match     00000000
0x81581f08: disc_els_rep_ex_port      00000000      0x81581f0c:
disc_els_sid_lkup_bit1   00000000
0x81581f10: disc_els_sid_lkup_bit0    00000000      0x81581f14:
disc_bls_frm_trap_bit1   00000000
0x81581f18: disc_ftb_token_err        00000000      0x81581f1c:
disc_asic_internal_err   00000000
0x81581f20: disc_hard_zone_miss       00000000      0x81581f24:
disc_lun_zone_miss       00000000
0x81581f28: discflt_frame_disc        00000000      0x81581f2c:
discflt_parity_err       00000000
0x81581f30: disc_frame_marked_du      00000000      0x81581f34:
disc_frame_marked_to     00000000
0x81581f38: disc_lkup_rte_prty_err    00000000

```

portstatsshow 51

```

stat_wtx          0          4-byte words transmitted
stat_wrx          0          4-byte words received
stat_ftx          0          Frames transmitted
stat_frx          0          Frames received
stat_c2_frx       0          Class 2 frames received
stat_c3_frx       0          Class 3 frames received
stat_lc_rx        0          Link control frames
received
stat_mc_rx        0          Multicast frames
received
stat_mc_to        0          Multicast timeouts
stat_mc_tx        0          Multicast frames
transmitted
tim_txcrd_z       0          Time TX Credit Zero
(2.5Us ticks)
tim_txcrd_z_vc   0- 3: 0          0          0          0
tim_txcrd_z_vc   4- 7: 0          0          0          0
tim_txcrd_z_vc   8-11: 0         0          0          0
tim_txcrd_z_vc  12-15: 0         0          0          0
lat_tot_pkt_vc   0- 3: 1          1          1          1
lat_tot_pkt_vc   4- 7: 1          1          1          1
lat_tot_pkt_vc   8-11: 1         1          1          1
lat_tot_pkt_vc  12-15: 1         1          1          1
lat_hi_time_vc   0- 3: 0          0          0          0
lat_hi_time_vc   4- 7: 0          0          0          0
lat_hi_time_vc   8-11: 0         0          0          0
lat_hi_time_vc  12-15: 0         0          0          0
lat_lo_time_vc   0- 3: 1          1          1          1
lat_lo_time_vc   4- 7: 1          1          1          1
lat_lo_time_vc   8-11: 1         1          1          1
lat_lo_time_vc  12-15: 1         1          1          1
max_latency_vc   0- 3: 1          1          1          1
max_latency_vc   4- 7: 1          1          1          1
max_latency_vc   8-11: 1         1          1          1

```

| | | | | | |
|------------------------------|------------|-----|-----|----------|--------------------------|
| max_latency_vc 12-15: | 1 | 1 | 1 | 1 | |
| latency_dma_ts | 09-09-2024 | UTC | Mon | 08:47:25 | TXQ |
| Latency DMA TimeStamp | | | | | |
| fec_cor_detected | 0 | | | | Count of blocks that |
| were corrected by FEC | | | | | |
| fec_uncor_detected | 0 | | | | Count of blocks that |
| were left uncorrected by FEC | | | | | |
| er_enc_in | 0 | | | | Encoding errors inside |
| of frames | | | | | |
| er_crc | 0 | | | | Frames with CRC errors |
| er_trunc | 0 | | | | Frames shorter than |
| minimum | | | | | |
| er_toolong | 0 | | | | Frames longer than |
| maximum | | | | | |
| er_bad_eof | 0 | | | | Frames with bad end-of- |
| frame | | | | | |
| er_enc_out | 0 | | | | Encoding error outside |
| of frames | | | | | |
| er_bad_os | 0 | | | | Invalid ordered set |
| er_pcs_blk | 0 | | | | PCS block errors |
| er_rx_c3_timeout | 0 | | | | Class 3 receive frames |
| discarded due to timeout | | | | | |
| er_tx_c3_timeout | 0 | | | | Class 3 transmit frames |
| discarded due to timeout | | | | | |
| er_unroutable | 0 | | | | Frames that are |
| unroutable | | | | | |
| er_unreachable | 0 | | | | Frame with unreachable |
| destination | | | | | |
| er_other_discard | 0 | | | | Other discards |
| er_type1_miss | 0 | | | | frames with FTB type 1 |
| miss | | | | | |
| er_type2_miss | 0 | | | | frames with FTB type 2 |
| miss | | | | | |
| er_type6_miss | 0 | | | | frames with FTB type 6 |
| miss | | | | | |
| er_zone_miss | 0 | | | | frames with hard zoning |
| miss | | | | | |
| er_lun_zone_miss | 0 | | | | frames with LUN zoning |
| miss | | | | | |
| er_crc_good_eof | 0 | | | | Crc error with good eof |
| er_inv_arb | 0 | | | | Invalid ARB |
| er_single_credit_loss | 0 | | | | Single vcrdy/frame loss |
| on link | | | | | |
| er_multi_credit_loss | 0 | | | | Multiple vcrdy/frame |
| loss on link | | | | | |
| other_credit_loss | 0 | | | | Link timeout/complete |
| credit loss | | | | | |
| phy_stats_clear_ts | 09-06-2024 | UTC | Fri | 08:30:19 | Timestamp of |
| phy_port stats clear | | | | | |
| lgc_stats_clear_ts | 09-06-2024 | UTC | Fri | 08:30:19 | Timestamp of |
| lgc_port stats clear | | | | | |
| fec_corrected_rate | 0 | | | | FEC Corrected blocks per |
| second | | | | | |

```

portstats64show 51
stat64_wtx      0      top_int : 4-byte words transmitted
                0      bottom_int : 4-byte words transmitted
stat64_wrx      0      top_int : 4-byte words received
                0      bottom_int : 4-byte words received
stat64_ftx      0      top_int : Frames transmitted
                0      bottom_int : Frames transmitted
stat64_frx      0      top_int : Frames received
                0      bottom_int : Frames received
stat64_c2_frx   0      top_int : Class 2 frames received
                0      bottom_int : Class 2 frames received
stat64_c3_frx   0      top_int : Class 3 frames received
                0      bottom_int : Class 3 frames received
stat64_lc_rx    0      top_int : Link control frames received
                0      bottom_int : Link control frames
received
stat64_mc_rx    0      top_int : Multicast frames received
                0      bottom_int : Multicast frames received
stat64_mc_to    0      top_int : Multicast timeouts
                0      bottom_int : Multicast timeouts
stat64_mc_tx    0      top_int : Multicast frames transmitted
                0      bottom_int : Multicast frames
transmitted
tim64_rdy_pri   0      top_int : Time R_RDY high priority
                0      bottom_int : Time R_RDY high priority
tim64_txcrd_z   0      top_int : Time BB_credit zero
                0      bottom_int : Time BB_credit zero
er64_enc_in     0      top_int : Encoding errors inside of
frames
                0      bottom_int : Encoding errors inside of
frames
er64_crc        0      top_int : Frames with CRC errors
                0      bottom_int : Frames with CRC errors
er64_trunc      0      top_int : Frames shorter than minimum
                0      bottom_int : Frames shorter than minimum
er64_toolong    0      top_int : Frames longer than maximum
                0      bottom_int : Frames longer than maximum
er64_bad_eof    0      top_int : Frames with bad end-of-frame
                0      bottom_int : Frames with bad end-of-
frame
er64_enc_out    0      top_int : Encoding error outside of
frames
                0      bottom_int : Encoding error outside of
frames
er64_disc_c3    0      top_int : Class 3 frames discarded
                0      bottom_int : Class 3 frames discarded
er64_pcs_blk    0      top_int : PCS block errors
                0      bottom_int : PCS block errors
stat64_rateTxFrame 0      Tx frame rate (fr/sec)
stat64_rateRxFrame 0      Rx frame rate (fr/sec)
stat64_rateTxPeakFrame 0    Tx peak frame rate (fr/sec)
stat64_rateRxPeakFrame 0    Rx peak frame rate (fr/sec)
stat64_rateTxWord  0      Tx Word rate (words/sec)
stat64_rateRxWord  0      Rx Word rate (words/sec)

```

```

stat64_rateTxPeakWord  0          Tx peak Word rate (words/sec)
stat64_rateRxPeakWord  0          Rx peak Word rate (words/sec)
stat64_PRJTFrames      0          top_int : Number of PRJT frames
returned to this port
                                0          bottom_int : Number of PRJT
frames returned to this port
stat64_PBSYFrames      0          top_int : Number of PBSY frames
returned to this port
                                0          bottom_int : Number of PBSY
frames returned to this port
stat64_inputBuffersFull 0          top_int : Number of occurrences
when all input buffers full
                                0          bottom_int : Number of
occurrences when all input buffers full
stat64_rxClass1Frames  0          top_int : Number of class 1
frames received
                                0          bottom_int : Number of class 1
frames received
stat64_aveTxFrameSize  0          Average Tx Frame size
stat64_aveRxFrameSize  0          Average Rx Frame size
Lr_in                   0          top_int
                                0          bottom_int
Ols_in                  0          top_int
                                0          bottom_int
Lr_out                  0          top_int
                                0          bottom_int
Ols_out                 0          top_int
                                0          bottom_int
Link_failure            0          top_int
                                0          bottom_int
Invalid_CRC             0          top_int
                                0          bottom_int
Invalid_word            0          top_int
                                0          bottom_int
Protocol_err            0          top_int
                                0          bottom_int
Loss_of_sig             0          top_int
                                0          bottom_int
Loss_of_sync            0          top_int
                                0          bottom_int
er_bad_os               0          top_int : Invalid ordered set
                                0          bottom_int: Invalid ordered set

```

```

portrouteshow 51
port address ID: 0x013300
external unicast routing table:
  0: Embedded
 255: Embedded
internal unicast routing table:
  0: Embedded

```

```

portcamshow 51
-----

```

| Port | SID used | DID used | SID entries | DID entries |
|------|----------|----------|-------------|-------------|
| 51 | 0 | 0 | 000000 | 000000 |

ptbufshow, ptcreditshow, ptdatashow, ptstatsshow 51

S:

S:VF Enable: 1

S:

S:C4 Global Variable:

S:-----

S:trace_stop: 0

S:

S:C4 Phy Data Pointers: c4_phyp = 0xb6ac6180

S:-----

S:tnodep 0xbb8367e0 pt

0x4302800a

S:proto_phyp 0xb8807b40 phy_cfg

0xb6ac8000

S:c4_chp 0x97e28000 c4_lgcp

0x97f70000

S:c4_phy_regp 0x81c50000 proc_dir

0xb8516320

S:-----

S:magic_id 0xc4345678 num_port_timer 12

S:prev_if_id 0x4302000a S:ftx 0

0x00000000

S:initialized 0 port_idx 10

S:ui_idx 51 slot_no

0

S:blade_idx 10 sw_usr_ports 400

S:unused 0 intr_debounced

0

S:aec_status 0x0 reason_code

0

S:debug 0x00000004 debug_trc_line 0

S:rxbuf_list_head 0xffffffff rxbuf_list_tail

0xffffffff

S:isAePort 0 port_misc_data

0

S:num_fault1_rx_disc 0 num_fault2_rx_disc 0

S:p_lli_cause0 0 p_sig_regained 0

S:p_sync_regained 0 enc_out

0x0

S:cached_fps_status 0 cached_sts_status 0

S:cached_er_crc_good_eof 0

S:cached_er_bad_os 0 cached_er_too_long 0

S:cached_er_trunc 0

cached_tot_er_crc_good_eof 0

S:num_pt_excess_intr 0 num_no_fid 0

S:num_fault1_cnt 0 num_fault2_cnt

0


```

S:num_fault_lip          0          num_fault_lli          0
S:num_fault_rx_fifo     0          num_fault_hss          0
S:num_fault_bwait       0          lli_intr_prim
  0
S:num_sw_link_to        0
be_link_err_mon_count   0
S:ecb_enc_enabled       0          ecb_comp_enabled
  0
S:ecb_rsv_enc           0          ecb_rsv_comp          0
S:ecb_enc_bm            0x0       ecb_key_index
0xffffffff
S:fab_idx                4
S:num_be_lto            0          lto_count_reset_intvl
  0
S:lr_count_reset_intvl  0          num_be_lr
  0
S:num_fault_qsfm        0          check_lto
  0
S:credit_loaded         0          num_credit_overrun
  0
S:fec_enabled           0x0       fec_los_to_flag       0x0
S:phy_stats_clear_ts    0          pcs_err_online
  1725611419
S:pcs_err_light_det     0          pcs_err_ignore
  0
S:pcs_blk_err           0          pcs_hiber              0
S:phy_port_status       0          ecb_enc_lr_count
  0
S:dport_mode            0          avoid_lto_det         0
S:sn_debounced          0x0       sn_started_kr_reqd    0
S:major_timer_started   0x0       ready_bm              0x0
S:parln_1_bm            0x0       parln_0_bm            0x0
S:be_los_of_sync_event_intvl 0
be_los_of_sync_event    0
S:errataPtenable_cntr   0          errataPoll_cntr
  0
S:jda_rx_sig_loss_det   0          jda_rx_sig_loss_cnt
  0
S:encrypt_blk_error     0
S:
S:      c4_trunk
S:=====
S:mark_ts                0x0       deskew                0x0
S:master_phyp            0x0
S:
S:adelay[00]: 0x00000000 0x00000000 0x00000000 0x00000000
S:adelay[04]: 0x00000000 0x00000000 0x00000000 0x00000000
S:
S:      c4_buf
S:=====
S:tx_csc                  0          rx_csc
  0
S:ld_vc_credits          0          tx_flag                0x0
S:alloc_buffers          0          req_buffers            0

```

```

S:est_buffers          20          ld_use_est          0
S:bb_sc_n              0          rx_bb_sc_n
0
S:data_cr              5          nondata_cr
6
S:cr_enable            0
S:ld_nondata_cr       6          tnodep
0xbb8368c0
S:tx_credits[0] 0      0      0      0      0      0      0      0
S:tx_credits[8] 0      0      0      0      0      0      0      0
S:tx_credits[16]      0      0      0      0      0      0      0      0
S:tx_credits[24]      0      0      0      0      0      0      0      0
S:tx_credits[32]      0      0      0      0      0      0      0      0
S:rx_credits[0] 0      0      0      0      0      0      0
S:rx_credits[8] 0      0      0      0      0      0      0
S:rx_credits[16]      0      0      0      0      0      0      0      0
S:rx_credits[24]      0      0      0      0      0      0      0      0
S:rx_credits[32]      0      0      0      0      0      0      0      0
S:tx_mbc[0]           0      0      0      0      0      0      0
S:tx_mbc[8]           0      0      0      0      0      0      0
S:tx_mbc[16]          0      0      0      0      0      0      0
S:tx_mbc[24]          0      0      0      0      0      0      0
S:tx_mbc[32]          0      0      0      0      0      0      0
S:rx_mbc[0]           0      0      0      0      0      0      0
S:rx_mbc[8]           0      0      0      0      0      0      0
S:rx_mbc[16]          0      0      0      0      0      0      0
S:rx_mbc[24]          0      0      0      0      0      0      0
S:rx_mbc[32]          0      0      0      0      0      0      0

```

S:
S:C4 Chip Variables: c4_phyp->c4_chp = 0x97e28000

```

S:-----
-----
S:version = 2.1
S:magic_id             0xc4234567      init_state          0x8
S:reset_reg_mem       0x1
S:ch_int0_en_bm       0x0          intr0_cause         0x0
S:ch_int1_en_bm       0x0          intr1_cause         0x0
S:ch_int2_en_bm       0x0          intr2_cause         0x0
S:ch                  0x43010080      ch_cfg
0xb7013ba0
S:raslog_hdl.hndl     0x0          obj_halted          0x0
S:c4_chip_regp        0x80000000      c4_fpg_regp
0x81800000
S:num_chip_timer      0x5
S:hi_task_bm          0x0          lo_task_bm          0x0
S:c4_deferq.q_head    0x0          c4_deferq.q_tail   0x0
S:c4_tmrq.q_head      0x0          c4_tmrq.q_tail     0x0
slot_no              0
S:chip_inst           0          chip_idx            0
S:pll_initialized     1
pll_serdes_initialized 1
S:init_tries          0          init_ptEnableBM
0xba01b488
S:tick_polling        0xb980c9c0      sec_polling

```

```

0xb980c960
S:bb_fid 129
S:ecb_key_bm[0] 0x0 ecb_key_bm[1] 0x0
S:ecb_key_bm[2] 0x0 ecb_key_bm[3] 0x0
S:is_chip_enc_enabled 0
is_chip_comp_enabled 0x0
S:ftb_rsrcp->ftb_flags 0x0 act_rsrcp->act_flag 0x1
S:lue_rsrcp->lue_flags[0] 0x0 lue_rsrcp->
>lue_flags[1] 0x0
S:c4_phyp[00]: 0xb6ab0000 0xb6ab2080 0xb6ab4100 0xb6ab6180
S:c4_phyp[04]: 0xb6ab9040 0xb6abb0c0 0xb6abd140 0xb6ac0000
S:c4_phyp[08]: 0xb6ac2080 0xb6ac4100 0xb6ac6180 0xb6ac9040
S:c4_phyp[12]: 0xb6acb0c0 0xb6acd140 0xb6ad0000 0xb6ad2080
S:c4_phyp[16]: 0xb6ad4100 0xb6ad6180 0xb6ad9040 0xb6adb0c0
S:c4_phyp[20]: 0xb6add140 0xb6ae0000 0xb6ae2080 0xb6ae4100
S:c4_phyp[24]: 0xb6ae6180 0xb6ae9040 0xb6aeb0c0 0xb6aed140
S:c4_phyp[28]: 0xb6af0000 0xb6af2080 0xb6af4100 0xb6af6180
S:c4_phyp[32]: 0xb6af9040 0xb6afb0c0 0xb6afd140 0xb6b00000
S:c4_phyp[36]: 0xb6b02080 0xb6b04100 0xb6b06180 0xb6b09040
S:c4_phyp[40]: 0xb6b0b0c0 0xb6b0d140 0xb6b10000 0xb6b12080
S:c4_phyp[44]: 0xb6b14100 0xb6b16180 0xb6b19040 0xb6b1b0c0
S:c4_phyp[48]: 0xb6b1d140 0xb6b20000 0xb6b22080 0xb6b24100
S:c4_phyp[52]: 0xb6b26180 0xb6b29040 0xb6b2b0c0 0xb6b2d140
S:c4_phyp[56]: 0xb6b30000 0xb6b32080 0xb6b34100 0xb6b36180
S:c4_phyp[60]: 0xb6b39040 0xb6b3b0c0 0xb6b3d140 0xb6b40000
S:c4_lgcp[00]: 0x97f48000 0x97f4c000 0x97f50000 0x97f54000
S:c4_lgcp[04]: 0x97f58000 0x97f5c000 0x97f60000 0x97f64000
S:c4_lgcp[08]: 0x97f68000 0x97f6c000 0x97f70000 0x97f74000
S:c4_lgcp[12]: 0x97f78000 0x97f7c000 0x97f80000 0x97f84000
S:c4_lgcp[16]: 0x97f88000 0x97f8c000 0x97f90000 0x97f94000
S:c4_lgcp[20]: 0x97f98000 0x97f9c000 0x97fa0000 0x97fa4000
S:c4_lgcp[24]: 0x97fa8000 0x97fac000 0x97fb0000 0x97fb4000
S:c4_lgcp[28]: 0x97fb8000 0x97fbc000 0x97fc0000 0x97fc4000
S:c4_lgcp[32]: 0x97fc8000 0x97fcc000 0x97fd0000 0x97fd4000
S:c4_lgcp[36]: 0x97fd8000 0x97fdc000 0x97fe0000 0x97fe4000
S:c4_lgcp[40]: 0x97fe8000 0x97fec000 0x97ff0000 0x97ff4000
S:c4_lgcp[44]: 0x97ff8000 0x97ffc000 0x8e000000 0x8e004000
S:c4_lgcp[48]: 0x8e008000 0x8e00c000 0x8e010000 0x8e014000
S:c4_lgcp[52]: 0x8e018000 0x8e01c000 0x8e020000 0x8e024000
S:c4_lgcp[56]: 0x8e028000 0x8e02c000 0x8e030000 0x8e034000
S:c4_lgcp[60]: 0x8e038000 0x8e03c000 0x8e040000 0x8e044000
S:chip_timers[00]: 0xb980c720 0xb980c780 0xb980c7e0 0xb980c840
S:chip_timers[04]: 0xb980c8a0 0xb980c900
S:disc_trap_enable_required 0x0 rxlp_disc_log_stop
0x0
S:curr_rxlp_frm_cnt 0x0 curr_rxlp_disc_frm_cnt 0x0
S:sw_disc_frm_cnt 0x0 last_disc_frm_cnt 0x0
S:txq_nopop_pr_cnt 0x0 pollErrataDfe_ptBM
0xba01b4b0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][0] 0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][1] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][2] 0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][0] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][1] 0x0

```

```

ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][2] 0x0
S:
S:C4 Logical Port Variables
S:-----
-----
S:c4_lgc_regp          0x81c50000
S:c4_phyp:
S:      0xb6ac6180      0x0          0x0          0x0

S:      0x0          0x0          0x0          0x0

S:master_phyp          0xb6ac6180      if_id
0x4302000a
S:min_phyp              0x0          max_phyp          0x0
S:num_phy_ports        1          lgc_num          10
S:num_iu_to             0          sw_txq_bm
0
S:port_fid             129          unused          0
S:port_group           1          lgc_stats_clear_ts
1725611419
S:domain_tbl_sel       0          area_tbl_sel
0
S:egid_tbl_sel         0
S:serv_lo_bm           0x0
S:
S:Proto Phy Variables:
S:-----
-----
S:magic_id              0xc4123456      asic_phyp
0xb6ac6180
S:port_id               0x4302800a      phy_cfg
0xb6ac8000
S:upsm_hdl              0xb8012780      physm_hdl
0xb8012500
S:ov_snsn_hdl           0xb80123c0      sw_snsn_hdl
0xb8012460
S:ov_lksm_hdl           0xb80125a0      sw_lksm_hdl
0xb8012640
S:trksm_hdl             0xb80126e0      lr_flag          0x0
S:lr_active             0x0          qsfp_txrx_rate_sel
0x0
S:
S:UPSM      UP00: UPST_PORT_DISABLED      --> UP00: UPST_PORT_DISABLED
S:SNSM(OV)  SN00: OV_SNST_STOPPED          --> SN00: OV_SNST_STOPPED
S:SNSM(SW)  SW00: SW_SNST_STAGE_WS        --> SW00: SW_SNST_STAGE_WS
S:PHYSM     PP00: PHYST_STOPPED           --> PP00: PHYST_STOPPED
S:LKSM(OV)  LK00: OV_LKST_INACTIVE        --> LK00: OV_LKST_INACTIVE
S:LKSM(SW)  SW13: INACTIVE                --> SW13: INACTIVE
S:TRKSM     TRK0: TRKST_INIT              --> TRK0: TRKST_INIT
S:
S:physm variables:
S:-----
-----
S:proto_phyp          0xb8807b40      physm_hdl

```

```

0xb8012500
S:force_offline          0          copper          0
S:fault_reason          0: UNKNOWN
S:phy_media_present      0
S:
S:sns variables:
S:-----
-----
S:speed                  0xff          proto_phyp
0xb8807b40
S:hw_sn_tries_left      0x0          sw_sn_tries_left  0x0
S:curr_txsp_count       0x0
S:tx_max                 0x0          curr_tx_indx
          0x0
S:curr_tx                0x0          curr_rxsp_count
          0x0
S:rx_max                 0x0          curr_rx_indx
          0x0
S:curr_rx                0x0          rx_mem
          0x0
S:rxsp_rec_count        0x0
S:nc_start               0x0          tx_start          0x0
S:sync_start            0x0          sync_present      0x0
S:diag_auto              0x0          diag_speed        0xff
S:striped_wd_tov        3000         hw_wd_tov
          3000
S:step                   0x0          qsfp28_speed_mode
          0x0
S:qsfp_mode0_hw_sn_tries_left  0x0
S:qsfp_mode1_hw_sn_tries_left  0x0
S:
S:lksm variables:
S:-----
-----
S:proto_phyp            0xb8807b40   ov_lksm_hdl
0xb80125a0
sw_lksm_hdl             0xb8012640
num_lf1                 0
S:hw_link_tries_left    0          sw_link_tries_left  0
S:buf_ptype             0x0          stored_entry_state  0x6
S:handshake_owner       0x0          mark_unsent
          0x0
S:busybuf_stuck         0x0          lr_wait           0x0
S:
S:trksm variables:
S:-----
-----
S:Not a trunk port
S:
S:upsm variables:
S:-----
-----
S:proto_phyp            0xb8807b40   upsm_hdl
0xb8012780

```

```

S:bb_credits          0          port_beacon          0
S:port_diag_flag     0          force_offline
  0
S:port_fault_rsn     0: PORT_NO_FAULT
S:retry_init_rsn     0: UNKNOWN
S:linit_reason        0          linit_result         0
S:ie_fctl_mode        0          fec_in_sync_tries_left 0
S:retry_sn_fail_init 0
retry_link_fail_init 0
S:excess_lr_count    0
S:
S:c4_ch_cfg
S:-----
-----
S:c4_desc_ring_size  256      292      256      256      292
292      2      292      292
S:thresh_def         0          16         1          0
S:intr_tries         500          cmem_pattern
0xdeadbeef
S:cmem_pattern_upwd  2          cmem_init_time      16
S:cmem_init_tries    5
S:ctrl_par_thresh    2          data_par_thresh
  4
S:cam_par_thresh     4          buf_loss_thresh
  12
S:crit_par_thresh    2          non_crit_par_thresh
  6
S:pci_abort_thresh   10          pci_err_thresh      5
S:excess_chintr_thresh 8          sw_err_thresh       20
S:err_sample_period  300          intr_sleep
20000
S:frame_timeout      2500          proxy_dev           16384
S:vf_route           81920          qos                 2048
S:stats 2048         f_redirect         2048
S:rsp_trap           2048          lun_zoning          20480
S:area_mode          0          ftb_max_loop[0]    0
S:ftb_max_loop[1]    6          ftb_max_loop[2]    9
S:ftb_max_loop[3]    10         ftb_max_loop[4]    10
S:ftb_max_loop[5]    5          ftb_max_loop[6]    6
S:ftb_seg_size[0]    0          ftb_seg_size[1]
16384
S:ftb_seg_size[2]    65536         ftb_seg_size[3]
16384
S:ftb_seg_size[4]    16384         ftb_seg_size[5]
65536
S:ftb_seg_size[6]    16384         ftb_seg_base[0]    0
S:ftb_seg_base[1]    0          ftb_seg_base[2]
65536
S:ftb_seg_base[3]    16384         ftb_seg_base[4]
32768
S:ftb_seg_base[5]    131072        ftb_seg_base[6]
49152
asic_err_monitor_period1 300
asic_err_monitor_period2 86400

```

```

zone_chk_to_poll_period 25
zone_chk_class2_reject_tov          220
S:
S:c4_phy_cfg
S:-----
-----
S:version = 2.1
S:pt          0x4302800a          fab_ptr
0x9a800000
S:fabattr          0x9a8000d4          fab_iop
          0x9a800050
S:cfgbm          0xbb836624          port_ctrl
0xb6ac8018
S:pcap.pcap_bm          0x8d215547          pcap.pcap2_bm
0x2588289
S:pcap.pcap3_bm          0x1bebe0c
ui_idx          51          S:slot_no
          0
is_icl          0          S:sw_usr_ports          400
S:neg_speed          0 0 0 0 0 0
S:my_domain          0x1          port_mode          0x0
S:hw_sn_maxtries          100          sw_sn_maxtries
          0
S:hw_link_maxtries          10          sw_link_maxtries          5
S:rx_cyc_tov          28          rttov          300
S:bufrdy_tov          300          busybuf_tov          286
S:mark_tov          300          lksm_tov          3000
S:buf_dealloc_wait          4          hw_wd_tov          3000
S:hw_lk_train_tov          540          hw_lk_test_tov
          150
S:syswait_tx_12_lips          1          lip_rx_tov          55
S:al_time_tov          15          lp_tov          2000
S:intr_tries_port          500          intr_mod_debounce
          250
S:intr_lsrflt_debounce          500          intr_efifo_debounce          100
S:port_no_fid          3          excess_ptintr_thresh          8
S:port_fault1_thresh          100          port_fault1_spur_thresh          250
S:port_fault1_disc_thresh          500
port_fault1_disc_spur_thresh          1000
S:port_fault2_thresh          5          losync_tov          100
S:port_sw_link_to          15          en_8g_scramble
          1
frc_hw_sn_mode          0x1
S:enc_poll_thresh          0          fec_enable
          0
S:fec_in_sync_to          50          fec_in_sync_try_max
          4
S:port_be_lto_threshold          100          port_be_lr_threshold
          2
S:be_cr_in_sync_to          5
port_credit_overrun_thresh          10
S:jda_sfp_losig_tov          400
jda_sfp_losig_try_max          30
S:striped_wd_tov          3000

```

```

no_sync_debounce          1200
S:
S:      fab_iop
S:=====
S:fab_iop->interop_mode 0x0          fab_iop->lab_mode          0x0
S:fab_iop->fl_bbc          0x0          fab_iop->fl_fan
      0x0
S:fab_iop->fl_cls          0x4          fab_iop->fl_rscn
      0x0
S:fab_iop->domain_id_offset 0x60          fab_iop-
>mcmt_fabric_mode      0x0
S:fab_iop->mcmt_default_zone          0x0          fab_iop-
>mcmt_safe_zone        0x0
S:
S:      port_ctrl
S:=====
S:port_ctrl.port_type      1          port_ctrl.port_grp      1
S:port_ctrl.port_number 51          port_ctrl.vc_mode      1
S:
S:      port_ctrl.lcap
S:=====
S:has_serdes          0          has_media          1
S:topology          1          skip_nego          0
S:skip_pnego          0          skip_init_event      0
S:en_shim          0          speed_neg
      1
S:loop_back          0          num_speeds          5
S:fec_enable          0
S:
S:      port_ctrl.speed_list array
S:=====
S:speed_list[0].auto_neg  1          speed_list[0].lnk_speed 0x0000000a
S:speed_list[1].auto_neg  1          speed_list[1].lnk_speed 0x00000008
S:speed_list[2].auto_neg  1          speed_list[2].lnk_speed 0x00000006
S:speed_list[3].auto_neg  1          speed_list[3].lnk_speed 0x00000005
S:speed_list[4].auto_neg  1          speed_list[4].lnk_speed 0x00000003
S:speed_list[5].auto_neg  0          speed_list[5].lnk_speed 0x00000000
S:
S:      port_ctrl.cm
S:=====
S:port_ctrl.cm.num_vcs          8
S:port_ctrl.cm.min_bufs          8
S:port_ctrl.cm.cr_shar_bufs      0
S:port_ctrl.vc_alloc
S:port_ctrl.vc_alloc          2 0 1 1 1 1 1 1
S:port_ctrl.vc_alloc          0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.norm_vc_alloc
S:port_ctrl.norm_vc_alloc          4 0 5 5 5 5 1 1
S:port_ctrl.norm_vc_alloc          0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.cm.skip_bb_credit          0
S:port_ctrl.cm.use_shim_based_sublist          0
S:

```



```

S:      port_ctrl.serdes_set
S:=====
S:serdes_type          0x8
S:serdes_data_t.ibm_hss_serdes.tx_drive_power          0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b_sign     0x1
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b         0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_a         0x0
S:serdes_data_t.ibm_hss_serdes.rxeq                   0x0
S:
S:      cfgbm
S:=====
S:old_distance        0x0          gport_lockdown      0x0
S:tport               0x1          speed                0x0
S:disable_eport       0x0          fcacc                0x0
S:lport_lockdown      0x0          priv_lport_lockdown
0x0
S:vcxlt_linit         0x0          delay_flogi          0x0
S:isl_interop         0x0          distance              0x0
S:BufStarvFlag        0x0          credit_sharing       0x0
S:lport_halfduplex    0x0          lport_fairness       0x0
S:soft_neg            0x0          asn_frc_hwretry      0x0
S:cr_recov            0x0          fport_buffers        0x0
S:export              0x0          export_mode
0x0
S:csctl_en            0x0          mirror_port          0x0
S:fault_delay         0x0          non_dfe              0x0
S:fec_configured*(0=ENAB) 0          fec_tts
0
S:port_persistently_disabled (permanently) 0 (0)
S:
S:      cfg property
S:=====
S:priv_pcfg_bm        0x00000000    lgcl_pcfg_bm
0xbb836664
S:fport_buffer        0x00000000
S:
S:
S:C4 Discard Cntrs: rxlp_stats = 0xb6ac6530
S:-----
-----
S:disc_mcast_wka      0x0          disc_inv_did         0x0
S:disc_cl1_cl4        0x0          disc_sid_chk_fail    0x0
S:disc_inv_dom_egid_txpt 0x0          disc_vft_hop_cnt_1
0x0
S:disc_classf         0x0          disc_fcp_cdb_inv     0x0
S:disc_vfid_trap_enabled 0x0
disc_vfid_hdr_chk_fail 0x0
S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err 0x0
S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err 0x0
S:disc_ftb_vm_mode    0x0          disc_ftb_agnt2_miss  0x0
S:disc_ecb_de_pad_err 0x0          disc_ecb_de_tag_err   0x0
S:disc_ecb_de_seq_err 0x0          disc_ecb_err          0x0
S:disc_ftb_type4_match 0x0          disc_fcp_rsp_ftb_type4 0x0
S:disc_fcp_rsp_ftb_type4 0x0          disc_ftb_type5_match

```

```

0x0
S:disc_ftb_type3_match 0x0          disc_els_ftb_type3      0x0
S:disc_ftb_type1_match 0x0          disc_els_rsp_ex_port   0x0
S:disc_inv_drp_dps      0x0          disc_did_lookup_miss   0x0
S:disc_ftb_type2_match 0x0          disc_trpd_plogi_pdisc  0x0
S:disc_type2_lookup_miss 0x0          disc_ftb_type6_match
0x0
S:disc_els_rep_ex_port 0x0          disc_els_sid_lkup_bit1 0x0
S:disc_els_sid_lkup_bit0 0x0
disc_bls_frm_trap_bit1 0x0
S:disc_ftb_token_err   0x0          disc_asic_internal_err 0x0
S:disc_hard_zone_miss  0x0          disc_lun_zone_miss     0x0
S:disc_flt_frame_disc  0x0          disc_flt_parity_err    0x0
S:disc_frame_marked_du 0x0          disc_frame_marked_to   0x0
E:Connection type: FE
E:Port type: E_port
E:Trunk port: No
E:Configured Speed: AUTO_SPEED_NEGO
E:Max Capable Speed: 32G
E:Current SNSM Speed: UNDEFINED
E:Hardware TX Speed: 32G (0x00000004)
E:Hardware RX Speed: 32G (0x00000040)
E:
E:Interrupts: 0          Link_failure: 0
Loss_of_sync: 0          Loss_of_sig: 0
E:Lli: 0                Invalid_word: 0
E:trapped_frm: 0         fwd_status_ok: 0
E:fwd_timeout: 0         fwd_tx_unavail: 0
E:fwd_unroutable: 0      fwd_zone_out: 0
E:fwd_other_err: 0       frm_err_discard: 0
E:Fltr listA: 0          Fltr listB: 0
E:Zone trap fwd: 0       Zone trap disc: 0
E:shim_csum: 0           RTE_perr: 0
E:Invalid_crc: 0         Delim_err: 0
E:Protocol_err: 0
E:Lr_in: 0               Lr_out: 0
E:Ols_in: 0              Ols_out: 0

```

filterportshow 51

FILTER DATA

```

-----
Shadow settings:
  Filter Enable: 0x00000000
  Redir RAM[0]: 0x00000000
  Redir RAM[1]: 0x00000000
  Redir RAM[2]: 0x00000000
  Redir RAM[3]: 0x00000000
  Redir RAM[4]: 0x00000000
  Redir RAM[5]: 0x00000000
  Redir RAM[6]: 0x00000000
  Redir RAM[7]: 0x00000000
  Redir RAM[8]: 0x00000000

```

Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass: 0x00000000

Real settings:

Enable RAM: 0x00000000, 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000

Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass RAM: 0x00000000

Shadowed filters:

Filter 0: Not Installed (MIRROR1)(LISTA)
c4_fldenable[0] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[0] = 0x00000000,c4_fltr_config[0] = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
c4_fldenable[1] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[1] = 0x00000000,c4_fltr_config[1] = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
c4_fldenable[2] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[2] = 0x00000000,c4_fltr_config[2] = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
c4_fldenable[3] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[3] = 0x00000000,c4_fltr_config[3] = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
c4_fldenable[4] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[4] = 0x00000000,c4_fltr_config[4] = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
c4_fldenable[5] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[5] = 0x00000000,c4_fltr_config[5] = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
c4_fldenable[6] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[6] = 0x00000000,c4_fltr_config[6] = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
c4_fldenable[7] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[7] = 0x00000000,c4_fltr_config[7] = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
c4_fldenable[8] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[8] = 0x00000000,c4_fltr_config[8] = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
c4_fldenable[9] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[9] = 0x00000000,c4_fltr_config[9] = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
c4_fldenable[10] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[10] = 0x00000000,c4_fltr_config[10] =
0x00000000
Filter 11: Not Installed (SIM)(LISTA)

```
    c4_fldenable[11] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[11] = 0x00000000,c4_fltr_config[11] =
0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
    c4_fldenable[12] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[12] = 0x00000000,c4_fltr_config[12] =
0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
    c4_fldenable[13] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[13] = 0x00000000,c4_fltr_config[13] =
0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
    c4_fldenable[14] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[14] = 0x00000000,c4_fltr_config[14] =
0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
    c4_fldenable[15] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[15] = 0x00000000,c4_fltr_config[15] =
0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
    c4_fldenable[16] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[16] = 0x00000000,c4_fltr_config[16] =
0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
    c4_fldenable[17] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[17] = 0x00000000,c4_fltr_config[17] =
0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
    c4_fldenable[18] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[18] = 0x00000000,c4_fltr_config[18] =
0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
    c4_fldenable[19] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[19] = 0x00000000,c4_fltr_config[19] =
0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
    c4_fldenable[20] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[20] = 0x00000000,c4_fltr_config[20] =
0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
    c4_fldenable[21] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[21] = 0x00000000,c4_fltr_config[21] =
0x00000000
```

Filter 22: Not Installed (PERF7)(LISTA)
c4_fldenable[22] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[22] = 0x00000000,c4_fltr_config[22] =
0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
c4_fldenable[23] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[23] = 0x00000000,c4_fltr_config[23] =
0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
c4_fldenable[24] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[24] = 0x00000000,c4_fltr_config[24] =
0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
c4_fldenable[25] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[25] = 0x00000000,c4_fltr_config[25] =
0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
c4_fldenable[26] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[26] = 0x00000000,c4_fltr_config[26] =
0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
c4_fldenable[27] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[27] = 0x00000000,c4_fltr_config[27] =
0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
c4_fldenable[28] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[28] = 0x00000000,c4_fltr_config[28] =
0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
c4_fldenable[29] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[29] = 0x00000000,c4_fltr_config[29] =
0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
c4_fldenable[30] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[30] = 0x00000000,c4_fltr_config[30] =
0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
c4_fldenable[31] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[31] = 0x00000000,c4_fltr_config[31] =
0x00000000

Real filters:

Filter 0: Not Installed (MIRROR1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 1: Not Installed (MIRROR2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 2: Not Installed (MIRROR3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 3: Not Installed (MIRROR4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 5: Not Installed (ZONING TRAP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 7: Not Installed (TIN TRAP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 8: Not Installed (FICON CUP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 9: Not Installed (FICON CUP DST)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 11: Not Installed (SIM)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 12: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 13: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,

0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 27: Not Installed (PERF12)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter dirty indicator: 0x00000000
Performance filters: 0
Port Mirror filters: 0 (0x0)

FIELD DATA

Shadowed fields:

fldoffset[0] = 0x00, fldmask[0] = 0x00, fldvalue_dyna[0]: 0x00 0x00
0x00 0x00
fldcontrol[0].inuse = 0x0 fldcontrol[0].refcnt = 0x00 0x00 0x00
0x00
fldoffset[1] = 0x00, fldmask[1] = 0x00, fldvalue_dyna[1]: 0x00 0x00
0x00 0x00
fldcontrol[1].inuse = 0x0 fldcontrol[1].refcnt = 0x00 0x00 0x00
0x00
fldoffset[2] = 0x00, fldmask[2] = 0x00, fldvalue_dyna[2]: 0x00 0x00
0x00 0x00
fldcontrol[2].inuse = 0x0 fldcontrol[2].refcnt = 0x00 0x00 0x00
0x00
fldoffset[3] = 0x00, fldmask[3] = 0x00, fldvalue_dyna[3]: 0x00 0x00
0x00 0x00
fldcontrol[3].inuse = 0x0 fldcontrol[3].refcnt = 0x00 0x00 0x00
0x00
fldoffset[4] = 0x00, fldmask[4] = 0x00, fldvalue_dyna[4]: 0x00 0x00
0x00 0x00
fldcontrol[4].inuse = 0x0 fldcontrol[4].refcnt = 0x00 0x00 0x00
0x00
fldoffset[5] = 0x00, fldmask[5] = 0x00, fldvalue_dyna[5]: 0x00 0x00
0x00 0x00
fldcontrol[5].inuse = 0x0 fldcontrol[5].refcnt = 0x00 0x00 0x00

```
0x00
fldoffset[6] = 0x00, fldmask[6] = 0x00, fldvalue_dyna[6]:0x00 0x00
0x00 0x00
fldcontrol[6].inuse = 0x0  fldcontrol[6].refcnt = 0x00 0x00 0x00
0x00
fldoffset[7] = 0x00, fldmask[7] = 0x00, fldvalue_dyna[7]:0x00 0x00
0x00 0x00
fldcontrol[7].inuse = 0x0  fldcontrol[7].refcnt = 0x00 0x00 0x00
0x00
fldoffset[8] = 0x00, fldmask[8] = 0x00, fldvalue_dyna[8]:0x00 0x00
0x00 0x00
fldcontrol[8].inuse = 0x0  fldcontrol[8].refcnt = 0x00 0x00 0x00
0x00
fldoffset[9] = 0x00, fldmask[9] = 0x00, fldvalue_dyna[9]:0x00 0x00
0x00 0x00
fldcontrol[9].inuse = 0x0  fldcontrol[9].refcnt = 0x00 0x00 0x00
0x00
fldoffset[10] = 0x00, fldmask[10] = 0x00, fldvalue_dyna[10]:0x00 0x00
0x00 0x00
fldcontrol[10].inuse = 0x0  fldcontrol[10].refcnt = 0x00 0x00 0x00
0x00
fldoffset[11] = 0x00, fldmask[11] = 0x00, fldvalue_dyna[11]:0x00 0x00
0x00 0x00
fldcontrol[11].inuse = 0x0  fldcontrol[11].refcnt = 0x00 0x00 0x00
0x00
fldoffset[12] = 0x00, fldmask[12] = 0x00, fldvalue_dyna[12]:0x00 0x00
0x00 0x00
fldcontrol[12].inuse = 0x0  fldcontrol[12].refcnt = 0x00 0x00 0x00
0x00
fldoffset[13] = 0x00, fldmask[13] = 0x00, fldvalue_dyna[13]:0x00 0x00
0x00 0x00
fldcontrol[13].inuse = 0x0  fldcontrol[13].refcnt = 0x00 0x00 0x00
0x00
fldoffset[14] = 0x00, fldmask[14] = 0x00, fldvalue_dyna[14]:0x00 0x00
0x00 0x00
fldcontrol[14].inuse = 0x0  fldcontrol[14].refcnt = 0x00 0x00 0x00
0x00
fldoffset[15] = 0x00, fldmask[15] = 0x00, fldvalue_dyna[15]:0x00 0x00
0x00 0x00
fldcontrol[15].inuse = 0x0  fldcontrol[15].refcnt = 0x00 0x00 0x00
0x00
fldoffset[16] = 0x00, fldmask[16] = 0x00, fldvalue_dyna[16]:0x00 0x00
0x00 0x00
fldcontrol[16].inuse = 0x0  fldcontrol[16].refcnt = 0x00 0x00 0x00
0x00
fldoffset[17] = 0x00, fldmask[17] = 0x00, fldvalue_dyna[17]:0x00 0x00
0x00 0x00
fldcontrol[17].inuse = 0x0  fldcontrol[17].refcnt = 0x00 0x00 0x00
0x00
fldoffset[18] = 0x00, fldmask[18] = 0x00, fldvalue_dyna[18]:0x00 0x00
0x00 0x00
fldcontrol[18].inuse = 0x0  fldcontrol[18].refcnt = 0x00 0x00 0x00
0x00
fldoffset[19] = 0x00, fldmask[19] = 0x00, fldvalue_dyna[19]:0x00 0x00
```

0x00 0x00
fldcontrol[19].inuse = 0x0 fldcontrol[19].refcnt = 0x00 0x00 0x00
0x00

Real fields:

fldoffset RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000
fldmask RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000
fld value4 RAM:
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
Field dirty indicator: 0x00000000

FDB reference count fdb: 0 [0 0 0 0]
FDB reference count fdb: 1 [0 0 0 0]
FDB reference count fdb: 2 [0 0 0 0]
FDB reference count fdb: 3 [0 0 0 0]
FDB reference count fdb: 4 [0 0 0 0]
FDB reference count fdb: 5 [0 0 0 0]
FDB reference count fdb: 6 [0 0 0 0]
FDB reference count fdb: 7 [0 0 0 0]
FDB reference count fdb: 8 [0 0 0 0]
FDB reference count fdb: 9 [0 0 0 0]
FDB reference count fdb: 10 [0 0 0 0]
FDB reference count fdb: 11 [0 0 0 0]
FDB reference count fdb: 12 [0 0 0 0]
FDB reference count fdb: 13 [0 0 0 0]
FDB reference count fdb: 14 [0 0 0 0]
FDB reference count fdb: 15 [0 0 0 0]
FDB reference count fdb: 16 [0 0 0 0]
FDB reference count fdb: 17 [0 0 0 0]
FDB reference count fdb: 18 [0 0 0 0]
FDB reference count fdb: 19 [0 0 0 0]

Filter counters:

Filter counter 0: 0 (MIRROR1)
Filter counter 1: 0 (MIRROR2)
Filter counter 2: 0 (MIRROR3)
Filter counter 3: 0 (MIRROR4)
Filter counter 4: 0 (AEPOR_T_NON_MIRR_DROP)
Filter counter 5: 0 (ZONING TRAP)
Filter counter 6: 0 (FCR_EXPORT_DC)
Filter counter 7: 0 (TIN TRAP)
Filter counter 8: 0 (FICON CUP)
Filter counter 9: 0 (FICON CUP DST)
Filter counter 10: 0 (WELL KNOWN ADDR)
Filter counter 11: 0 (SIM)
Filter counter 12: 0 (UNUSED)
Filter counter 13: 0 (UNUSED)
Filter counter 14: 0 (UNUSED)
Filter counter 15: 0 (UNUSED)
Filter counter 16: 0 (PERF1)
Filter counter 17: 0 (PERF2)
Filter counter 18: 0 (PERF3)
Filter counter 19: 0 (PERF4)
Filter counter 20: 0 (PERF5)
Filter counter 21: 0 (PERF6)
Filter counter 22: 0 (PERF7)
Filter counter 23: 0 (PERF8)
Filter counter 24: 0 (PERF9)
Filter counter 25: 0 (PERF10)
Filter counter 26: 0 (PERF11)
Filter counter 27: 0 (PERF12)
Filter counter 28: 0 (OPM1)
Filter counter 29: 0 (OPM2)
Filter counter 30: 0 (IPM1)
Filter counter 31: 0 (IPM2)

ACL DATA

Logical port 10: Hard Zoning disabled, Soft Zoning disabled
Zone type: WWN Zoning
Frames with hard zone miss: 0

*** Please use filterportshow on user port 56 to display ACL hash
tables and Mirroring resources of thischip.
***We show this data only for the first physical port which is an
external port.

portFcPortCmdShow --slot 0 52 3
doing portFcPortCmdShow: arg1 = 3, arg2 = -2

portshow 52
portDisableReason: None
portCFlags: 0x0
portFlags: 0x4021 PRESENT U_PORT DISABLED LED
LocalSwcFlags: 0x0
portType: 26.0

POD Port: Need license to enable the port
 portState: 2 Offline
 Protocol: FC
 portPhys: 2 No_Module portScn: 2 Offline
 port generation number: 0
 state transition count: 0

portId: 013400
 portIfId: 4302000c
 portWwn: 20:34:d8:1f:cc:2c:99:90
 portWwn of device(s) connected:
 16b Area list:
 Distance: normal
 portSpeed: N32Gbps

FEC: Inactive
 Credit Recovery: Inactive
 LE domain: 0
 Peer beacon: Off
 FC Fastwrite: OFF

| | | | | |
|-------------|---|---------------|---|-------|
| Interrupts: | 0 | Link_failure: | 0 | Frjt: |
| 0 | | | | |
| Unknown: | 0 | Loss_of_sync: | 0 | Fbsy: |
| 0 | | | | |
| Lli: | 0 | Loss_of_sig: | 0 | |
| Proc_rqrd: | 0 | Protocol_err: | 0 | |
| Timed_out: | 0 | Invalid_word: | 0 | |
| Tx_unavail: | 0 | Invalid_crc: | 0 | |
| Delim_err: | 0 | Address_err: | 0 | |
| Lr_in: | 0 | Ols_in: | 0 | |
| Lr_out: | 0 | Ols_out: | 0 | |

```
portloginshow 52
Type PID World Wide Name credit df_sz cos
=====
```

```
portloginshow 52 -history
Type PID World Wide Name logout time
=====
```

portregshow 52

LED registers
 =====
 0x81c62000: c4_led_status 00000000 0x81c62004:
 c4_led_ctl 00000000

FPL registers
 =====
 0x81c60200: fpl_port_config 23490000
 0x81c6020c: fpl_port_id_ctl 00000000 0x81c60210:

```

fpl_port_id_addr      00013400
0x81c60214: fpl_port_speed      00000004      0x81c6021c:
fpl_lli_ctl          00000903
0x81c60228: fpl_lli_os_ctl      bc95b5b5      0x81c6022c:
fpl_lli_send_word    bc95b5b5
0x81c60230: fpl_lli_mark_rx     00000000      0x81c60234:
fpl_lli_rnd_trip_time 00000000
0x81c60238: fpl_lli_ns_status    80070007      0x81c6023c:
fpl_lli_intr_status  80070007
0x81c60244: fpl_lli_def         00000000      0x81c60254:
fpl_lli_intr_enable_clr 00100000
0x81c60258: fpl_err_intr_status  00000000      0x81c60260:
fpl_err_intr_enable_clr 00000000
0x81c60268: fpl_err_first_error  00000000      0x81c6026c:
fpl_speed_neg_ctl    00000000
0x81c60270: fpl_speed_neg_stat     00000000      0x81c60274:
fpl_softasn_ctl      0000000f
0x81c60278: fpl_link_init_ctl    00000000      0x81c6027c:
fpl_link_init_stat   00000000
0x81c60280: fpl_aec_ctl           00051060      0x81c60284:
fpl_aec_ctl2         04009f60
0x81c60288: fpl_pcs_ctl         00000160      0x81c6028c:
fpl_fec_ctl          00000441
0x81c60290: fpl_fec_cor         00000000      0x81c60294:
fpl_fec_uncor        00000000
0x81c60298: fpl_hss_link_ctl     0031f040      0x81c6029c:
fpl_afifo_link_ctl   00000a86
0x81c602a0: fpl_echo_lb_ctl     0000028c      0x81c602a4:
fpl_scratch          00000121
0x81c602a8: fpl_debug           00030005      0x81c602ac:
fpl_misc_debug       00001800
0x00000000: SW_shadow_reg      00000000      0x00000000:
SW_c4_phyp->cfgptr    00030000

```

per-fpg (per octet) registers

```

=====
0x8180b82c: fpg_serdes_ctla0      81a37be7      0x8180b830:
fpg_serdes_ctla1      81a37be7
0x8180b834: fpg_serdes_ctlb0         81a1c3c3      0x8180b838:
fpg_serdes_ctlb1      81a1c3c3
0x8180b83c: fpg_serdes_xgmii_1ms     00067c28      0x8180b840:
fpg_serdes_regtimctl  40e47946
0x8180b844: fpg_serdes_asnrsttimctl 00000102

```

HSS PLL registers

```

=====
0x8180b400: 00_hssplla_vco_coarse_cal0 00000000      0x8180b404:
01_hssplla_vco_coarse_cal1 00000014
0x8180b408: 02_hssplla_vco_coarse_cal2 00000000      0x8180b40c:
03_hssplla_vco_coarse_cal3 00000000
0x8180b410: 04_hssplla_vco_coarse_cal4 00000000      0x8180b424:
09_hssplla_power_ctl  00000000
0x8180b428: 0A_hssplla_charge_pump_ctl 00000004      0x8180b438:
0E_hssplla_pll_misc_ctl 00000000

```

| | | |
|--|----------|-------------|
| 0x8180b43c: 0F_hssplla_pclk_ctl | 000000f8 | 0x8180b440: |
| 10_hssplla_eyem_intv_ctl | 00000000 | |
| 0x8180b444: 11_hssplla_eyem_intv_lim1 | 00000000 | 0x8180b448: |
| 12_hssplla_eyem_intv_lim2 | 00000000 | |
| 0x8180b44c: 13_hssplla_eyem_intv_lim3 | 00000000 | 0x8180b450: |
| 14_hssplla_eyem_intv_lim4 | 00000000 | |
| 0x8180b4f0: 3C_hssplla_macro_tst_ctl4 | 00000000 | 0x8180b4f4: |
| 3D_hssplla_macro_tst_ctl3 | 00000000 | |
| 0x8180b4f8: 3E_hssplla_macro_tst_ctl2 | 00000000 | 0x8180b4fc: |
| 3F_hssplla_macro_tst_ctl1 | 00000000 | |
| 0x8180b500: 00_hssppll_vco_coarse_cal0 | 0000000a | 0x8180b504: |
| 01_hssppll_vco_coarse_cal1 | 00000014 | |
| 0x8180b508: 02_hssppll_vco_coarse_cal2 | 00000000 | 0x8180b50c: |
| 03_hssppll_vco_coarse_cal3 | 00000000 | |
| 0x8180b510: 04_hssppll_vco_coarse_cal4 | 00000000 | 0x8180b524: |
| 09_hssppll_power_ctl | 00000000 | |
| 0x8180b528: 0A_hssppll_charge_pump_ctl | 00000004 | 0x8180b538: |
| 0E_hssppll_pll_misc_ctl | 00000000 | |
| 0x8180b53c: 0F_hssppll_pclk_ctl | 000000f8 | 0x8180b540: |
| 10_hssppll_eyem_intv_ctl | 00000000 | |
| 0x8180b544: 11_hssppll_eyem_intv_lim1 | 00000000 | 0x8180b548: |
| 12_hssppll_eyem_intv_lim2 | 00000000 | |
| 0x8180b54c: 13_hssppll_eyem_intv_lim3 | 00000000 | 0x8180b550: |
| 14_hssppll_eyem_intv_lim4 | 00000000 | |
| 0x8180b5f0: 3C_hssppll_macro_tst_ctl4 | 00000000 | 0x8180b5f4: |
| 3D_hssppll_macro_tst_ctl3 | 00000000 | |
| 0x8180b5f8: 3E_hssppll_macro_tst_ctl2 | 00000000 | 0x8180b5fc: |
| 3F_hssppll_macro_tst_ctl1 | 00000000 | |

HSS TX registers

=====

| | | |
|--------------------------------------|----------|-------------|
| 0x8180a000: 00_hsstx_cfg_mode_PHY | 00009f48 | 0x8180a004: |
| 01_hsstx_test_ctl | 00000000 | |
| 0x8180a008: 02_hsstx_coeff_ctl_INV | 00000000 | 0x8180a00c: |
| 03_hsstx_drv_mode_ctl | 00000000 | |
| 0x8180a010: 04_hsstx_drv_ovrd_ctl | 00000010 | 0x8180a014: |
| 05_hsstx_dclk_align_ovrd | 00000080 | |
| 0x8180a018: 06_hsstx_imp_cal_ovrd | 00000c0c | 0x8180a01c: |
| 07_hsstx_dclk_drift_tol | 00000004 | |
| 0x8180a020: 08_hsstx_tap0_coeff_TUNE | 00000000 | 0x8180a024: |
| 09_hsstx_tap1_coeff_TUNE | 00000003 | |
| 0x8180a028: 0A_hsstx_tap2_coeff_TUNE | 00000018 | 0x8180a02c: |
| 0B_hsstx_tap3_coeff_TUNE | 0000000d | |
| 0x8180a034: 0D_hsstx_pol_INV | 00000004 | 0x8180a038: |
| 0E_hsstx_ae_cmd | 00000000 | |
| 0x8180a03c: 0F_hsstx_ae_stat | 00000000 | 0x8180a040: |
| 10_hsstx_ae_tap0_TUNE | 00000000 | |
| 0x8180a044: 11_hsstx_ae_tap1_TUNE | 00000000 | 0x8180a048: |
| 12_hsstx_ae_tap2_TUNE | 00000028 | |
| 0x8180a04c: 13_hsstx_ae_tap3_TUNE | 00000000 | 0x8180a054: |
| 15_hsstx_app_tune | 0000120e | |
| 0x8180a058: 16_hsstx_analog_diag | 00000000 | 0x8180a060: |
| 18_hsstx_4x_seg_app | 0000aafa | |
| 0x8180a064: 19_hsstx_2x_seg_app | 00000000 | 0x8180a068: |

| | | | |
|---|----------|-------------|--|
| 1A_hsstx_1x_seg_app | 0000ff5d | | |
| 0x8180a06c: 1B_hsstx_seg_4x_term_app | 00000000 | 0x8180a070: | |
| 1C_hsstx_seg_2x1x_term_app | 00000f00 | | |
| 0x8180a074: 1D_hsstx_tap_sign_app | 00000004 | 0x8180a078: | |
| 1E_hsstx_ext_addr_data | 00000001 | | |
| 0x8180a07c: 1F_hsstx_ext_addr_addr | 00000000 | 0x8180a080: | |
| 20_hsstx_pat_buf_bytes_1_0 | 00000000 | | |
| 0x8180a084: 21_hsstx_pat_buf_bytes_3_2 | 00000000 | 0x8180a088: | |
| 22_hsstx_pat_buf_bytes_5_4 | 00000000 | | |
| 0x8180a08c: 23_hsstx_pat_buf_bytes_7_6 | 00000000 | 0x8180a09c: | |
| 27_hsstx_8023az_ctl | 00000000 | | |
| 0x8180a0a0: 28_hsstx_dcc_ctl | 000060c0 | 0x8180a0a4: | |
| 29_hsstx_dcc_ovrd | 00001000 | | |
| 0x8180a0a8: 2A_hsstx_dcc_app | 00000000 | 0x8180a0ac: | |
| 2B_hsstx_dcc_timeout | 0000ffff | | |
| 0x8180a0c0: 30_hsstx_tap_sign_ovrd | 00000000 | 0x8180a0c8: | |
| 32_hsstx_seg_4x_ovrd | 00000000 | | |
| 0x8180a0cc: 33_hsstx_seg_2x_ovrd | 00000000 | 0x8180a0d0: | |
| 34_hsstx_seg_1x_ovrd | 00000000 | | |
| 0x8180a0d8: 36_hsstx_tap_seg_4x_term_ovrd | 00000000 | 0x8180a0dc: | |
| 37_hsstx_tap_seg_2x_term_ovrd | 00000000 | | |
| 0x8180a0e0: 38_hsstx_tap_seg_1x_term_ovrd | 00000000 | 0x8180a0ec: | |
| 3B_hsstx_mac_test_ctl5 | 00000000 | | |
| 0x8180a0f0: 3C_hsstx_mac_test_ctl4 | 00000000 | 0x8180a0f4: | |
| 3D_hsstx_mac_test_ctl3 | 00000000 | | |
| 0x8180a0f8: 3E_hsstx_mac_test_ctl2 | 00000000 | 0x8180a0fc: | |
| 3F_hsstx_mac_test_ctl1 | 000000c6 | | |

HSS RX registers

=====

| | | | |
|---------------------------------------|----------|-------------|--|
| 0x8180a200: 00_hssrx_cfg_mode_PHY | 00009e78 | 0x8180a204: | |
| 01_hssrx_test_ctl | 00000000 | | |
| 0x8180a208: 02_hssrx_phs_rot_ctl | 0000cb80 | 0x8180a20c: | |
| 03_hssrx_phs_rot_ofs_ctl | 00003610 | | |
| 0x8180a210: 04_hssrx_phs_rot_posn1 | 00003b3b | 0x8180a214: | |
| 05_hssrx_phs_rot_posn2 | 00000028 | | |
| 0x8180a218: 06_hssrx_phs_rot_sta_ofs1 | 00000000 | 0x8180a21c: | |
| 07_hssrx_phs_rot_sta_ofs2 | 00000000 | | |
| 0x8180a220: 08_hssrx_dfe_ctl_PHY | 00002002 | 0x8180a224: | |
| 09_hssrx_dfe_smpl_snap1 | 00000000 | | |
| 0x8180a228: 0A_hssrx_dfe_smpl_snap2 | 00008000 | 0x8180a22c: | |
| 0B_hssrx_vga_ctl1 | 000041fe | | |
| 0x8180a230: 0C_hssrx_vga_ctl2 | 00007aa0 | 0x8180a234: | |
| 0D_hssrx_vga_ctl3 | 000009e4 | | |
| 0x8180a238: 0E_hssrx_pwr_mgmnt_ctl | 0000001f | 0x8180a23c: | |
| 0F_hssrx_iqamp_ctl1 | 0000001a | | |
| 0x8180a240: 10_hssrx_iqamp_ctl2 | 00000005 | 0x8180a244: | |
| 11_hssrx_dacap_dacan_sel | 00000003 | | |
| 0x8180a248: 12_hssrx_dacap_dacan | 0000ffff | 0x8180a24c: | |
| 13_hssrx_daca_min | 00000000 | | |
| 0x8180a250: 14_hssrx_adac_ctl | 00000000 | 0x8180a254: | |
| 15_hssrx_ac_cp_ctl | 000031c3 | | |
| 0x8180a258: 16_hssrx_ac_cp_val | 00000052 | 0x8180a25c: | |
| 17_hssrx_dfe_h1h2h3_lcl_off_ch | 00000014 | | |

| | | |
|--|----------------|-------------|
| 0x8180a260: 18_hssrx_dfe_h1h2h3_lcl_off_val | 00000000 | 0x8180a264: |
| 19_hssrx_peaked_intg | 000000ff | |
| 0x8180a268: 1A_hssrx_cdr_analog_sw | 0000ce00 | 0x8180a26c: |
| 1B_hssrx_peaking_amp_init_c_PHY | 00000000 | |
| 0x8180a270: 1C_hssrx_dac_dpc | 00000040 | 0x8180a274: |
| 1D_hssrx_ddc | 00000000 | |
| 0x8180a278: 1E_hssrx_int_stat_PHY | 00001c0f | 0x8180a27c: |
| 1F_hssrx_dfe_func_ctl1_PHY | 0000ffff | |
| 0x8180a280: 20_hssrx_dfe_func_ctl2_INV | 00007ebf | 0x8180a284: |
| 21_hssrx_ofs_ch_dcc_qcc_idx | 00002000 | |
| 0x8180a288: 22_hssrx_dfe_ofs_val | 00007a7c | 0x8180a28c: |
| 23_hssrx_h_coeff_bist | 00000401 | |
| 0x8180a290: 24_hssrx_ac_cap_bist | 0000006b | 0x8180a294: |
| 25_hssrx_max_gain_path_idx_res | 00007800 | |
| 0x8180a298: 26_hssrx_loff_ctl | 00000040 | 0x8180a29c: |
| 27_hssrx_sigdet_ctl | 00002880 | |
| 0x8180a2a0: 28_hssrx_ana_ctl_sw | 00000000 | 0x8180a2a4: |
| 29_hssrx_intg_dac_ofs | 0000dee1 | |
| 0x8180a2a8: 2A_hssrx_eye_ctl | 00000000 | 0x8180a2ac: |
| 2B_hssrx_eye_met | 00000004 | |
| 0x8180a2b0: 2C_hssrx_eye_met_err_cnt | 00000000 | 0x8180a2b4: |
| 2D_hssrx_eye_met_pdf_eyec | 00000000 | |
| 0x8180a2b8: 2E_hssrx_eye_met_pat_len | 0000007f | 0x8180a2bc: |
| 2F_hssrx_dfe_func_ctl3 | 0000dfff | |
| 0x8180a2c0: 30_hssrx_dfe_tap_ctl_idx_ptr | 00000008 | 0x8180a2c4: |
| 31_hssrx_dfe_tap | 00003030 | |
| 0x8180a2c8: 32_hssrx_lte_ctl_TUNE | 00001601 | 0x8180a2e4: |
| 39_hssrx_int_stat2 | 0000c1ff | |
| 0x8180a2e8: 3A_hssrx_ac_cpl_cur_src_adj | 00000040 | 0x8180a2ec: |
| 3B_hssrx_dcd_ctl | 00007c45 | |
| 0x8180a2f0: 3C_hssrx_dcc_ctl | 00000d83 | 0x8180a2f4: |
| 3D_hssrx_qcc_ctl | 00006986 | |
| 0x8180a2f8: 3E_hssrx_mac_test_ctl2 | 00000000 | 0x8180a2fc: |
| 3F_hssrx_mac_test_ctl1 | 00000000 | |
| 0x8180a248: 12_hssrx_dacap_dacan[02] | 00ff ffff | |
| 0x8180a260: 18_hssrx_dfe_h1h2h3_lcl_off_va[00] | 0000 0000 0000 | |
| 0000 0000 0000 0000 0000 | | |
| 0x8180a260: 18_hssrx_dfe_h1h2h3_lcl_off_va[08] | 0000 0000 0000 | |
| 0000 0000 0000 0000 0000 | | |
| 0x8180a260: 18_hssrx_dfe_h1h2h3_lcl_off_va[16] | 0000 0000 0000 | |
| 0000 0000 | | |
| 0x8180a288: 22_hssrx_dfe_ofs_val[00][00] | 7a7c 0000 0d11 | |
| 7f7f 7d01 7f7f | | |
| 0x8180a288: 22_hssrx_dfe_ofs_val[03][00] | 047a 7f00 7f7a | |
| 0000 7d7b 0000 | | |
| 0x8180a288: 22_hssrx_dfe_ofs_val[06][00] | 7f7f 0000 037c | |
| 7f00 0301 7f7f | | |
| 0x8180a288: 22_hssrx_dfe_ofs_val[09][00] | 7979 0000 037b | |
| 7f00 0708 7f7f | | |
| 0x8180a288: 22_hssrx_dfe_ofs_val[12][00] | 037f 0000 7903 | |
| 0000 0107 007f | | |
| 0x8180a288: 22_hssrx_dfe_ofs_val[15][00] | 7d02 0000 7d00 | |
| 0000 7b03 0000 | | |
| 0x8180a288: 22_hssrx_dfe_ofs_val[18][00] | 7f01 0000 797c | |

```

0000 007b 0000
0x8180a288: 22_hssrx_dfe_ofs_val[21][00] 007b 0000 007b
0000 007b 0000
0x8180a288: 22_hssrx_dfe_ofs_val[24][00] 097d 7f00 7e7b
7f00 7c7d 0000
0x8180a294: 25_hssrx_max_gain_path_idx_res[00] 005e 084f 1111
1898 20d0 28a0 3089 3800
0x8180a294: 25_hssrx_max_gain_path_idx_res[08] 40b0 4890 507d
5800 6040 6800 70fe 7800
0x8180a2c4: 31_hssrx_dfe_tap[00] fffe 8080 0000
0000 0030 0030 3030 3030
0x8180a2c4: 31_hssrx_dfe_tap[08] 3030 3030 3030
0000
0x8180a2e8: 3A_hssrx_ac_cpl_cur_src_adj[00] 0040 0040 0040
0040
0x8180a2ec: 3B_hssrx_dcd_ctl[00] 7c45 5c00 7c83
5c00 7c81
0x8180a2f0: 3C_hssrx_dcc_ctl[00] 0d83 0d00 0d43
0d42
0x8180a2f4: 3D_hssrx_qcc_ctl[00] 698b 6986

```

xfipcs, fec, aec, & aet registers

=====

```

0x81c60400: xfipcs_reg [00] 00002040 00000080 00000000
00000000 00000001 00000008 00000000 00000000
0x81c60420: xfipcs_reg [08] 00008c01 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c60440: xfipcs_reg [16] 00000000 00000000 00000000
00000000 00000040 00000000 00000000 00000000
0x81c60460: xfipcs_reg [24] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c60480: xfipcs_reg [32] 00000004 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c60620: fec_32g_128g_reg [08] 00000000 00000000 00000000
00000000 00000000 00000000 00000000
0x81c60648: fec_32g_128g_reg [18] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c60a00: aec_reg [00] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c60c00: aet_reg [00] 00000000 00000000 00000000
00000000 00000000

```

bbc registers

=====

```

0x81c61800: bbc_trc 0 0 0 0 0 0 0
0
0x81c61840: bbc_trc 0 0 0 0 0 0 0
0
0x81c61880: bbc_trc 0 0 0 0 0 0 0
0
0x81c618c0: bbc_trc 0 0 0 0 0 0 0
0
0x81c61900: bbc_trc 0 0 0 0 0 0 0
0

```

| | | | | | | | |
|-------------------------------------|----------|----------------------|---|---|---|---|---|
| 0x81c61804: bbc_mbc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c61844: bbc_mbc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c61884: bbc_mbc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c618c4: bbc_mbc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c61904: bbc_mbc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c61a00: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c61a20: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c61a40: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c61a60: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c61a80: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c61c00: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c61c20: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c61c40: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c61c60: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c61c80: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c61d00: bbc_fbpc | 00000000 | | | | | | |
| 00000000 | | | | | | | |
| 0x81c61d08: bbc_rcc_inc | 00000000 | | | | | | |
| bbc_rqc_inc | 00000000 | | | | | | |
| 0x81c61d10: bbc_fbpc_inc | 00000000 | | | | | | |
| bbc_tmc_inc | 00000000 | | | | | | |
| 0x81c61d18: bbc_threshold | 00080100 | | | | | | |
| bbc_counter_clr | 00000000 | | | | | | |
| 0x81c61d20: bbc_debug_en | 00000000 | | | | | | |
| 00200020 | | | | | | | |
| 0x81c61d28: bbc_rqc_rcc_thresh | 00000055 | | | | | | |
| bbc_bb_sc_n | 00000000 | | | | | | |
| 0x81c61d38: bbc_crd_reco_debug | 00000000 | | | | | | |
| bbc_crd_reco_debug_data | 00000000 | | | | | | |
| 0x81c61d40: bbc_multi_frm_loss_cnt | 00000000 | | | | | | |
| bbc_multi_rdy_loss_cnt | 00000000 | | | | | | |
| 0x81c61d48: bbc_1frm_loss_recov_cnt | 00000000 | | | | | | |
| bbc_1rdy_loss_recov_cnt | 00000000 | | | | | | |
| 0x81c61d58: bbc_int_status | 00000000 | | | | | | |
| bbc_int_set | 00000000 | | | | | | |
| 0x81c61d60: bbc_int_first | 00000000 | | | | | | |
| bbc_frm_rdy_rx_err_addr | 00000000 | | | | | | |
| 0x81c61d68: bbc_frm_rdy_tx_err_addr | 00000000 | | | | | | |
| bbc_trc_mbc_err_addr | 00000000 | | | | | | |
| | | 0x81c61d04: bbc_csc | | | | | |
| | | 0x81c61d0c: | | | | | |
| | | 0x81c61d14: | | | | | |
| | | 0x81c61d1c: | | | | | |
| | | 0x81c61d24: bbc_ctrl | | | | | |
| | | 0x81c61d34: | | | | | |
| | | 0x81c61d3c: | | | | | |
| | | 0x81c61d44: | | | | | |
| | | 0x81c61d4c: | | | | | |
| | | 0x81c61d5c: | | | | | |
| | | 0x81c61d64: | | | | | |
| | | 0x81c61d6c: | | | | | |

```

0x81c61d70: bbc_frm_rdy_rx_dbl_ecc 00000000 0x81c61d74:
bbc_frm_rdy_tx_dbl_ecc 00000000
0x81c61d78: bbc_trc_mbc_dbl_ecc 00000000
0x81c61d7c: bbc_fsm_status 00001011 0x81c61d80:
bbc_force_err 00000000
0x81c61d84: bbc_crdr_avail0 ffffffff 0x81c61d88:
bbc_crdr_avail1 000000ff
0x81c61d8c: bbc_scratch 00000000

```

FPS registers

=====

```

0x81c60004: fps_er_enc_in 00000000 0x81c60008:
fps_er_crc 00000000
0x81c6000c: fps_er_trunc 00000000 0x81c60010:
fps_er_toolong 00000000
0x81c60014: fps_er_bad_eof 00000000 0x81c60018:
fps_er_enc_out 00000000
0x81c6001c: fps_er_bad_os 00000000 0x81c60020:
fps_er_flush 00000000
0x81c60024: fps_er_ifg 00000000 0x81c60038:
fps_er_crc_good_eof 00000000
0x81c6003c: fps_inv_arb 00000000 0x81c60040:
fps_slow_sts_status 00000000
0x81c60044: fps_tx_frm_cnt 00000000 0x81c60048:
fps_rx_frm_cnt 00000000
0x81c60050: fps_tx_word_cnt_hi 00000000 0x81c6004c:
fps_tx_word_cnt_lo 00000000
0x81c60058: fps_rx_word_cnt_hi 00000000 0x81c60054:
fps_rx_word_cnt_lo 00000000

```

BAL registers

=====

```

0x81c67000: bal_desired_buf 00000000 0x81c67004:
bal_alloc_buf 00000000
0x81c67008: bal_busy_buf 00000000 0x81c6700c:
bal_usable_buf 00000000
0x81c67010: bal_max_bor_buf 00000000
0x81c67014: bal_busy_buf_thresh 00000002

```

TXQ registers

=====

```

0x81c63004: txq_phys_port_ctl 00440000
0x81c63050: txq_link_skew 00000000
0x81c63068: txq_cr_lk_dttm_intr_sts [00] 00000000 00000000
0x81c63070: txq_cr_lk_dttm_intr_en [00] 00000000 00000000
0x81c63024: txq_disc_frm_trap_cnt 00000014

```

FDS registers

=====

```

0x81c64000: fds_rxf_ctl 00000002 0x81c64004:
fds_rxf_wait_thresh 00000909
0x81c64018: fds_rxf_first_error 00000000 0x81c6401c:
fds_rxf_first_error_info 00000000
0x81c64020: fds_rxf_inout_pkt_cnt 00000000

```

```

0x81c64008: fds_rxf_err_int_status 00000000 0x81c64024:
fds_rxf_fifo_status 00888888
0x81c65000: fds_txf_ctl 0000003a 0x81c65004:
fds_txf_wait_ifg_thresh 00a00106
0x81c65008: fds_txf_err_int_status 00000000 0x81c65024:
fds_txf_fifo_status 00088888
0x81c6502c: fds_txf_bbc_scs 00000000

```

Logical TXQ registers

=====

```

0x81c63000: txq_log_port_ctl 00000002 0x81c63008:
txq_port_status 00000000
0x81c6300c: txq_todo_flags [00] 00000000 00000000
0x81c63014: txq_spd_match_desc [00] 00000000 00000000 00000000
00000000
0x81c63024: txq_spd_match_desc [04] 00000014
0x81c63028: txq_vc_weight [00] 01010101 01010101 01010101
01010101
0x81c63038: txq_vc_weight [04] 01010101 01010101 01010101
01010101
0x81c63048: txq_vc_weight [08] 01010101 00010101
0x81c63054: txq_cong_dttm_ctrl 00000000
0x81c63058: txq_cong_dttm_intr_sts [00] 00000000 00000000
0x81c63060: txq_cong_dttm_intr_en [00] 00000000 00000000
0x81c63078: txq_bw_limit_en_reg [00] 00000000 00000000
0x81c63080: txq_bw_gua_en_reg [00] 00000000 00000000
0x81c63088: txq_vc_group [00] 03030300 03030303 03030303
03030303
0x81c63098: txq_vc_group [04] 03030303 03030303 03030303
03030303
0x81c630a8: txq_vc_group [08] 03030303 03030303 00000000
00000000
0x81c630b0: txq_bw_thresh_group [00] 00000000 00000000 00000000
00000000
0x81c630c0: txq_bw_thresh_group [04] 00000000 00000000 00000000
00000000
0x81c630d0: txq_bw_thresh_group [08] 00000000 00000000 00000000
00000000
0x81c630e0: txq_bw_thresh_group [12] 00000000 00000000 00000000
00000000
0x81c630f0: txq_bw_thresh_group [16] 00000000 00000000 00000000
00000000
0x81c63100: txq_bw_thresh_group [20] 00000000 00000000 00000000
00000000
0x81c63110: txq_bw_thresh_group [24] 00000000 00000000 00000000
00000000
0x81c63120: txq_bw_thresh_group [28] 00000000 00000000 00000000
00000000
0x81c63130: txq_bw_thresh_group [32] 00000000 00000000 00000000
00000000
0x81c63140: txq_bw_thresh_group [36] 00000000 00000000 00000000
00000000

```

txq Congestion detection Statistics RAM

```

=====
0x81090780: vc[0]      00000000      0x81090784: vc[1]
00000000
0x81090788: vc[2]      00000000      0x8109078c: vc[3]
00000000
0x81090790: vc[4]      00000000      0x81090794: vc[5]
00000000
0x81090798: vc[6]      00000000      0x8109079c: vc[7]
00000000
0x810907a0: vc[8]      00000000      0x810907a4: vc[9]
00000000
0x810907a8: vc[10]     00000000      0x810907ac: vc[11]
00000000
0x810907b0: vc[12]     00000000      0x810907b4: vc[13]
00000000
0x810907b8: vc[14]     00000000      0x810907bc: vc[15]
00000000
0x810907c0: vc[16]     00000000      0x810907c4: vc[17]
00000000
0x810907c8: vc[18]     00000000      0x810907cc: vc[19]
00000000
0x810907d0: vc[20]     00000000      0x810907d4: vc[21]
00000000
0x810907d8: vc[22]     00000000      0x810907dc: vc[23]
00000000
0x810907e0: vc[24]     00000000      0x810907e4: vc[25]
00000000
0x810907e8: vc[26]     00000000      0x810907ec: vc[27]
00000000
0x810907f0: vc[28]     00000000      0x810907f4: vc[29]
00000000
0x810907f8: vc[30]     00000000      0x810907fc: vc[31]
00000000
0x81090800: vc[32]     00000000      0x81090804: vc[33]
00000000
0x81090808: vc[34]     00000000      0x8109080c: vc[35]
00000000
0x81090810: vc[36]     00000000      0x81090814: vc[37]
00000000
0x81090818: vc[38]     00000000      0x8109081c: vc[39]
00000000

```

Logical STS registers

```

=====
0x81584984: sts_ftb_type1_miss  00000000
0x81584988: sts_ftb_type2_miss  00000000
0x8158498c: sts_ftb_type6_miss  00000000
0x81584990: sts_hard_zoning_miss  00000000
0x81584994: sts_lun_zoning_miss  00000000
0x8158499c: sts_unroutable        00000000
0x815819b4: sts_rte_cl2          00000000      0x815819b8:
sts_rte_cl3          00000000      0x815819bc: sts_rte_link_ctl
00000000      0x815849a8: sts_tx_timeout        00000000

```

Logical STS filter registers

=====

| | | | | |
|-------------------------|------|----------|----------|----------|
| 0x81584900: stsflt_trig | [00] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584910: stsflt_trig | [04] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584920: stsflt_trig | [08] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584930: stsflt_trig | [12] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584940: stsflt_trig | [16] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584950: stsflt_trig | [20] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584960: stsflt_trig | [24] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584970: stsflt_trig | [28] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584980: stsflt_trig | [32] | | | |

Logical STS discard registers

=====

| | | |
|------------------------------------|----------|-------------|
| 0x81582170: disc_mcast_wka | 00000000 | 0x81582174: |
| disc_inv_did | 00000000 | |
| 0x81582178: disc_cll_cl4 | 00000000 | 0x8158217c: |
| disc_sid_chk_fail | 00000000 | |
| 0x81582180: disc_inv_dom_egid_txpt | 00000000 | 0x81582184: |
| disc_vft_hop_cnt_1 | 00000000 | |
| 0x81582188: disc_classf | 00000000 | 0x8158218c: |
| disc_fcp_cdb_inv | 00000000 | |
| 0x81582190: disc_vfid_trap_enabled | 00000000 | 0x81582194: |
| disc_vfid_hdr_chk_fail | 00000000 | |
| 0x81582198: disc_shim_cksum_fail | 00000000 | 0x8158219c: |
| disc_fed_edit_cmd_err | 00000000 | |
| 0x815821a0: disc_ftb_vm_mode | 00000000 | 0x815821a4: |
| disc_ftb_agnt2_miss | 00000000 | |
| 0x815821a8: disc_ecb_reserved | 00000000 | 0x815821ac: |
| disc_ecb_de_pad_err | 00000000 | |
| 0x815821b0: disc_ecb_de_tag_err | 00000000 | 0x815821b4: |
| disc_ecb_de_seq_err | 00000000 | |
| 0x815821b8: disc_ecb_err | 00000000 | 0x815821bc: |
| disc_ftb_type4_match | 00000000 | |
| 0x815821c0: disc_fcp_rsp_ftb_type4 | 00000000 | 0x815821c4: |
| disc_ftb_type5_match | 00000000 | |
| 0x815821c8: disc_ftb_type3_match | 00000000 | 0x815821cc: |
| disc_els_ftb_type3 | 00000000 | |
| 0x815821d0: disc_ftb_type1_match | 00000000 | 0x815821d4: |
| disc_els_rsp_ex_port | 00000000 | |
| 0x815821d8: disc_inv_drp_dps | 00000000 | 0x815821dc: |
| disc_did_lookup_miss | 00000000 | |
| 0x815821e0: disc_ftb_type2_match | 00000000 | 0x815821e4: |
| disc_trpd_plogi_pdisc | 00000000 | |
| 0x815821e8: disc_type2_lookup_miss | 00000000 | 0x815821ec: |

```

disc_ftb_type6_match      00000000
0x815821f0: disc_els_rep_ex_port      00000000      0x815821f4:
disc_els_sid_lkup_bit1   00000000
0x815821f8: disc_els_sid_lkup_bit0    00000000      0x815821fc:
disc_bls_frm_trap_bit1   00000000
0x81582200: disc_ftb_token_err      00000000      0x81582204:
disc_asic_internal_err   00000000
0x81582208: disc_hard_zone_miss      00000000      0x8158220c:
disc_lun_zone_miss       00000000
0x81582210: discflt_frame_disc      00000000      0x81582214:
discflt_parity_err       00000000
0x81582218: disc_frame_marked_du      00000000      0x8158221c:
disc_frame_marked_to     00000000
0x81582220: disc_lkup_rte_prty_err    00000000

```

portstatsshow 52

```

stat_wtx      0      4-byte words transmitted
stat_wrx      0      4-byte words received
stat_ftx      0      Frames transmitted
stat_frx      0      Frames received
stat_c2_frx   0      Class 2 frames received
stat_c3_frx   0      Class 3 frames received
stat_lc_rx    0      Link control frames
received
stat_mc_rx    0      Multicast frames
received
stat_mc_to    0      Multicast timeouts
stat_mc_tx    0      Multicast frames
transmitted
tim_txcrd_z   0      Time TX Credit Zero
(2.5Us ticks)
tim_txcrd_z_vc 0- 3: 0      0      0      0
tim_txcrd_z_vc 4- 7: 0      0      0      0
tim_txcrd_z_vc 8-11: 0     0      0      0
tim_txcrd_z_vc 12-15: 0    0      0      0
lat_tot_pkt_vc 0- 3: 1      1      1      1
lat_tot_pkt_vc 4- 7: 1      1      1      1
lat_tot_pkt_vc 8-11: 1     1      1      1
lat_tot_pkt_vc 12-15: 1    1      1      1
lat_hi_time_vc 0- 3: 0      0      0      0
lat_hi_time_vc 4- 7: 0      0      0      0
lat_hi_time_vc 8-11: 0     0      0      0
lat_hi_time_vc 12-15: 0    0      0      0
lat_lo_time_vc 0- 3: 1      1      1      1
lat_lo_time_vc 4- 7: 1      1      1      1
lat_lo_time_vc 8-11: 1     1      1      1
lat_lo_time_vc 12-15: 1    1      1      1
max_latency_vc 0- 3: 1      1      1      1
max_latency_vc 4- 7: 1      1      1      1
max_latency_vc 8-11: 1     1      1      1
max_latency_vc 12-15: 1    1      1      1

```

```

latency_dma_ts      09-09-2024 UTC Mon 08:47:25      TXQ
Latency DMA TimeStamp

```


| | | |
|------------------------------|-----------------------------|--------------------------|
| fec_cor_detected | 0 | Count of blocks that |
| were corrected by FEC | | |
| fec_uncor_detected | 0 | Count of blocks that |
| were left uncorrected by FEC | | |
| er_enc_in | 0 | Encoding errors inside |
| of frames | | |
| er_crc | 0 | Frames with CRC errors |
| er_trunc | 0 | Frames shorter than |
| minimum | | |
| er_toolong | 0 | Frames longer than |
| maximum | | |
| er_bad_eof | 0 | Frames with bad end-of- |
| frame | | |
| er_enc_out | 0 | Encoding error outside |
| of frames | | |
| er_bad_os | 0 | Invalid ordered set |
| er_pcs_blk | 0 | PCS block errors |
| er_rx_c3_timeout | 0 | Class 3 receive frames |
| discarded due to timeout | | |
| er_tx_c3_timeout | 0 | Class 3 transmit frames |
| discarded due to timeout | | |
| er_unroutable | 0 | Frames that are |
| unroutable | | |
| er_unreachable | 0 | Frame with unreachable |
| destination | | |
| er_other_discard | 0 | Other discards |
| er_type1_miss | 0 | frames with FTB type 1 |
| miss | | |
| er_type2_miss | 0 | frames with FTB type 2 |
| miss | | |
| er_type6_miss | 0 | frames with FTB type 6 |
| miss | | |
| er_zone_miss | 0 | frames with hard zoning |
| miss | | |
| er_lun_zone_miss | 0 | frames with LUN zoning |
| miss | | |
| er_crc_good_eof | 0 | Crc error with good eof |
| er_inv_arb | 0 | Invalid ARB |
| er_single_credit_loss | 0 | Single vcrdy/frame loss |
| on link | | |
| er_multi_credit_loss | 0 | Multiple vcrdy/frame |
| loss on link | | |
| other_credit_loss | 0 | Link timeout/complete |
| credit loss | | |
| phy_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | Timestamp of |
| phy_port stats clear | | |
| lgc_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | Timestamp of |
| lgc_port stats clear | | |
| fec_corrected_rate | 0 | FEC Corrected blocks per |
| second | | |

portstats64show 52

stat64_wtx 0
0

top_int : 4-byte words transmitted
bottom_int : 4-byte words transmitted

| | | |
|------------------------|---|--|
| stat64_wrx | 0 | top_int : 4-byte words received |
| | 0 | bottom_int : 4-byte words received |
| stat64_ftx | 0 | top_int : Frames transmitted |
| | 0 | bottom_int : Frames transmitted |
| stat64_frx | 0 | top_int : Frames received |
| | 0 | bottom_int : Frames received |
| stat64_c2_frx | 0 | top_int : Class 2 frames received |
| | 0 | bottom_int : Class 2 frames received |
| stat64_c3_frx | 0 | top_int : Class 3 frames received |
| | 0 | bottom_int : Class 3 frames received |
| stat64_lc_rx | 0 | top_int : Link control frames received |
| | 0 | bottom_int : Link control frames |
| received | | |
| stat64_mc_rx | 0 | top_int : Multicast frames received |
| | 0 | bottom_int : Multicast frames received |
| stat64_mc_to | 0 | top_int : Multicast timeouts |
| | 0 | bottom_int : Multicast timeouts |
| stat64_mc_tx | 0 | top_int : Multicast frames transmitted |
| | 0 | bottom_int : Multicast frames |
| transmitted | | |
| tim64_rdy_pri | 0 | top_int : Time R_RDY high priority |
| | 0 | bottom_int : Time R_RDY high priority |
| tim64_txcrd_z | 0 | top_int : Time BB_credit zero |
| | 0 | bottom_int : Time BB_credit zero |
| er64_enc_in | 0 | top_int : Encoding errors inside of |
| frames | 0 | bottom_int : Encoding errors inside of |
| frames | | |
| er64_crc | 0 | top_int : Frames with CRC errors |
| | 0 | bottom_int : Frames with CRC errors |
| er64_trunc | 0 | top_int : Frames shorter than minimum |
| | 0 | bottom_int : Frames shorter than minimum |
| er64_toolong | 0 | top_int : Frames longer than maximum |
| | 0 | bottom_int : Frames longer than maximum |
| er64_bad_eof | 0 | top_int : Frames with bad end-of-frame |
| | 0 | bottom_int : Frames with bad end-of- |
| frame | | |
| er64_enc_out | 0 | top_int : Encoding error outside of |
| frames | 0 | bottom_int : Encoding error outside of |
| frames | | |
| er64_disc_c3 | 0 | top_int : Class 3 frames discarded |
| | 0 | bottom_int : Class 3 frames discarded |
| er64_pcs_blk | 0 | top_int : PCS block errors |
| | 0 | bottom_int : PCS block errors |
| stat64_rateTxFrame | 0 | Tx frame rate (fr/sec) |
| stat64_rateRxFrame | 0 | Rx frame rate (fr/sec) |
| stat64_rateTxPeakFrame | 0 | Tx peak frame rate (fr/sec) |
| stat64_rateRxPeakFrame | 0 | Rx peak frame rate (fr/sec) |
| stat64_rateTxWord | 0 | Tx Word rate (words/sec) |
| stat64_rateRxWord | 0 | Rx Word rate (words/sec) |
| stat64_rateTxPeakWord | 0 | Tx peak Word rate (words/sec) |
| stat64_rateRxPeakWord | 0 | Rx peak Word rate (words/sec) |
| stat64_PRJTFrames | 0 | top_int : Number of PRJT frames |

```

returned to this port          0          bottom_int : Number of PRJT
frames returned to this port
stat64_PBSYFrames             0          top_int : Number of PBSY frames
returned to this port          0          bottom_int : Number of PBSY
frames returned to this port
stat64_inputBuffersFull       0          top_int : Number of occurrences
when all input buffers full    0          bottom_int : Number of
occurrences when all input buffers full
stat64_rxClass1Frames         0          top_int : Number of class 1
frames received                0          bottom_int : Number of class 1
frames received
stat64_aveTxFrameSize         0          Average Tx Frame size
stat64_aveRxFrameSize         0          Average Rx Frame size
Lr_in                          0          top_int
                          0          bottom_int
Ols_in                          0          top_int
                          0          bottom_int
Lr_out                          0          top_int
                          0          bottom_int
Ols_out                          0          top_int
                          0          bottom_int
Link_failure                    0          top_int
                          0          bottom_int
Invalid_CRC                     0          top_int
                          0          bottom_int
Invalid_word                     0          top_int
                          0          bottom_int
Protocol_err                     0          top_int
                          0          bottom_int
Loss_of_sig                      0          top_int
                          0          bottom_int
Loss_of_sync                      0          top_int
                          0          bottom_int
er_bad_os                        0          top_int : Invalid ordered set
                          0          bottom_int: Invalid ordered set

```

```

portrouteshow 52
port address ID: 0x013400
external unicast routing table:
  0: Embedded
 255: Embedded
internal unicast routing table:
  0: Embedded

```

```
portcamshow 52
```

```

-----
Port  SID used  DID used  SID entries  DID entries
52    0         0        000000      000000
-----

```

ptbufshow, ptcreditshow, ptdatashow, ptstatsshow 52

S:

S:VF Enable: 1

S:

S:C4 Global Variable:

S:-----

S:trace_stop: 0

S:

S:C4 Phy Data Pointers: c4_phyp = 0xb6acb0c0

S:-----

S:tnodep 0xbb838d20 pt
0x4302800c

S:proto_phyp 0xb8808240 phy_cfg
0xb6acc100

S:c4_chp 0x97e28000 c4_lgcp
0x97f78000

S:c4_phy_regp 0x81c60000 proc_dir
0xb8517140

S:-----

S:magic_id 0xc4345678 num_port_timer 12

S:prev_if_id 0x4302000c S:ftx 0
tov 0

S:initialized 0 port_idx 12

S:ui_idx 52 slot_no
0

S:blade_idx 12 sw_usr_ports 400

S:unused 0 intr_debounced
0

S:aec_status 0x0 reason_code
0

S:debug 0x00000004 debug_trc_line 0

S:rxbuf_list_head 0xffffffff rxbuf_list_tail
0xffffffff

S:isAePort 0 port_misc_data
0

S:num_fault1_rx_disc 0 num_fault2_rx_disc 0

S:p_lli_cause0 0 p_sig_regained 0

S:p_sync_regained 0 enc_out
0x0

S:cached_fps_status 0 cached_sts_status 0

S:cached_er_crc_good_eof 0

S:cached_er_bad_os 0 cached_er_too_long 0

S:cached_er_trunc 0

cached_tot_er_crc_good_eof 0

S:num_pt_excess_intr 0 num_no_fid 0

S:num_fault1_cnt 0 num_fault2_cnt
0

S:num_fault_lip 0 num_fault_lli 0

S:num_fault_rx_fifo 0 num_fault_hss 0

S:num_fault_bwait 0 lli_intr_prim

```

    0
S:num_sw_link_to          0
be_link_err_mon_count    0
S:ecb_enc_enabled        0          ecb_comp_enabled
    0
S:ecb_rsv_enc            0          ecb_rsv_comp          0
S:ecb_enc_bm            0x0        ecb_key_index
0xffffffff
S:fab_idx                4
S:num_be_lto             0          lto_count_reset_intvl
    0
S:lr_count_reset_intvl  0          num_be_lr
    0
S:num_fault_qsfps       0          check_lto
    0
S:credit_loaded         0          num_credit_overrun
    0
S:fec_enabled           0x0        fec_los_to_flag        0x0
S:phy_stats_clear_ts    1725611419  pcs_err_online
    0
S:pcs_err_light_det     0          pcs_err_ignore
    0
S:pcs_blk_err           0          pcs_hiber              0
S:phy_port_status       0          ecb_enc_lr_count
    0
S:dport_mode            0          avoid_lto_det          0
S:sn_debounced          0x0        sn_started_kr_reqd     0
S:major_timer_started   0x0        ready_bm               0x0
S:parln_1_bm            0x0        parln_0_bm             0x0
S:be_los_of_sync_event_intvl
be_los_of_sync_event    0
S:errataPtenable_cntr   0          errataPoll_cntr
    0
S:jda_rx_sig_loss_det   0          jda_rx_sig_loss_cnt
    0
S:encrypt_blk_error     0
S:
S:      c4_trunk
S:=====
S:mark_ts                0x0          deskew                 0x0
S:master_phyp            0x0
S:
S:adelay[00]: 0x00000000 0x00000000 0x00000000 0x00000000
S:adelay[04]: 0x00000000 0x00000000 0x00000000 0x00000000
S:
S:      c4_buf
S:=====
S:tx_csc                  0          rx_csc
    0
S:ld_vc_credits          0          tx_flag                0x0
S:alloc_buffers          0          req_buffers            0
S:est_buffers            20         ld_use_est             0
S:bb_sc_n                0          rx_bb_sc_n
    0

```

```

S:data_cr          5          nondata_cr
  6
S:cr_enable      0
S:ld_nondata_cr  6          tnodep
0xbb838e00
S:tx_credits[0]  0    0    0    0    0    0    0    0
S:tx_credits[8]  0    0    0    0    0    0    0    0
S:tx_credits[16]    0    0    0    0    0    0    0    0    0
S:tx_credits[24]    0    0    0    0    0    0    0    0    0
S:tx_credits[32]    0    0    0    0    0    0    0    0    0
S:rx_credits[0]  0    0    0    0    0    0    0    0
S:rx_credits[8]  0    0    0    0    0    0    0    0
S:rx_credits[16]    0    0    0    0    0    0    0    0    0
S:rx_credits[24]    0    0    0    0    0    0    0    0    0
S:rx_credits[32]    0    0    0    0    0    0    0    0    0
S:tx_mbc[0]      0    0    0    0    0    0    0    0
S:tx_mbc[8]      0    0    0    0    0    0    0    0
S:tx_mbc[16]     0    0    0    0    0    0    0    0
S:tx_mbc[24]     0    0    0    0    0    0    0    0
S:tx_mbc[32]     0    0    0    0    0    0    0    0
S:rx_mbc[0]      0    0    0    0    0    0    0    0
S:rx_mbc[8]      0    0    0    0    0    0    0    0
S:rx_mbc[16]     0    0    0    0    0    0    0    0
S:rx_mbc[24]     0    0    0    0    0    0    0    0
S:rx_mbc[32]     0    0    0    0    0    0    0    0

```

```

S:
S:C4 Chip Variables: c4_phyp->c4_chp = 0x97e28000

```

```

S:-----

```

```

S:version = 2.1
S:magic_id      0xc4234567      init_state      0x8
S:reset_reg_mem 0x1
S:ch_int0_en_bm 0x0          intr0_cause     0x0
S:ch_int1_en_bm 0x0          intr1_cause     0x0
S:ch_int2_en_bm 0x0          intr2_cause     0x0
S:ch            0x43010080      ch_cfg
0xb7013ba0
S:raslog_hndl.hndl 0x0          obj_halted     0x0
S:c4_chip_regp  0x80000000      c4_fpg_regp
0x81800000
S:num_chip_timer 0x5
S:hi_task_bm    0x0          lo_task_bm     0x0
S:c4_deferq.q_head 0x0          c4_deferq.q_tail 0x0
S:c4_tmrq.q_head 0x0          c4_tmrq.q_tail 0x0
slot_no        0
S:chip_inst     0          chip_idx       0
S:pll_initialized 1          1
pll_serdes_initialized 1
S:init_tries    0          init_ptEnableBM
0xba01b488
S:tick_polling 0xb980c9c0      sec_polling
0xb980c960
S:bb_fid        129
S:ecb_key_bm[0] 0x0          ecb_key_bm[1] 0x0

```

```

S:ecb_key_bm[2]          0x0          ecb_key_bm[3]          0x0
S:is_chip_enc_enabled   0          0
is_chip_comp_enabled    0x0
S:ftb_rsrcp->ftb_flags  0x0          act_rsrcp->act_flag    0x1
S:lue_rsrcp->lue_flags[0]      0x0          lue_rsrcp-
>lue_flags[1]          0x0
S:c4_phyp[00]: 0xb6ab0000 0xb6ab2080 0xb6ab4100 0xb6ab6180
S:c4_phyp[04]: 0xb6ab9040 0xb6abb0c0 0xb6abd140 0xb6ac0000
S:c4_phyp[08]: 0xb6ac2080 0xb6ac4100 0xb6ac6180 0xb6ac9040
S:c4_phyp[12]: 0xb6acb0c0 0xb6acd140 0xb6ad0000 0xb6ad2080
S:c4_phyp[16]: 0xb6ad4100 0xb6ad6180 0xb6ad9040 0xb6adb0c0
S:c4_phyp[20]: 0xb6add140 0xb6ae0000 0xb6ae2080 0xb6ae4100
S:c4_phyp[24]: 0xb6ae6180 0xb6ae9040 0xb6aeb0c0 0xb6aed140
S:c4_phyp[28]: 0xb6af0000 0xb6af2080 0xb6af4100 0xb6af6180
S:c4_phyp[32]: 0xb6af9040 0xb6afb0c0 0xb6afd140 0xb6b00000
S:c4_phyp[36]: 0xb6b02080 0xb6b04100 0xb6b06180 0xb6b09040
S:c4_phyp[40]: 0xb6b0b0c0 0xb6b0d140 0xb6b10000 0xb6b12080
S:c4_phyp[44]: 0xb6b14100 0xb6b16180 0xb6b19040 0xb6b1b0c0
S:c4_phyp[48]: 0xb6b1d140 0xb6b20000 0xb6b22080 0xb6b24100
S:c4_phyp[52]: 0xb6b26180 0xb6b29040 0xb6b2b0c0 0xb6b2d140
S:c4_phyp[56]: 0xb6b30000 0xb6b32080 0xb6b34100 0xb6b36180
S:c4_phyp[60]: 0xb6b39040 0xb6b3b0c0 0xb6b3d140 0xb6b40000
S:c4_lgcp[00]: 0x97f48000 0x97f4c000 0x97f50000 0x97f54000
S:c4_lgcp[04]: 0x97f58000 0x97f5c000 0x97f60000 0x97f64000
S:c4_lgcp[08]: 0x97f68000 0x97f6c000 0x97f70000 0x97f74000
S:c4_lgcp[12]: 0x97f78000 0x97f7c000 0x97f80000 0x97f84000
S:c4_lgcp[16]: 0x97f88000 0x97f8c000 0x97f90000 0x97f94000
S:c4_lgcp[20]: 0x97f98000 0x97f9c000 0x97fa0000 0x97fa4000
S:c4_lgcp[24]: 0x97fa8000 0x97fac000 0x97fb0000 0x97fb4000
S:c4_lgcp[28]: 0x97fb8000 0x97fbc000 0x97fc0000 0x97fc4000
S:c4_lgcp[32]: 0x97fc8000 0x97fcc000 0x97fd0000 0x97fd4000
S:c4_lgcp[36]: 0x97fd8000 0x97fdc000 0x97fe0000 0x97fe4000
S:c4_lgcp[40]: 0x97fe8000 0x97fec000 0x97ff0000 0x97ff4000
S:c4_lgcp[44]: 0x97ff8000 0x97ffc000 0x8e000000 0x8e004000
S:c4_lgcp[48]: 0x8e008000 0x8e00c000 0x8e010000 0x8e014000
S:c4_lgcp[52]: 0x8e018000 0x8e01c000 0x8e020000 0x8e024000
S:c4_lgcp[56]: 0x8e028000 0x8e02c000 0x8e030000 0x8e034000
S:c4_lgcp[60]: 0x8e038000 0x8e03c000 0x8e040000 0x8e044000
S:chip_timers[00]: 0xb980c720 0xb980c780 0xb980c7e0 0xb980c840
S:chip_timers[04]: 0xb980c8a0 0xb980c900
S:disc_trap_enable_required 0x0          rxlp_disc_log_stop
0x0
S:curr_rxlp_frm_cnt     0x0          curr_rxlp_disc_frm_cnt 0x0
S:sw_disc_frm_cnt       0x0          last_disc_frm_cnt       0x0
S:txq_nopop_pr_cnt     0x0          pollErrataDfe_ptBM
0xba01b4b0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][0] 0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][1] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][2] 0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][0] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][1] 0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][2] 0x0
S:
S:C4 Logical Port Variables

```

```

S:-----
-----
S:c4_lgc_regp          0x81c60000
S:c4_phyp:
S:      0xb6acb0c0      0x0          0x0          0x0

S:      0x0          0x0          0x0          0x0

S:master_phyp          0xb6acb0c0      if_id
0x4302000c
S:min_phyp            0x0          max_phyp          0x0
S:num_phy_ports      1          lgc_num          12
S:num_iu_to          0          sw_txq_bm
0
S:port_fid          129          unused          0
S:port_group        1          lgc_stats_clear_ts
1725611419
S:domain_tbl_sel      0          area_tbl_sel
0
S:egid_tbl_sel        0
S:serv_lo_bm          0x0
S:
S:Proto Phy Variables:
S:-----
-----
S:magic_id            0xc4123456      asic_phyp
0xb6acb0c0
S:port_id              0x4302800c      phy_cfg
0xb6acc100
S:upsm_hdl            0xb8013320      physm_hdl
0xb80130a0
S:ov_snsn_hdl         0xb8012f00      sw_snsn_hdl
0xb8013000
S:ov_lksm_hdl         0xb8013140      sw_lksm_hdl
0xb80131e0
S:trksm_hdl           0xb8013280      lr_flag          0x0
S:lr_active           0x0          qsfp_trxr_rate_sel
0x0
S:
S:UPSM      UP00: UPST_PORT_DISABLED    --> UP00: UPST_PORT_DISABLED
S:SNSM(OV)  SN00: OV_SNST_STOPPED          --> SN00: OV_SNST_STOPPED
S:SNSM(SW)  SW00: SW_SNST_STAGE_WS      --> SW00: SW_SNST_STAGE_WS
S:PHYSM     PP00: PHYST_STOPPED         --> PP00: PHYST_STOPPED
S:LKSM(OV)  LK00: OV_LKST_INACTIVE       --> LK00: OV_LKST_INACTIVE
S:LKSM(SW)  SW13: INACTIVE              --> SW13: INACTIVE
S:TRKSM     TRK0: TRKST_INIT            --> TRK0: TRKST_INIT
S:
S:physm variables:
S:-----
-----
S:proto_phyp          0xb8808240      physm_hdl
0xb80130a0
S:force_offline       0          copper          0
S:fault_reason        0: UNKNOWN

```



```

S:phy_media_present          0
S:
S:sns variables:
S:-----
-----
S:speed                      0xff          proto_phyp
0xb8808240
S:hw_sn_tries_left          0x0          sw_sn_tries_left          0x0
S:curr_txsp_count          0x0
S:tx_max                    0x0          curr_tx_indx
          0x0
S:curr_tx                   0x0          curr_rxsp_count
          0x0
S:rx_max                    0x0          curr_rx_indx
          0x0
S:curr_rx                   0x0          rx_mem
          0x0
S:rxsp_rec_count           0x0
S:nc_start                  0x0          tx_start                  0x0
S:sync_start               0x0          sync_present              0x0
S:diag_auto                0x0          diag_speed                0xff
S:striped_wd_tov           3000          hw_wd_tov
          3000
S:step                      0x0          qsfp28_speed_mode
          0x0
S:qsfp_mode0_hw_sn_tries_left 0x0
S:qsfp_mode1_hw_sn_tries_left 0x0
S:
S:lksm variables:
S:-----
-----
S:proto_phyp                0xb8808240  ov_lksm_hdl
0xb8013140
sw_lksm_hdl                 0xb80131e0
num_lf1                     0
S:hw_link_tries_left        0          sw_link_tries_left        0
S:buf_ptype                 0x0          stored_entry_state        0x6
S:handshake_owner           0x0          mark_unsent
          0x0
S:busybuf_stuck             0x0          lr_wait                   0x0
S:
S:trksm variables:
S:-----
-----
S:Not a trunk port
S:
S:upsm variables:
S:-----
-----
S:proto_phyp                0xb8808240  upsm_hdl
0xb8013320
S:bb_credits                0          port_beacon               0
S:port_diag_flag           0          force_offline
          0

```

```

S:port_fault_rsn          0: PORT_NO_FAULT
S:retry_init_rsn         0: UNKNOWN
S:limit_reason           0          linit_result          0
S:ie_fctl_mode           0          fec_in_sync_tries_left 0
S:retry_sn_fail_init     0
retry_link_fail_init     0
S:excess_lr_count       0
S:

```

```
S:c4_ch_cfg
```

```
S:-----
```

```

S:c4_desc_ring_size      256      292      256      256      292
292      2      292      292
S:thresh_def             0          16          1          0
S:intr_tries             500          cmem_pattern
0xdeadbeef
S:cmem_pattern_upwd      2          cmem_init_time          16
S:cmem_init_tries        5
S:ctrl_par_thresh        2          data_par_thresh
4
S:cam_par_thresh         4          buf_loss_thresh
12
S:crit_par_thresh        2          non_crit_par_thresh
6
S:pci_abort_thresh       10          pci_err_thresh          5
S:excess_chintr_thresh   8          sw_err_thresh           20
S:err_sample_period      300          intr_sleep
20000
S:frame_timeout          2500          proxy_dev                16384
S:vf_route               81920          qos                      2048
S:stats 2048             f_redirect          2048
S:rsp_trap               2048          lun_zoning                20480
S:area_mode              0          ftb_max_loop[0]          0
S:ftb_max_loop[1]        6          ftb_max_loop[2]          9
S:ftb_max_loop[3]        10         ftb_max_loop[4]          10
S:ftb_max_loop[5]        5          ftb_max_loop[6]          6
S:ftb_seg_size[0]        0          ftb_seg_size[1]
16384
S:ftb_seg_size[2]        65536         ftb_seg_size[3]
16384
S:ftb_seg_size[4]        16384         ftb_seg_size[5]
65536
S:ftb_seg_size[6]        16384         ftb_seg_base[0]          0
S:ftb_seg_base[1]        0          ftb_seg_base[2]
65536
S:ftb_seg_base[3]        16384         ftb_seg_base[4]
32768
S:ftb_seg_base[5]        131072        ftb_seg_base[6]
49152
asic_err_monitor_period1 300
asic_err_monitor_period2 86400
zone_chk_to_poll_period 25
zone_chk_class2_reject_tov 220
S:

```

S:c4_phy_cfg

S:-----

S:version = 2.1
S:pt 0x4302800c fab_ptr
0x9a800000
S:fabattr 0x9a8000d4 fab_iop
0x9a800050
S:cfgbm 0xbb838b64 port_ctrl
0xb6acc118
S:pcap.pcap_bm 0x8d215547 pcap.pcap2_bm
0x2588289
S:pcap.pcap3_bm 0x1bebe0c
ui_idx 52 S:slot_no
0
is_icl 0 S:sw_usr_ports 400
S:neg_speed 0 0 0 0 0 0
S:my_domain 0x1 port_mode 0x0
S:hw_sn_maxtries 100 sw_sn_maxtries
0
S:hw_link_maxtries 10 sw_link_maxtries 5
S:rx_cyc_tov 28 rttov 300
S:bufrdy_tov 300 busybuf_tov 286
S:mark_tov 300 lksm_tov 3000
S:buf_dealloc_wait 4 hw_wd_tov 3000
S:hw_lk_train_tov 540 hw_lk_test_tov
150
S:syswait_tx_12_lips 1 lip_rx_tov 55
S:al_time_tov 15 lp_tov 2000
S:intr_tries_port 500 intr_mod_debounce
250
S:intr_lsrflt_debounce 500 intr_efifo_debounce 100
S:port_no_fid 3 excess_ptintr_thresh 8
S:port_fault1_thresh 100 port_fault1_spur_thresh 250
S:port_fault1_disc_thresh 500
port_fault1_disc_spur_thresh 1000
S:port_fault2_thresh 5 losync_tov 100
S:port_sw_link_to 15 en_8g_scramble
1
frc_hw_sn_mode 0x1
S:enc_poll_thresh 0 fec_enable
0
S:fec_in_sync_to 50 fec_in_sync_try_max
4
S:port_be_lto_threshold 100 port_be_lr_threshold
2
S:be_cr_in_sync_to 5
port_credit_overrun_thresh 10
S:jda_sfp_losig_tov 400
jda_sfp_losig_try_max 30
S:striped_wd_tov 3000
no_sync_debounce 1200
S:
S: fab_iop

```

S:=====
S:fab_iop->interop_mode 0x0          fab_iop->lab_mode      0x0
S:fab_iop->fl_bbc          0x0          fab_iop->fl_fan
0x0
S:fab_iop->fl_cls          0x4          fab_iop->fl_rscn
0x0
S:fab_iop->domain_id_offset 0x60          fab_iop-
>mcdt_fabric_mode      0x0
S:fab_iop->mcdt_default_zone 0x0          fab_iop-
>mcdt_safe_zone      0x0
S:
S:      port_ctrl
S:=====
S:port_ctrl.port_type  1          port_ctrl.port_grp    1
S:port_ctrl.port_number 52          port_ctrl.vc_mode     1
S:
S:      port_ctrl.lcap
S:=====
S:has_serdes          0          has_media              1
S:topology            1          skip_nego              0
S:skip_pnego          0          skip_init_event        0
S:en_shim              0          speed_neg
1
S:loop_back           0          num_speeds             5
S:fec_enable          0
S:
S:      port_ctrl.speed_list array
S:=====
S:speed_list[0].auto_neg 1          speed_list[0].lnk_speed 0x0000000a
S:speed_list[1].auto_neg 1          speed_list[1].lnk_speed 0x00000008
S:speed_list[2].auto_neg 1          speed_list[2].lnk_speed 0x00000006
S:speed_list[3].auto_neg 1          speed_list[3].lnk_speed 0x00000005
S:speed_list[4].auto_neg 1          speed_list[4].lnk_speed 0x00000003
S:speed_list[5].auto_neg 0          speed_list[5].lnk_speed 0x00000000
S:
S:      port_ctrl.cm
S:=====
S:port_ctrl.cm.num_vcs          8
S:port_ctrl.cm.min_bufs        8
S:port_ctrl.cm.cr_shar_bufs    0
S:port_ctrl.vc_alloc
S:port_ctrl.vc_alloc          2 0 1 1 1 1 1 1
S:port_ctrl.vc_alloc          0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.norm_vc_alloc
S:port_ctrl.norm_vc_alloc      4 0 5 5 5 5 1 1
S:port_ctrl.norm_vc_alloc      0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.cm.skip_bb_credit  0
S:port_ctrl.cm.use_shim_based_sublist 0
S:
S:      port_ctrl.serdes_set
S:=====
S:serdes_type                0x8

```

```

S:serdes_data_t.ibm_hss_serdes.tx_drive_power          0x1
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b_sign    0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b        0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_a        0x0
S:serdes_data_t.ibm_hss_serdes.rxeq                  0x0
S:
S:      cfgbm
S:=====
S:old_distance          0x0          gport_lockdown          0x0
S:tport                 0x1          speed                      0x0
S:disable_eport        0x0          fcacc                    0x0
S:lport_lockdown      0x0          priv_lport_lockdown
0x0
S:vcxlt_linit          0x0          delay_flogi              0x0
S:isl_interop          0x0          distance                  0x0
S:BufStarvFlag        0x0          credit_sharing           0x0
S:lport_halfduplex    0x0          lport_fairness           0x0
S:soft_neg             0x0          asn_frc_hwretry          0x0
S:cr_recov             0x0          fport_buffers            0x0
S:export               0x0          export_mode
0x0
S:csctl_en             0x0          mirror_port              0x0
S:fault_delay          0x0          non_dfe                  0x0
S:fec_configured*(0=ENAB) 0          fec_tts
0
S:port_persistently_disabled (permanently) 0 (0)
S:
S:      cfg property
S:=====
S:priv_pcfg_bm          0x00000000    lgcl_pcfg_bm
0xbb838ba4
S:fport_buffer          0x00000000
S:
S:
S:C4 Discard Cntrs: rxlp_stats = 0xb6acb470
S:-----
-----
S:disc_mcast_wka        0x0          disc_inv_did              0x0
S:disc_cl1_cl4         0x0          disc_sid_chk_fail        0x0
S:disc_inv_dom_egid_txpt 0x0          disc_vft_hop_cnt_1
0x0
S:disc_classf          0x0          disc_fcp_cdb_inv         0x0
S:disc_vfid_trap_enabled 0x0
disc_vfid_hdr_chk_fail 0x0
S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err    0x0
S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err    0x0
S:disc_ftb_vm_mode     0x0          disc_ftb_agn_t2_miss     0x0
S:disc_ecb_de_pad_err  0x0          disc_ecb_de_tag_err      0x0
S:disc_ecb_de_seq_err  0x0          disc_ecb_err              0x0
S:disc_ftb_type4_match 0x0          disc_fcp_rsp_ftb_type4   0x0
S:disc_fcp_rsp_ftb_type4 0x0          disc_ftb_type5_match
0x0
S:disc_ftb_type3_match 0x0          disc_els_ftb_type3       0x0
S:disc_ftb_type1_match 0x0          disc_els_rsp_ex_port     0x0

```

```

S:disc_inv_drp_dps      0x0          disc_did_lookup_miss    0x0
S:disc_ftb_type2_match 0x0          disc_trpd_plogi_pdisc   0x0
S:disc_type2_lookup_miss      0x0          disc_ftb_type6_match
      0x0
S:disc_els_rep_ex_port  0x0          disc_els_sid_lkup_bit1  0x0
S:disc_els_sid_lkup_bit0      0x0
disc_bls_frm_trap_bit1 0x0
S:disc_ftb_token_err      0x0          disc_asic_internal_err  0x0
S:disc_hard_zone_miss      0x0          disc_lun_zone_miss      0x0
S:discflt_frame_disc      0x0          discflt_parity_err      0x0
S:disc_frame_marked_du     0x0          disc_frame_marked_to    0x0
E:Connection type: FE
E:Port type: E_port
E:Trunk port: No
E:Configured Speed: AUTO_SPEED_NEGO
E:Max Capable Speed: 32G
E:Current SNSM Speed: UNDEFINED
E:Hardware TX Speed: 32G (0x00000004)
E:Hardware RX Speed: 32G (0x00000040)
E:
E:Interrupts:      0          Link_failure:           0
Loss_of_sync:      0          Loss_of_sig:            0
E:Lli:              0          Invalid_word:           0
E:trapped_frm:      0          fwd_status_ok:          0
E:fwd_timeout:      0          fwd_tx_unavail:         0
E:fwd_unroutable:      0          fwd_zone_out:           0
E:fwd_other_err:      0          frm_err_discard:        0
E:Fltr listA:      0          Fltr listB:             0
E:Zone trap fwd:      0          Zone trap disc:         0
E:shim_csum:        0          RTE_perr:               0
E:Invalid_crc:      0          Delim_err:              0
E:Protocol_err:     0
E:Lr_in:            0          Lr_out:                 0
E:Ols_in:           0          Ols_out:                0

```

filterportshow 52

FILTER DATA

```

Shadow settings:
  Filter Enable: 0x00000000
  Redir RAM[0]: 0x00000000
  Redir RAM[1]: 0x00000000
  Redir RAM[2]: 0x00000000
  Redir RAM[3]: 0x00000000
  Redir RAM[4]: 0x00000000
  Redir RAM[5]: 0x00000000
  Redir RAM[6]: 0x00000000
  Redir RAM[7]: 0x00000000
  Redir RAM[8]: 0x00000000
  Redir RAM[9]: 0x00000000
  Redir RAM[10]: 0x00000000
  Redir RAM[11]: 0x00000000

```

Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass: 0x00000000

Real settings:

Enable RAM: 0x00000000, 0x00000000

Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000

Redir RAM[31]: 0x00000000
Bypass RAM: 0x00000000

Shadowed filters:

Filter 0: Not Installed (MIRROR1)(LISTA)
c4_fldenable[0] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[0] = 0x00000000,c4_fltr_config[0] = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
c4_fldenable[1] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[1] = 0x00000000,c4_fltr_config[1] = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
c4_fldenable[2] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[2] = 0x00000000,c4_fltr_config[2] = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
c4_fldenable[3] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[3] = 0x00000000,c4_fltr_config[3] = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
c4_fldenable[4] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[4] = 0x00000000,c4_fltr_config[4] = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
c4_fldenable[5] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[5] = 0x00000000,c4_fltr_config[5] = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
c4_fldenable[6] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[6] = 0x00000000,c4_fltr_config[6] = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
c4_fldenable[7] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[7] = 0x00000000,c4_fltr_config[7] = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
c4_fldenable[8] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[8] = 0x00000000,c4_fltr_config[8] = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
c4_fldenable[9] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[9] = 0x00000000,c4_fltr_config[9] = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
c4_fldenable[10] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[10] = 0x00000000,c4_fltr_config[10] =
0x00000000
Filter 11: Not Installed (SIM)(LISTA)
c4_fldenable[11] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[11] = 0x00000000,c4_fltr_config[11] =


```
0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
    c4_fldenable[12] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[12] = 0x00000000,c4_fltr_config[12] =
0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
    c4_fldenable[13] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[13] = 0x00000000,c4_fltr_config[13] =
0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
    c4_fldenable[14] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[14] = 0x00000000,c4_fltr_config[14] =
0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
    c4_fldenable[15] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[15] = 0x00000000,c4_fltr_config[15] =
0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
    c4_fldenable[16] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[16] = 0x00000000,c4_fltr_config[16] =
0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
    c4_fldenable[17] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[17] = 0x00000000,c4_fltr_config[17] =
0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
    c4_fldenable[18] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[18] = 0x00000000,c4_fltr_config[18] =
0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
    c4_fldenable[19] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[19] = 0x00000000,c4_fltr_config[19] =
0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
    c4_fldenable[20] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[20] = 0x00000000,c4_fltr_config[20] =
0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
    c4_fldenable[21] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[21] = 0x00000000,c4_fltr_config[21] =
0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
    c4_fldenable[22] = 0x00000000 0x00000000 0x00000000
0x00000000
```

```
    c4_fldnegate[22] = 0x00000000,c4_fltr_config[22] =
0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
    c4_fldenable[23] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[23] = 0x00000000,c4_fltr_config[23] =
0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
    c4_fldenable[24] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[24] = 0x00000000,c4_fltr_config[24] =
0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
    c4_fldenable[25] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[25] = 0x00000000,c4_fltr_config[25] =
0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
    c4_fldenable[26] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[26] = 0x00000000,c4_fltr_config[26] =
0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
    c4_fldenable[27] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[27] = 0x00000000,c4_fltr_config[27] =
0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
    c4_fldenable[28] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[28] = 0x00000000,c4_fltr_config[28] =
0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
    c4_fldenable[29] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[29] = 0x00000000,c4_fltr_config[29] =
0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    c4_fldenable[30] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[30] = 0x00000000,c4_fltr_config[30] =
0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    c4_fldenable[31] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[31] = 0x00000000,c4_fltr_config[31] =
0x00000000
```

Real filters:

```
Filter 0: Not Installed (MIRROR1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
```

fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 11: Not Installed (SIM)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)

fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,

```
      fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
      fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
      fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
      fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
      fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
      fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
      fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
      fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
      fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter dirty indicator: 0x00000000
Performance filters: 0
Port Mirror filters: 0 (0x0)
```

FIELD DATA

Shadowed fields:

```
fldoffset[0] = 0x00, fldmask[0] = 0x00, fldvalue_dyna[0]: 0x00 0x00
0x00 0x00
fldcontrol[0].inuse = 0x0 fldcontrol[0].refcnt = 0x00 0x00 0x00
0x00
fldoffset[1] = 0x00, fldmask[1] = 0x00, fldvalue_dyna[1]: 0x00 0x00
0x00 0x00
fldcontrol[1].inuse = 0x0 fldcontrol[1].refcnt = 0x00 0x00 0x00
0x00
fldoffset[2] = 0x00, fldmask[2] = 0x00, fldvalue_dyna[2]: 0x00 0x00
0x00 0x00
fldcontrol[2].inuse = 0x0 fldcontrol[2].refcnt = 0x00 0x00 0x00
0x00
fldoffset[3] = 0x00, fldmask[3] = 0x00, fldvalue_dyna[3]: 0x00 0x00
0x00 0x00
fldcontrol[3].inuse = 0x0 fldcontrol[3].refcnt = 0x00 0x00 0x00
0x00
fldoffset[4] = 0x00, fldmask[4] = 0x00, fldvalue_dyna[4]: 0x00 0x00
0x00 0x00
fldcontrol[4].inuse = 0x0 fldcontrol[4].refcnt = 0x00 0x00 0x00
0x00
fldoffset[5] = 0x00, fldmask[5] = 0x00, fldvalue_dyna[5]: 0x00 0x00
0x00 0x00
fldcontrol[5].inuse = 0x0 fldcontrol[5].refcnt = 0x00 0x00 0x00
0x00
fldoffset[6] = 0x00, fldmask[6] = 0x00, fldvalue_dyna[6]: 0x00 0x00
0x00 0x00
```

```
fldcontrol[6].inuse = 0x0 fldcontrol[6].refcnt = 0x00 0x00 0x00
0x00
fldoffset[7] = 0x00, fldmask[7] = 0x00, fldvalue_dyna[7]:0x00 0x00
0x00 0x00
fldcontrol[7].inuse = 0x0 fldcontrol[7].refcnt = 0x00 0x00 0x00
0x00
fldoffset[8] = 0x00, fldmask[8] = 0x00, fldvalue_dyna[8]:0x00 0x00
0x00 0x00
fldcontrol[8].inuse = 0x0 fldcontrol[8].refcnt = 0x00 0x00 0x00
0x00
fldoffset[9] = 0x00, fldmask[9] = 0x00, fldvalue_dyna[9]:0x00 0x00
0x00 0x00
fldcontrol[9].inuse = 0x0 fldcontrol[9].refcnt = 0x00 0x00 0x00
0x00
fldoffset[10] = 0x00, fldmask[10] = 0x00, fldvalue_dyna[10]:0x00 0x00
0x00 0x00
fldcontrol[10].inuse = 0x0 fldcontrol[10].refcnt = 0x00 0x00 0x00
0x00
fldoffset[11] = 0x00, fldmask[11] = 0x00, fldvalue_dyna[11]:0x00 0x00
0x00 0x00
fldcontrol[11].inuse = 0x0 fldcontrol[11].refcnt = 0x00 0x00 0x00
0x00
fldoffset[12] = 0x00, fldmask[12] = 0x00, fldvalue_dyna[12]:0x00 0x00
0x00 0x00
fldcontrol[12].inuse = 0x0 fldcontrol[12].refcnt = 0x00 0x00 0x00
0x00
fldoffset[13] = 0x00, fldmask[13] = 0x00, fldvalue_dyna[13]:0x00 0x00
0x00 0x00
fldcontrol[13].inuse = 0x0 fldcontrol[13].refcnt = 0x00 0x00 0x00
0x00
fldoffset[14] = 0x00, fldmask[14] = 0x00, fldvalue_dyna[14]:0x00 0x00
0x00 0x00
fldcontrol[14].inuse = 0x0 fldcontrol[14].refcnt = 0x00 0x00 0x00
0x00
fldoffset[15] = 0x00, fldmask[15] = 0x00, fldvalue_dyna[15]:0x00 0x00
0x00 0x00
fldcontrol[15].inuse = 0x0 fldcontrol[15].refcnt = 0x00 0x00 0x00
0x00
fldoffset[16] = 0x00, fldmask[16] = 0x00, fldvalue_dyna[16]:0x00 0x00
0x00 0x00
fldcontrol[16].inuse = 0x0 fldcontrol[16].refcnt = 0x00 0x00 0x00
0x00
fldoffset[17] = 0x00, fldmask[17] = 0x00, fldvalue_dyna[17]:0x00 0x00
0x00 0x00
fldcontrol[17].inuse = 0x0 fldcontrol[17].refcnt = 0x00 0x00 0x00
0x00
fldoffset[18] = 0x00, fldmask[18] = 0x00, fldvalue_dyna[18]:0x00 0x00
0x00 0x00
fldcontrol[18].inuse = 0x0 fldcontrol[18].refcnt = 0x00 0x00 0x00
0x00
fldoffset[19] = 0x00, fldmask[19] = 0x00, fldvalue_dyna[19]:0x00 0x00
0x00 0x00
fldcontrol[19].inuse = 0x0 fldcontrol[19].refcnt = 0x00 0x00 0x00
0x00
```

Real fields:

fldoffset RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000

fldmask RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000

fld value4 RAM:

0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000

Field dirty indicator: 0x00000000

FDB reference count fdb: 0 [0 0 0 0]
FDB reference count fdb: 1 [0 0 0 0]
FDB reference count fdb: 2 [0 0 0 0]
FDB reference count fdb: 3 [0 0 0 0]
FDB reference count fdb: 4 [0 0 0 0]
FDB reference count fdb: 5 [0 0 0 0]
FDB reference count fdb: 6 [0 0 0 0]
FDB reference count fdb: 7 [0 0 0 0]
FDB reference count fdb: 8 [0 0 0 0]
FDB reference count fdb: 9 [0 0 0 0]
FDB reference count fdb: 10 [0 0 0 0]
FDB reference count fdb: 11 [0 0 0 0]
FDB reference count fdb: 12 [0 0 0 0]
FDB reference count fdb: 13 [0 0 0 0]
FDB reference count fdb: 14 [0 0 0 0]
FDB reference count fdb: 15 [0 0 0 0]
FDB reference count fdb: 16 [0 0 0 0]
FDB reference count fdb: 17 [0 0 0 0]
FDB reference count fdb: 18 [0 0 0 0]
FDB reference count fdb: 19 [0 0 0 0]

Filter counters:

Filter counter 0: 0 (MIRROR1)
Filter counter 1: 0 (MIRROR2)

Filter counter 2: 0 (MIRROR3)
Filter counter 3: 0 (MIRROR4)
Filter counter 4: 0 (AEPORT_NON_MIRR_DROP)
Filter counter 5: 0 (ZONING TRAP)
Filter counter 6: 0 (FCR_EXPORT_DC)
Filter counter 7: 0 (TIN TRAP)
Filter counter 8: 0 (FICON CUP)
Filter counter 9: 0 (FICON CUP DST)
Filter counter 10: 0 (WELL KNOWN ADDR)
Filter counter 11: 0 (SIM)
Filter counter 12: 0 (UNUSED)
Filter counter 13: 0 (UNUSED)
Filter counter 14: 0 (UNUSED)
Filter counter 15: 0 (UNUSED)
Filter counter 16: 0 (PERF1)
Filter counter 17: 0 (PERF2)
Filter counter 18: 0 (PERF3)
Filter counter 19: 0 (PERF4)
Filter counter 20: 0 (PERF5)
Filter counter 21: 0 (PERF6)
Filter counter 22: 0 (PERF7)
Filter counter 23: 0 (PERF8)
Filter counter 24: 0 (PERF9)
Filter counter 25: 0 (PERF10)
Filter counter 26: 0 (PERF11)
Filter counter 27: 0 (PERF12)
Filter counter 28: 0 (OPM1)
Filter counter 29: 0 (OPM2)
Filter counter 30: 0 (IPM1)
Filter counter 31: 0 (IPM2)

ACL DATA

Logical port 12: Hard Zoning disabled, Soft Zoning disabled
Zone type: WWN Zoning
Frames with hard zone miss: 0

*** Please use filterportshow on user port 56 to display ACL hash tables and Mirroring resources of thischip.
***We show this data only for the first physical port which is an external port.

portFcPortCmdShow --slot 0 53 3
doing portFcPortCmdShow: arg1 = 3, arg2 = -2

portshow 53
portDisableReason: None
portCFlags: 0x0
portFlags: 0x4021 PRESENT U_PORT DISABLED LED
LocalSwcFlags: 0x0
portType: 26.0
POD Port: Need license to enable the port
portState: 2 Offline
Protocol: FC

portPhys: 2 No_Module portScn: 2 Offline
port generation number: 0
state transition count: 0

portId: 013500
portIfId: 4302000f
portWwn: 20:35:d8:1f:cc:2c:99:90
portWwn of device(s) connected:
16b Area list:
Distance: normal
portSpeed: N32Gbps

FEC: Inactive
Credit Recovery: Inactive
LE domain: 0
Peer beacon: Off
FC Fastwrite: OFF

| | | | | |
|-------------|---|---------------|---|-------|
| Interrupts: | 0 | Link_failure: | 0 | Frjt: |
| 0 | | | | |
| Unknown: | 0 | Loss_of_sync: | 0 | Fbsy: |
| 0 | | | | |
| Lli: | 0 | Loss_of_sig: | 0 | |
| Proc_rqrd: | 0 | Protocol_err: | 0 | |
| Timed_out: | 0 | Invalid_word: | 0 | |
| Tx_unavail: | 0 | Invalid_crc: | 0 | |
| Delim_err: | 0 | Address_err: | 0 | |
| Lr_in: | 0 | Ols_in: | 0 | |
| Lr_out: | 0 | Ols_out: | 0 | |

portloginshow 53

| Type | PID | World Wide Name | credit | df_sz | cos |
|------|-----|-----------------|--------|-------|-----|
|------|-----|-----------------|--------|-------|-----|

=====

portloginshow 53 -history

| Type | PID | World Wide Name | logout time |
|------|-----|-----------------|-------------|
|------|-----|-----------------|-------------|

=====

portregshow 53

LED registers

=====

| | | | |
|-------------|---------------|----------|-------------|
| 0x81c7a000: | c4_led_status | 00000000 | 0x81c7a004: |
| c4_led_ctl | 00000000 | | |

FPL registers

=====

| | | | |
|------------------|-----------------|----------|-------------|
| 0x81c78200: | fpl_port_config | 23490000 | |
| 0x81c7820c: | fpl_port_id_ctl | 00000000 | 0x81c78210: |
| fpl_port_id_addr | 00013500 | | |
| 0x81c78214: | fpl_port_speed | 00000004 | 0x81c7821c: |
| fpl_lll_ctl | 00000903 | | |

| | | |
|---------------------------------|----------|-------------|
| 0x81c78228: fpl_lli_os_ctl | bc95b5b5 | 0x81c7822c: |
| fpl_lli_send_word | bc95b5b5 | |
| 0x81c78230: fpl_lli_mark_rx | 00000000 | 0x81c78234: |
| fpl_lli_rnd_trip_time | 00000000 | |
| 0x81c78238: fpl_lli_ns_status | 00070007 | 0x81c7823c: |
| fpl_lli_intr_status | 80070007 | |
| 0x81c78244: fpl_lli_def | 00000000 | 0x81c78254: |
| fpl_lli_intr_enable_clr | 00100000 | |
| 0x81c78258: fpl_err_intr_status | 00000000 | 0x81c78260: |
| fpl_err_intr_enable_clr | 00000000 | |
| 0x81c78268: fpl_err_first_error | 00000000 | 0x81c7826c: |
| fpl_speed_neg_ctl | 00000000 | |
| 0x81c78270: fpl_speed_neg_stat | 00000000 | 0x81c78274: |
| fpl_softasn_ctl | 0000000f | |
| 0x81c78278: fpl_link_init_ctl | 00000000 | 0x81c7827c: |
| fpl_link_init_stat | 00000000 | |
| 0x81c78280: fpl_aec_ctl | 00051060 | 0x81c78284: |
| fpl_aec_ctl2 | 04009f60 | |
| 0x81c78288: fpl_pcs_ctl | 00000160 | 0x81c7828c: |
| fpl_fec_ctl | 00000441 | |
| 0x81c78290: fpl_fec_cor | 00000000 | 0x81c78294: |
| fpl_fec_uncor | 00000000 | |
| 0x81c78298: fpl_hss_link_ctl | 0031f040 | 0x81c7829c: |
| fpl_afifo_link_ctl | 00000a86 | |
| 0x81c782a0: fpl_echo_lb_ctl | 0000028c | 0x81c782a4: |
| fpl_scratch | 00000121 | |
| 0x81c782a8: fpl_debug | 00030005 | 0x81c782ac: |
| fpl_misc_debug | 00001800 | |
| 0x00000000: SW_shadow_reg | 00000000 | 0x00000000: |
| SW_c4_phyp->cfgptr | 00030000 | |

per-fpg (per octet) registers

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| | | |
|-------------------------------------|----------|-------------|
| 0x8180b82c: fpg_serdes_ctla0 | 81a37be7 | 0x8180b830: |
| fpg_serdes_ctla1 | 81a37be7 | |
| 0x8180b834: fpg_serdes_ctlb0 | 81a1c3c3 | 0x8180b838: |
| fpg_serdes_ctlb1 | 81a1c3c3 | |
| 0x8180b83c: fpg_serdes_xgmii_1ms | 00067c28 | 0x8180b840: |
| fpg_serdes_regtimctl | 40e47946 | |
| 0x8180b844: fpg_serdes_asnrsttimctl | 00000102 | |

HSS PLL registers

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| | | |
|--|----------|-------------|
| 0x8180b400: 00_hssplla_vco_coarse_cal0 | 00000000 | 0x8180b404: |
| 01_hssplla_vco_coarse_cal1 | 00000014 | |
| 0x8180b408: 02_hssplla_vco_coarse_cal2 | 00000000 | 0x8180b40c: |
| 03_hssplla_vco_coarse_cal3 | 00000000 | |
| 0x8180b410: 04_hssplla_vco_coarse_cal4 | 00000000 | 0x8180b424: |
| 09_hssplla_power_ctl | 00000000 | |
| 0x8180b428: 0A_hssplla_charge_pump_ctl | 00000004 | 0x8180b438: |
| 0E_hssplla_pll_misc_ctl | 00000000 | |
| 0x8180b43c: 0F_hssplla_pclk_ctl | 000000f8 | 0x8180b440: |
| 10_hssplla_eyem_intv_ctl | 00000000 | |
| 0x8180b444: 11_hssplla_eyem_intv_lim1 | 00000000 | 0x8180b448: |

| | | |
|--|----------|-------------|
| 12_hssplla_eyem_intv_lim2 | 00000000 | |
| 0x8180b44c: 13_hssplla_eyem_intv_lim3 | 00000000 | 0x8180b450: |
| 14_hssplla_eyem_intv_lim4 | 00000000 | |
| 0x8180b4f0: 3C_hssplla_macro_tst_ctl4 | 00000000 | 0x8180b4f4: |
| 3D_hssplla_macro_tst_ctl3 | 00000000 | |
| 0x8180b4f8: 3E_hssplla_macro_tst_ctl2 | 00000000 | 0x8180b4fc: |
| 3F_hssplla_macro_tst_ctl1 | 00000000 | |
| 0x8180b500: 00_hssppll_vco_coarse_cal0 | 0000000a | 0x8180b504: |
| 01_hssppll_vco_coarse_cal1 | 00000014 | |
| 0x8180b508: 02_hssppll_vco_coarse_cal2 | 00000000 | 0x8180b50c: |
| 03_hssppll_vco_coarse_cal3 | 00000000 | |
| 0x8180b510: 04_hssppll_vco_coarse_cal4 | 00000000 | 0x8180b524: |
| 09_hssppll_power_ctl | 00000000 | |
| 0x8180b528: 0A_hssppll_charge_pump_ctl | 00000004 | 0x8180b538: |
| 0E_hssppll_pll_misc_ctl | 00000000 | |
| 0x8180b53c: 0F_hssppll_pclk_ctl | 000000f8 | 0x8180b540: |
| 10_hssppll_eyem_intv_ctl | 00000000 | |
| 0x8180b544: 11_hssppll_eyem_intv_lim1 | 00000000 | 0x8180b548: |
| 12_hssppll_eyem_intv_lim2 | 00000000 | |
| 0x8180b54c: 13_hssppll_eyem_intv_lim3 | 00000000 | 0x8180b550: |
| 14_hssppll_eyem_intv_lim4 | 00000000 | |
| 0x8180b5f0: 3C_hssppll_macro_tst_ctl4 | 00000000 | 0x8180b5f4: |
| 3D_hssppll_macro_tst_ctl3 | 00000000 | |
| 0x8180b5f8: 3E_hssppll_macro_tst_ctl2 | 00000000 | 0x8180b5fc: |
| 3F_hssppll_macro_tst_ctl1 | 00000000 | |

HSS TX registers

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| | | |
|--------------------------------------|----------|-------------|
| 0x8180a500: 00_hsstx_cfg_mode_PHY | 00009f48 | 0x8180a504: |
| 01_hsstx_test_ctl | 00000000 | |
| 0x8180a508: 02_hsstx_coeff_ctl_INV | 00000000 | 0x8180a50c: |
| 03_hsstx_drv_mode_ctl | 00000000 | |
| 0x8180a510: 04_hsstx_drv_ovrd_ctl | 00000010 | 0x8180a514: |
| 05_hsstx_dclk_align_ovrd | 00000080 | |
| 0x8180a518: 06_hsstx_imp_cal_ovrd | 00000c0c | 0x8180a51c: |
| 07_hsstx_dclk_drift_tol | 00000004 | |
| 0x8180a520: 08_hsstx_tap0_coeff_TUNE | 00000000 | 0x8180a524: |
| 09_hsstx_tap1_coeff_TUNE | 00000003 | |
| 0x8180a528: 0A_hsstx_tap2_coeff_TUNE | 00000018 | 0x8180a52c: |
| 0B_hsstx_tap3_coeff_TUNE | 0000000d | |
| 0x8180a534: 0D_hsstx_pol_INV | 0000000a | 0x8180a538: |
| 0E_hsstx_ae_cmd | 00000000 | |
| 0x8180a53c: 0F_hsstx_ae_stat | 00000000 | 0x8180a540: |
| 10_hsstx_ae_tap0_TUNE | 00000000 | |
| 0x8180a544: 11_hsstx_ae_tap1_TUNE | 00000000 | 0x8180a548: |
| 12_hsstx_ae_tap2_TUNE | 00000028 | |
| 0x8180a54c: 13_hsstx_ae_tap3_TUNE | 00000000 | 0x8180a554: |
| 15_hsstx_app_tune | 0000120e | |
| 0x8180a558: 16_hsstx_analog_diag | 00000000 | 0x8180a560: |
| 18_hsstx_4x_seg_app | 0000aafa | |
| 0x8180a564: 19_hsstx_2x_seg_app | 00000000 | 0x8180a568: |
| 1A_hsstx_1x_seg_app | 0000ff5d | |
| 0x8180a56c: 1B_hsstx_seg_4x_term_app | 00000000 | 0x8180a570: |
| 1C_hsstx_seg_2x1x_term_app | 00000f00 | |

| | | | |
|-------------|-------------------------------|----------|-------------|
| 0x8180a574: | 1D_hsstx_tap_sign_app | 0000000a | 0x8180a578: |
| | 1E_hsstx_ext_addr_data | 00000001 | |
| 0x8180a57c: | 1F_hsstx_ext_addr_addr | 00000000 | 0x8180a580: |
| | 20_hsstx_pat_buf_bytes_1_0 | 00000000 | |
| 0x8180a584: | 21_hsstx_pat_buf_bytes_3_2 | 00000000 | 0x8180a588: |
| | 22_hsstx_pat_buf_bytes_5_4 | 00000000 | |
| 0x8180a58c: | 23_hsstx_pat_buf_bytes_7_6 | 00000000 | 0x8180a59c: |
| | 27_hsstx_8023az_ctl | 00000000 | |
| 0x8180a5a0: | 28_hsstx_dcc_ctl | 000060c0 | 0x8180a5a4: |
| | 29_hsstx_dcc_ovrd | 00000000 | |
| 0x8180a5a8: | 2A_hsstx_dcc_app | 00000107 | 0x8180a5ac: |
| | 2B_hsstx_dcc_timeout | 0000ffff | |
| 0x8180a5c0: | 30_hsstx_tap_sign_ovrd | 00000000 | 0x8180a5c8: |
| | 32_hsstx_seg_4x_ovrd | 00000000 | |
| 0x8180a5cc: | 33_hsstx_seg_2x_ovrd | 00000000 | 0x8180a5d0: |
| | 34_hsstx_seg_1x_ovrd | 00000000 | |
| 0x8180a5d8: | 36_hsstx_tap_seg_4x_term_ovrd | 00000000 | 0x8180a5dc: |
| | 37_hsstx_tap_seg_2x_term_ovrd | 00000000 | |
| 0x8180a5e0: | 38_hsstx_tap_seg_1x_term_ovrd | 00000000 | 0x8180a5ec: |
| | 3B_hsstx_mac_test_ctl5 | 00000000 | |
| 0x8180a5f0: | 3C_hsstx_mac_test_ctl4 | 00000000 | 0x8180a5f4: |
| | 3D_hsstx_mac_test_ctl3 | 00000000 | |
| 0x8180a5f8: | 3E_hsstx_mac_test_ctl2 | 00000000 | 0x8180a5fc: |
| | 3F_hsstx_mac_test_ctl1 | 000000c6 | |

HSS RX registers

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| | | | |
|-------------|---------------------------------|----------|-------------|
| 0x8180a700: | 00_hssrx_cfg_mode_PHY | 00009e78 | 0x8180a704: |
| | 01_hssrx_test_ctl | 00000000 | |
| 0x8180a708: | 02_hssrx_phs_rot_ctl | 0000cb80 | 0x8180a70c: |
| | 03_hssrx_phs_rot_ofs_ctl | 00000610 | |
| 0x8180a710: | 04_hssrx_phs_rot_posn1 | 00002120 | 0x8180a714: |
| | 05_hssrx_phs_rot_posn2 | 00000011 | |
| 0x8180a718: | 06_hssrx_phs_rot_sta_ofs1 | 00000100 | 0x8180a71c: |
| | 07_hssrx_phs_rot_sta_ofs2 | 0000001f | |
| 0x8180a720: | 08_hssrx_dfe_ctl_PHY | 00002002 | 0x8180a724: |
| | 09_hssrx_dfe_smpl_snap1 | 00000000 | |
| 0x8180a728: | 0A_hssrx_dfe_smpl_snap2 | 00008000 | 0x8180a72c: |
| | 0B_hssrx_vga_ctl1 | 000041f4 | |
| 0x8180a730: | 0C_hssrx_vga_ctl2 | 00007aa0 | 0x8180a734: |
| | 0D_hssrx_vga_ctl3 | 000009e4 | |
| 0x8180a738: | 0E_hssrx_pwr_mgmt_ctl | 0000001f | 0x8180a73c: |
| | 0F_hssrx_iqamp_ctl1 | 00000019 | |
| 0x8180a740: | 10_hssrx_iqamp_ctl2 | 00000001 | 0x8180a744: |
| | 11_hssrx_dacap_dacan_sel | 00000003 | |
| 0x8180a748: | 12_hssrx_dacap_dacan | 00000201 | 0x8180a74c: |
| | 13_hssrx_daca_min | 00000000 | |
| 0x8180a750: | 14_hssrx_adac_ctl | 00000001 | 0x8180a754: |
| | 15_hssrx_ac_cp_ctl | 000031c3 | |
| 0x8180a758: | 16_hssrx_ac_cp_val | 00008051 | 0x8180a75c: |
| | 17_hssrx_dfe_h1h2h3_lcl_off_ch | 00000014 | |
| 0x8180a760: | 18_hssrx_dfe_h1h2h3_lcl_off_val | 00000000 | 0x8180a764: |
| | 19_hssrx_peaked_intg | 000000ff | |
| 0x8180a768: | 1A_hssrx_cdr_analog_sw | 0000ce00 | 0x8180a76c: |

| | | | |
|--|----------|----------------|-------------|
| 1B_hssrx_peaking_amp_init_c_PHY | 00000000 | | |
| 0x8180a770: 1C_hssrx_dac_dpc | | 00000040 | 0x8180a774: |
| 1D_hssrx_ddc | 00000000 | | |
| 0x8180a778: 1E_hssrx_int_stat_PHY | | 00000c0f | 0x8180a77c: |
| 1F_hssrx_dfe_func_ctl1_PHY | 0000ffff | | |
| 0x8180a780: 20_hssrx_dfe_func_ctl2_INV | | 00007ebf | 0x8180a784: |
| 21_hssrx_ofs_ch_dcc_qcc_idx | 00002000 | | |
| 0x8180a788: 22_hssrx_dfe_ofs_val | | 0000797f | 0x8180a78c: |
| 23_hssrx_h_coeff_bist | 00000401 | | |
| 0x8180a790: 24_hssrx_ac_cap_bist | | 00000000 | 0x8180a794: |
| 25_hssrx_max_gain_path_idx_res | 00007800 | | |
| 0x8180a798: 26_hssrx_loff_ctl | | 00000054 | 0x8180a79c: |
| 27_hssrx_sigdet_ctl | 00004180 | | |
| 0x8180a7a0: 28_hssrx_ana_ctl_sw | | 00000000 | 0x8180a7a4: |
| 29_hssrx_intg_dac_ofs | 0000acaf | | |
| 0x8180a7a8: 2A_hssrx_eye_ctl | | 00000000 | 0x8180a7ac: |
| 2B_hssrx_eye_met | 00000004 | | |
| 0x8180a7b0: 2C_hssrx_eye_met_err_cnt | | 00000000 | 0x8180a7b4: |
| 2D_hssrx_eye_met_pdf_eyec | 00000000 | | |
| 0x8180a7b8: 2E_hssrx_eye_met_pat_len | | 0000007f | 0x8180a7bc: |
| 2F_hssrx_dfe_func_ctl3 | 0000dfff | | |
| 0x8180a7c0: 30_hssrx_dfe_tap_ctl_idx_ptr | | 00000008 | 0x8180a7c4: |
| 31_hssrx_dfe_tap | 00003030 | | |
| 0x8180a7c8: 32_hssrx_lte_ctl_TUNE | | 00001601 | 0x8180a7e4: |
| 39_hssrx_int_stat2 | 000041ff | | |
| 0x8180a7e8: 3A_hssrx_ac_cpl_cur_src_adj | | 00000042 | 0x8180a7ec: |
| 3B_hssrx_dcd_ctl | 00007c81 | | |
| 0x8180a7f0: 3C_hssrx_dcc_ctl | | 00000d82 | 0x8180a7f4: |
| 3D_hssrx_qcc_ctl | 00006984 | | |
| 0x8180a7f8: 3E_hssrx_mac_test_ctl2 | | 00000000 | 0x8180a7fc: |
| 3F_hssrx_mac_test_ctl1 | 00000000 | | |
| 0x8180a748: 12_hssrx_dacap_dacan[02] | | 0200 0201 | |
| 0x8180a760: 18_hssrx_dfe_h1h2h3_lcl_off_va[00] | | 0000 0000 0000 | |
| 0000 0000 0000 0000 0000 | | | |
| 0x8180a760: 18_hssrx_dfe_h1h2h3_lcl_off_va[08] | | 0000 0000 0000 | |
| 0000 0000 0000 0000 0000 | | | |
| 0x8180a760: 18_hssrx_dfe_h1h2h3_lcl_off_va[16] | | 0000 0000 0000 | |
| 0000 0000 | | | |
| 0x8180a788: 22_hssrx_dfe_ofs_val[00][00] | | 797f 0000 | 077d |
| 7f00 0509 7f7f | | | |
| 0x8180a788: 22_hssrx_dfe_ofs_val[03][00] | | 0707 7f7f | 7c07 |
| 007f 7b01 0000 | | | |
| 0x8180a788: 22_hssrx_dfe_ofs_val[06][00] | | 037b 0000 | 0b7f |
| 7f00 0b7f 7f00 | | | |
| 0x8180a788: 22_hssrx_dfe_ofs_val[09][00] | | 7e7d 0000 | 7a7b |
| 0000 0079 0000 | | | |
| 0x8180a788: 22_hssrx_dfe_ofs_val[12][00] | | 7e7b 0000 | 057d |
| 0000 7d04 0000 | | | |
| 0x8180a788: 22_hssrx_dfe_ofs_val[15][00] | | 7f02 007f | 7f7b |
| 7f00 017d 0000 | | | |
| 0x8180a788: 22_hssrx_dfe_ofs_val[18][00] | | 017f 0000 | 7f7f |
| 0000 007d 0000 | | | |
| 0x8180a788: 22_hssrx_dfe_ofs_val[21][00] | | 007d 0000 | 007d |
| 0000 007d 0000 | | | |

```

0x8180a788: 22_hssrx_dfe_ofs_val[24][00]          0306 007f 7d0c
007f 7e00 0000
0x8180a794: 25_hssrx_max_gain_path_idx_res[00]    005a 0855 1007
1887 20f0 28ba 30a2 3800
0x8180a794: 25_hssrx_max_gain_path_idx_res[08]    40e0 48a5 5090
5800 6044 6804 7000 7800
0x8180a7c4: 31_hssrx_dfe_tap[00]                  fffe 8080 0000
0000 0030 0030 3030 3030
0x8180a7c4: 31_hssrx_dfe_tap[08]                  3030 3030 3030
0000
0x8180a7e8: 3A_hssrx_ac_cpl_cur_src_adj[00]       0042 0042 0042
0042
0x8180a7ec: 3B_hssrx_dcd_ctl[00]                  7c81 5c00 7c00
5c00 7c81
0x8180a7f0: 3C_hssrx_dcc_ctl[00]                  0d82 0d81 0d81
0d42
0x8180a7f4: 3D_hssrx_qcc_ctl[00]                  6946 6984

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xfipcs, fec, aec, & aet registers

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```

0x81c78400: xfipcs_reg [00] 00002040 00000080 00000000
00000000 00000001 00000008 00000000 00000000
0x81c78420: xfipcs_reg [08] 00008c01 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c78440: xfipcs_reg [16] 00000000 00000000 00000000
00000000 00000040 00000000 00000000 00000000
0x81c78460: xfipcs_reg [24] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c78480: xfipcs_reg [32] 00000004 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c78620: fec_32g_128g_reg [08] 00000000 00000000 00000000
00000000 00000000 00000000 00000000
0x81c78648: fec_32g_128g_reg [18] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c78a00: aec_reg [00] 00000000 00000000 00000000
00000000 00000000 00000000 00000000
0x81c78c00: aet_reg [00] 00000000 00000000 00000000
00000000 00000000

```

bbc registers

=====

```

0x81c79800: bbc_trc 0 0 0 0 0 0 0
0
0x81c79840: bbc_trc 0 0 0 0 0 0 0
0
0x81c79880: bbc_trc 0 0 0 0 0 0 0
0
0x81c798c0: bbc_trc 0 0 0 0 0 0 0
0
0x81c79900: bbc_trc 0 0 0 0 0 0 0
0
0x81c79804: bbc_mbc 0 0 0 0 0 0 0
0
0x81c79844: bbc_mbc 0 0 0 0 0 0 0

```

| | | | | | | | |
|-------------------------|-------------------------|----------|---|---|---|---|----------------------|
| 0 | | | | | | | |
| 0x81c79884: | bbc_mbc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c798c4: | bbc_mbc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c79904: | bbc_mbc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c79a00: | bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c79a20: | bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c79a40: | bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c79a60: | bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c79a80: | bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c79c00: | bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c79c20: | bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c79c40: | bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c79c60: | bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c79c80: | bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c79d00: | bbc_fbpc | 00000000 | | | | | 0x81c79d04: bbc_csc |
| 00000000 | | | | | | | |
| 0x81c79d08: | bbc_rcc_inc | 00000000 | | | | | 0x81c79d0c: |
| bbc_rqc_inc | 00000000 | | | | | | |
| 0x81c79d10: | bbc_fbpc_inc | 00000000 | | | | | 0x81c79d14: |
| bbc_tmc_inc | 00000000 | | | | | | |
| 0x81c79d18: | bbc_threshold | 00080100 | | | | | 0x81c79d1c: |
| bbc_counter_clr | 00000000 | | | | | | |
| 0x81c79d20: | bbc_debug_en | 00000000 | | | | | 0x81c79d24: bbc_ctrl |
| 00200020 | | | | | | | |
| 0x81c79d28: | bbc_rqc_rcc_thresh | 00000055 | | | | | 0x81c79d34: |
| bbc_bb_sc_n | 00000000 | | | | | | |
| 0x81c79d38: | bbc_crd_reco_debug | 00000000 | | | | | 0x81c79d3c: |
| bbc_crd_reco_debug_data | 00000000 | | | | | | |
| 0x81c79d40: | bbc_multi_frm_loss_cnt | 00000000 | | | | | 0x81c79d44: |
| bbc_multi_rdy_loss_cnt | 00000000 | | | | | | |
| 0x81c79d48: | bbc_1frm_loss_recov_cnt | 00000000 | | | | | 0x81c79d4c: |
| bbc_1rdy_loss_recov_cnt | 00000000 | | | | | | |
| 0x81c79d58: | bbc_int_status | 00000000 | | | | | 0x81c79d5c: |
| bbc_int_set | 00000000 | | | | | | |
| 0x81c79d60: | bbc_int_first | 00000000 | | | | | 0x81c79d64: |
| bbc_frm_rdy_rx_err_addr | 00000000 | | | | | | |
| 0x81c79d68: | bbc_frm_rdy_tx_err_addr | 00000000 | | | | | 0x81c79d6c: |
| bbc_trc_mbc_err_addr | 00000000 | | | | | | |
| 0x81c79d70: | bbc_frm_rdy_rx_dbl_ecc | 00000000 | | | | | 0x81c79d74: |
| bbc_frm_rdy_tx_dbl_ecc | 00000000 | | | | | | |
| 0x81c79d78: | bbc_trc_mbc_dbl_ecc | 00000000 | | | | | |

| | | |
|-----------------------------|----------|-------------|
| 0x81c79d7c: bbc_fsm_status | 00001011 | 0x81c79d80: |
| bbc_force_err | 00000000 | |
| 0x81c79d84: bbc_crdt_avail0 | ffffffff | 0x81c79d88: |
| bbc_crdt_avail1 | 000000ff | |
| 0x81c79d8c: bbc_scratch | 00000000 | |

FPS registers

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| | | |
|--------------------------------|----------|-------------|
| 0x81c78004: fps_er_enc_in | 00000000 | 0x81c78008: |
| fps_er_crc | 00000000 | |
| 0x81c7800c: fps_er_trunc | 00000000 | 0x81c78010: |
| fps_er_toolong | 00000000 | |
| 0x81c78014: fps_er_bad_eof | 00000000 | 0x81c78018: |
| fps_er_enc_out | 00000000 | |
| 0x81c7801c: fps_er_bad_os | 00000000 | 0x81c78020: |
| fps_er_flush | 00000000 | |
| 0x81c78024: fps_er_ifg | 00000000 | 0x81c78038: |
| fps_er_crc_good_eof | 00000000 | |
| 0x81c7803c: fps_inv_arb | 00000000 | 0x81c78040: |
| fps_slow_sts_status | 00000000 | |
| 0x81c78044: fps_tx_frm_cnt | 00000000 | 0x81c78048: |
| fps_rx_frm_cnt | 00000000 | |
| 0x81c78050: fps_tx_word_cnt_hi | 00000000 | 0x81c7804c: |
| fps_tx_word_cnt_lo | 00000000 | |
| 0x81c78058: fps_rx_word_cnt_hi | 00000000 | 0x81c78054: |
| fps_rx_word_cnt_lo | 00000000 | |

BAL registers

=====

| | | |
|---------------------------------|----------|-------------|
| 0x81c7f000: bal_desired_buf | 00000000 | 0x81c7f004: |
| bal_alloc_buf | 00000000 | |
| 0x81c7f008: bal_busy_buf | 00000000 | 0x81c7f00c: |
| bal_usable_buf | 00000000 | |
| 0x81c7f010: bal_max_bor_buf | 00000000 | |
| 0x81c7f014: bal_busy_buf_thresh | 00000002 | |

TXQ registers

=====

| | | |
|-------------------------------------|------------------------|--|
| 0x81c7b004: txq_phys_port_ctl | 00470000 | |
| 0x81c7b050: txq_link_skew | 00000000 | |
| 0x81c7b068: txq_cr_lk_dttm_intr_sts | [00] 00000000 00000000 | |
| 0x81c7b070: txq_cr_lk_dttm_intr_en | [00] 00000000 00000000 | |
| 0x81c7b024: txq_disc_frm_trap_cnt | 00000014 | |

FDS registers

=====

| | | |
|------------------------------------|----------|-------------|
| 0x81c7c000: fds_rxf_ctl | 00000002 | 0x81c7c004: |
| fds_rxf_wait_thresh | 00000909 | |
| 0x81c7c018: fds_rxf_first_error | 00000000 | 0x81c7c01c: |
| fds_rxf_first_error_info | 00000000 | |
| 0x81c7c020: fds_rxf_inout_pkt_cnt | 00000000 | |
| 0x81c7c008: fds_rxf_err_int_status | 00000000 | 0x81c7c024: |
| fds_rxf_fifo_status | 00888888 | |
| 0x81c7d000: fds_txf_ctl | 0000003a | 0x81c7d004: |


```

fds_txf_wait_ifg_thresh 00a00106
0x81c7d008: fds_txf_err_int_status 00000000 0x81c7d024:
fds_txf_fifo_status 00088888
0x81c7d02c: fds_txf_bbc_scs 00000000

```

Logical TXQ registers

=====

```

0x81c7b000: txq_log_port_ctl 00000002 0x81c7b008:
txq_port_status 00000000
0x81c7b00c: txq_todo_flags [00] 00000000 00000000
0x81c7b014: txq_spd_match_desc [00] 00000000 00000000 00000000
00000000
0x81c7b024: txq_spd_match_desc [04] 00000014
0x81c7b028: txq_vc_weight [00] 01010101 01010101 01010101
01010101
0x81c7b038: txq_vc_weight [04] 01010101 01010101 01010101
01010101
0x81c7b048: txq_vc_weight [08] 01010101 00010101
0x81c7b054: txq_cong_dttm_ctrl 00000000
0x81c7b058: txq_cong_dttm_intr_sts [00] 00000000 00000000
0x81c7b060: txq_cong_dttm_intr_en [00] 00000000 00000000
0x81c7b078: txq_bw_limit_en_reg [00] 00000000 00000000
0x81c7b080: txq_bw_gua_en_reg [00] 00000000 00000000
0x81c7b088: txq_vc_group [00] 03030300 03030303 03030303
03030303
0x81c7b098: txq_vc_group [04] 03030303 03030303 03030303
03030303
0x81c7b0a8: txq_vc_group [08] 03030303 03030303 00000000
00000000
0x81c7b0b0: txq_bw_thresh_group [00] 00000000 00000000 00000000
00000000
0x81c7b0c0: txq_bw_thresh_group [04] 00000000 00000000 00000000
00000000
0x81c7b0d0: txq_bw_thresh_group [08] 00000000 00000000 00000000
00000000
0x81c7b0e0: txq_bw_thresh_group [12] 00000000 00000000 00000000
00000000
0x81c7b0f0: txq_bw_thresh_group [16] 00000000 00000000 00000000
00000000
0x81c7b100: txq_bw_thresh_group [20] 00000000 00000000 00000000
00000000
0x81c7b110: txq_bw_thresh_group [24] 00000000 00000000 00000000
00000000
0x81c7b120: txq_bw_thresh_group [28] 00000000 00000000 00000000
00000000
0x81c7b130: txq_bw_thresh_group [32] 00000000 00000000 00000000
00000000
0x81c7b140: txq_bw_thresh_group [36] 00000000 00000000 00000000
00000000

```

txq Congestion detection Statistics RAM

=====

```

0x81090960: vc[0] 00000000 0x81090964: vc[1]
00000000

```

| | | |
|--------------------|----------|--------------------|
| 0x81090968: vc[2] | 00000000 | 0x8109096c: vc[3] |
| 00000000 | | |
| 0x81090970: vc[4] | 00000000 | 0x81090974: vc[5] |
| 00000000 | | |
| 0x81090978: vc[6] | 00000000 | 0x8109097c: vc[7] |
| 00000000 | | |
| 0x81090980: vc[8] | 00000000 | 0x81090984: vc[9] |
| 00000000 | | |
| 0x81090988: vc[10] | 00000000 | 0x8109098c: vc[11] |
| 00000000 | | |
| 0x81090990: vc[12] | 00000000 | 0x81090994: vc[13] |
| 00000000 | | |
| 0x81090998: vc[14] | 00000000 | 0x8109099c: vc[15] |
| 00000000 | | |
| 0x810909a0: vc[16] | 00000000 | 0x810909a4: vc[17] |
| 00000000 | | |
| 0x810909a8: vc[18] | 00000000 | 0x810909ac: vc[19] |
| 00000000 | | |
| 0x810909b0: vc[20] | 00000000 | 0x810909b4: vc[21] |
| 00000000 | | |
| 0x810909b8: vc[22] | 00000000 | 0x810909bc: vc[23] |
| 00000000 | | |
| 0x810909c0: vc[24] | 00000000 | 0x810909c4: vc[25] |
| 00000000 | | |
| 0x810909c8: vc[26] | 00000000 | 0x810909cc: vc[27] |
| 00000000 | | |
| 0x810909d0: vc[28] | 00000000 | 0x810909d4: vc[29] |
| 00000000 | | |
| 0x810909d8: vc[30] | 00000000 | 0x810909dc: vc[31] |
| 00000000 | | |
| 0x810909e0: vc[32] | 00000000 | 0x810909e4: vc[33] |
| 00000000 | | |
| 0x810909e8: vc[34] | 00000000 | 0x810909ec: vc[35] |
| 00000000 | | |
| 0x810909f0: vc[36] | 00000000 | 0x810909f4: vc[37] |
| 00000000 | | |
| 0x810909f8: vc[38] | 00000000 | 0x810909fc: vc[39] |
| 00000000 | | |

Logical STS registers

=====

| | | |
|----------------------------------|----------------------------|------------------------------|
| 0x81584bc4: sts_ftb_type1_miss | 00000000 | |
| 0x81584bc8: sts_ftb_type2_miss | 00000000 | |
| 0x81584bcc: sts_ftb_type6_miss | 00000000 | |
| 0x81584bd0: sts_hard_zoning_miss | 00000000 | |
| 0x81584bd4: sts_lun_zoning_miss | 00000000 | |
| 0x81584bdc: sts_unroutable | 00000000 | |
| 0x81581bf4: sts_rte_cl2 | 00000000 | 0x81581bf8: |
| sts_rte_cl3 | 00000000 | 0x81581bfc: sts_rte_link_ctl |
| 00000000 | 0x81584be8: sts_tx_timeout | 00000000 |

Logical STS filter registers

=====

| | | | | |
|--------------------------|------|----------|----------|----------|
| 0x81584b40: sts_flt_trig | [00] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584b50: sts_flt_trig | [04] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584b60: sts_flt_trig | [08] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584b70: sts_flt_trig | [12] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584b80: sts_flt_trig | [16] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584b90: sts_flt_trig | [20] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584ba0: sts_flt_trig | [24] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584bb0: sts_flt_trig | [28] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584bc0: sts_flt_trig | [32] | | | |

Logical STS discard registers

=====

| | | |
|------------------------------------|----------|-------------|
| 0x815825cc: disc_mcast_wka | 00000000 | 0x815825d0: |
| disc_inv_did | 00000000 | |
| 0x815825d4: disc_cl1_cl4 | 00000000 | 0x815825d8: |
| disc_sid_chk_fail | 00000000 | |
| 0x815825dc: disc_inv_dom_egid_txpt | 00000000 | 0x815825e0: |
| disc_vft_hop_cnt_1 | 00000000 | |
| 0x815825e4: disc_classf | 00000000 | 0x815825e8: |
| disc_fcp_cdb_inv | 00000000 | |
| 0x815825ec: disc_vfid_trap_enabled | 00000000 | 0x815825f0: |
| disc_vfid_hdr_chk_fail | 00000000 | |
| 0x815825f4: disc_shim_cksum_fail | 00000000 | 0x815825f8: |
| disc_fed_edit_cmd_err | 00000000 | |
| 0x815825fc: disc_ftb_vm_mode | 00000000 | 0x81582600: |
| disc_ftb_agnt2_miss | 00000000 | |
| 0x81582604: disc_ecb_reserved | 00000000 | 0x81582608: |
| disc_ecb_de_pad_err | 00000000 | |
| 0x8158260c: disc_ecb_de_tag_err | 00000000 | 0x81582610: |
| disc_ecb_de_seq_err | 00000000 | |
| 0x81582614: disc_ecb_err | 00000000 | 0x81582618: |
| disc_ftb_type4_match | 00000000 | |
| 0x8158261c: disc_fcp_rsp_ftb_type4 | 00000000 | 0x81582620: |
| disc_ftb_type5_match | 00000000 | |
| 0x81582624: disc_ftb_type3_match | 00000000 | 0x81582628: |
| disc_els_ftb_type3 | 00000000 | |
| 0x8158262c: disc_ftb_type1_match | 00000000 | 0x81582630: |
| disc_els_rsp_ex_port | 00000000 | |
| 0x81582634: disc_inv_drpdps | 00000000 | 0x81582638: |
| disc_did_lookup_miss | 00000000 | |
| 0x8158263c: disc_ftb_type2_match | 00000000 | 0x81582640: |
| disc_trpd_plogi_pdisc | 00000000 | |
| 0x81582644: disc_type2_lookup_miss | 00000000 | 0x81582648: |
| disc_ftb_type6_match | 00000000 | |
| 0x8158264c: disc_els_rep_ex_port | 00000000 | 0x81582650: |
| disc_els_sid_lkup_bit1 | 00000000 | |

```

0x81582654: disc_els_sid_lkup_bit0 00000000 0x81582658:
disc_bls_frm_trap_bit1 00000000
0x8158265c: disc_ftb_token_err 00000000 0x81582660:
disc_asic_internal_err 00000000
0x81582664: disc_hard_zone_miss 00000000 0x81582668:
disc_lun_zone_miss 00000000
0x8158266c: disc_flt_frame_disc 00000000 0x81582670:
disc_flt_parity_err 00000000
0x81582674: disc_frame_marked_du 00000000 0x81582678:
disc_frame_marked_to 00000000
0x8158267c: disc_lkup_rte_prty_err 00000000

```

portstatsshow 53

```

stat_wtx 0 4-byte words transmitted
stat_wrx 0 4-byte words received
stat_ftx 0 Frames transmitted
stat_frx 0 Frames received
stat_c2_frx 0 Class 2 frames received
stat_c3_frx 0 Class 3 frames received
stat_lc_rx 0 Link control frames
received
stat_mc_rx 0 Multicast frames
received
stat_mc_to 0 Multicast timeouts
stat_mc_tx 0 Multicast frames
transmitted
tim_txcrd_z 0 Time TX Credit Zero
(2.5Us ticks)
tim_txcrd_z_vc 0- 3: 0 0 0 0
tim_txcrd_z_vc 4- 7: 0 0 0 0
tim_txcrd_z_vc 8-11: 0 0 0 0
tim_txcrd_z_vc 12-15: 0 0 0 0
lat_tot_pkt_vc 0- 3: 1 1 1 1
lat_tot_pkt_vc 4- 7: 1 1 1 1
lat_tot_pkt_vc 8-11: 1 1 1 1
lat_tot_pkt_vc 12-15: 1 1 1 1
lat_hi_time_vc 0- 3: 0 0 0 0
lat_hi_time_vc 4- 7: 0 0 0 0
lat_hi_time_vc 8-11: 0 0 0 0
lat_hi_time_vc 12-15: 0 0 0 0
lat_lo_time_vc 0- 3: 1 1 1 1
lat_lo_time_vc 4- 7: 1 1 1 1
lat_lo_time_vc 8-11: 1 1 1 1
lat_lo_time_vc 12-15: 1 1 1 1
max_latency_vc 0- 3: 1 1 1 1
max_latency_vc 4- 7: 1 1 1 1
max_latency_vc 8-11: 1 1 1 1
max_latency_vc 12-15: 1 1 1 1
latency_dma_ts 09-09-2024 UTC Mon 08:47:26 TXQ
Latency DMA TimeStamp
fec_cor_detected 0 Count of blocks that
were corrected by FEC
fec_uncor_detected 0 Count of blocks that

```

```

were left uncorrected by FEC
er_enc_in           0           Encoding errors inside
of frames
er_crc              0           Frames with CRC errors
er_trunc            0           Frames shorter than
minimum
er_toolong          0           Frames longer than
maximum
er_bad_eof          0           Frames with bad end-of-
frame
er_enc_out          0           Encoding error outside
of frames
er_bad_os           0           Invalid ordered set
er_pcs_blk          0           PCS block errors
er_rx_c3_timeout    0           Class 3 receive frames
discarded due to timeout
er_tx_c3_timeout    0           Class 3 transmit frames
discarded due to timeout
er_unroutable       0           Frames that are
unroutable
er_unreachable      0           Frame with unreachable
destination
er_other_discard    0           Other discards
er_type1_miss       0           frames with FTB type 1
miss
er_type2_miss       0           frames with FTB type 2
miss
er_type6_miss       0           frames with FTB type 6
miss
er_zone_miss        0           frames with hard zoning
miss
er_lun_zone_miss    0           frames with LUN zoning
miss
er_crc_good_eof     0           Crc error with good eof
er_inv_arb          0           Invalid ARB
er_single_credit_loss 0           Single vcrdy/frame loss
on link
er_multi_credit_loss 0           Multiple vcrdy/frame
loss on link
other_credit_loss   0           Link timeout/complete
credit loss
phy_stats_clear_ts   09-06-2024 UTC Fri 08:30:19   Timestamp of
phy_port stats clear
lgc_stats_clear_ts   09-06-2024 UTC Fri 08:30:19   Timestamp of
lgc_port stats clear
fec_corrected_rate   0           FEC Corrected blocks per
second

```

```
portstats64show 53
```

```

stat64_wtx          0           top_int : 4-byte words transmitted
                                0           bottom_int : 4-byte words transmitted
stat64_wrx          0           top_int : 4-byte words received
                                0           bottom_int : 4-byte words received
stat64_ftx          0           top_int : Frames transmitted

```

| | | |
|------------------------------|---|--|
| stat64_frx | 0 | bottom_int : Frames transmitted |
| | 0 | top_int : Frames received |
| stat64_c2_frx | 0 | bottom_int : Frames received |
| | 0 | top_int : Class 2 frames received |
| stat64_c3_frx | 0 | bottom_int : Class 2 frames received |
| | 0 | top_int : Class 3 frames received |
| stat64_lc_rx | 0 | bottom_int : Class 3 frames received |
| | 0 | top_int : Link control frames received |
| received | 0 | bottom_int : Link control frames |
| stat64_mc_rx | 0 | top_int : Multicast frames received |
| | 0 | bottom_int : Multicast frames received |
| stat64_mc_to | 0 | top_int : Multicast timeouts |
| | 0 | bottom_int : Multicast timeouts |
| stat64_mc_tx | 0 | top_int : Multicast frames transmitted |
| | 0 | bottom_int : Multicast frames |
| transmitted | | |
| tim64_rdy_pri | 0 | top_int : Time R_RDY high priority |
| | 0 | bottom_int : Time R_RDY high priority |
| tim64_txcrd_z | 0 | top_int : Time BB_credit zero |
| | 0 | bottom_int : Time BB_credit zero |
| er64_enc_in | 0 | top_int : Encoding errors inside of |
| frames | 0 | bottom_int : Encoding errors inside of |
| frames | | |
| er64_crc | 0 | top_int : Frames with CRC errors |
| | 0 | bottom_int : Frames with CRC errors |
| er64_trunc | 0 | top_int : Frames shorter than minimum |
| | 0 | bottom_int : Frames shorter than minimum |
| er64_toolong | 0 | top_int : Frames longer than maximum |
| | 0 | bottom_int : Frames longer than maximum |
| er64_bad_eof | 0 | top_int : Frames with bad end-of-frame |
| | 0 | bottom_int : Frames with bad end-of- |
| frame | | |
| er64_enc_out | 0 | top_int : Encoding error outside of |
| frames | 0 | bottom_int : Encoding error outside of |
| frames | | |
| er64_disc_c3 | 0 | top_int : Class 3 frames discarded |
| | 0 | bottom_int : Class 3 frames discarded |
| er64_pcs_blk | 0 | top_int : PCS block errors |
| | 0 | bottom_int : PCS block errors |
| stat64_rateTxFrame | 0 | Tx frame rate (fr/sec) |
| stat64_rateRxFrame | 0 | Rx frame rate (fr/sec) |
| stat64_rateTxPeakFrame | 0 | Tx peak frame rate (fr/sec) |
| stat64_rateRxPeakFrame | 0 | Rx peak frame rate (fr/sec) |
| stat64_rateTxWord | 0 | Tx Word rate (words/sec) |
| stat64_rateRxWord | 0 | Rx Word rate (words/sec) |
| stat64_rateTxPeakWord | 0 | Tx peak Word rate (words/sec) |
| stat64_rateRxPeakWord | 0 | Rx peak Word rate (words/sec) |
| stat64_PRJTFrames | 0 | top_int : Number of PRJT frames |
| returned to this port | 0 | bottom_int : Number of PRJT |
| frames returned to this port | | |

```

stat64_PBSYFrames      0          top_int : Number of PBSY frames
returned to this port
                                0          bottom_int : Number of PBSY
frames returned to this port
stat64_inputBuffersFull 0          top_int : Number of occurrences
when all input buffers full
                                0          bottom_int : Number of
occurrences when all input buffers full
stat64_rxClass1Frames  0          top_int : Number of class 1
frames received
                                0          bottom_int : Number of class 1
frames received
stat64_aveTxFrameSize  0          Average Tx Frame size
stat64_aveRxFrameSize  0          Average Rx Frame size
Lr_in                   0          top_int
                                0          bottom_int
Ols_in                  0          top_int
                                0          bottom_int
Lr_out                   0          top_int
                                0          bottom_int
Ols_out                  0          top_int
                                0          bottom_int
Link_failure             0          top_int
                                0          bottom_int
Invalid_CRC              0          top_int
                                0          bottom_int
Invalid_word             0          top_int
                                0          bottom_int
Protocol_err            0          top_int
                                0          bottom_int
Loss_of_sig              0          top_int
                                0          bottom_int
Loss_of_sync            0          top_int
                                0          bottom_int
er_bad_os                0          top_int : Invalid ordered set
                                0          bottom_int: Invalid ordered set

```

```

portrouteshow 53
port address ID: 0x013500
external unicast routing table:
  0: Embedded
 255: Embedded
internal unicast routing table:
  0: Embedded

```

```
portcamshow 53
```

```

-----
Port  SID used  DID used  SID entries  DID entries
53    0          0        000000     000000
-----

```

```

ptbufshow, ptcreditshow, ptdatashow, ptstatsshow 53
S:

```

```

S:VF Enable:          1
S:
S:C4 Global Variable:
S:-----
-----
S:trace_stop:        0
S:
S:C4 Phy Data Pointers: c4_phyp = 0xb6ad2080
S:-----
-----
S:tnodep              0xbb83c540      pt
      0x4302800f
S:proto_phyp          0xb8808c60      phy_cfg
0xb6ad30c0
S:c4_chp              0x97e28000      c4_lgcp
0x97f84000
S:c4_phy_regp         0x81c78000      proc_dir
0xb8518640
S:-----
-----
S:magic_id            0xc4345678      num_port_timer      12
S:prev_if_id         0x4302000f      S:ftx                0
      tov              0
S:initialized         0          port_idx              15
S:ui_idx              53          slot_no
      0
S:blade_idx           15          sw_usr_ports          400
S:unused              0          intr_debounced
      0
S:aec_status          0x0          reason_code
      0
S:debug               0x00000004      debug_trc_line        0
S:rxbuf_list_head    0xffffffff      rxbuf_list_tail
0xffffffff
S:isAePort            0          port_misc_data
      0
S:num_fault1_rx_disc  0          num_fault2_rx_disc    0
S:p_llli_cause0       0          p_sig_regained        0
S:p_sync_regained     0          enc_out
      0x0
S:cached_fps_status   0          cached_sts_status     0
S:cached_er_crc_good_eof 0
S:cached_er_bad_os    0          cached_er_too_long    0
S:cached_er_trunc     0
cached_tot_er_crc_good_eof 0
S:num_pt_excess_intr  0          num_no_fid            0
S:num_fault1_cnt      0          num_fault2_cnt
      0
S:num_fault_lip       0          num_fault_llli        0
S:num_fault_rx_fifo   0          num_fault_hss         0
S:num_fault_bwait     0          lli_intr_prim
      0
S:num_sw_link_to      0
be_link_err_mon_count 0

```



```

S:ecb_enc_enabled          0          ecb_comp_enabled
      0
S:ecb_rsv_enc              0          ecb_rsv_comp          0
S:ecb_enc_bm              0x0        ecb_key_index
0xffffffff
S:fab_idx                  4
S:num_be_lto              0          lto_count_reset_intvl
      0
S:lr_count_reset_intvl    0          num_be_lr
      0
S:num_fault_qsf           0          check_lto
      0
S:credit_loaded           0          num_credit_overrun
      0
S:fec_enabled             0x0        fec_los_to_flag        0x0
S:phy_stats_clear_ts      1725611419  pcs_err_online
      0
S:pcs_err_light_det       0          pcs_err_ignore
      0
S:pcs_blk_err             0          pcs_hiber              0
S:phy_port_status         0          ecb_enc_lr_count
      0
S:dport_mode              0          avoid_lto_det          0
S:sn_debounced           0x0        sn_started_kr_reqd     0
S:major_timer_started     0x0        ready_bm               0x0
S:parln_1_bm              0x0        parln_0_bm             0x0
S:be_los_of_sync_event_intvl
be_los_of_sync_event      0
S:errataPtenable_cntr    0          errataPoll_cntr
      0
S:jda_rx_sig_loss_det     0          jda_rx_sig_loss_cnt
      0
S:encrypt_blk_error       0
S:
S:      c4_trunk
S:=====
S:mark_ts                  0x0          deskew                  0x0
S:master_phyp              0x0
S:
S:adelay[00]: 0x00000000 0x00000000 0x00000000 0x00000000
S:adelay[04]: 0x00000000 0x00000000 0x00000000 0x00000000
S:
S:      c4_buf
S:=====
S:tx_csc                    0          rx_csc
      0
S:ld_vc_credits            0          tx_flag                 0x0
S:alloc_buffers            0          req_buffers             0
S:est_buffers              20         ld_use_est              0
S:bb_sc_n                  0          rx_bb_sc_n
      0
S:data_cr                   5          nondata_cr
      6
S:cr_enable                 0

```

```

S:ld_nondata_cr          6          tnodep
0xbb83c620
S:tx_credits[0] 0      0      0      0      0      0      0      0
S:tx_credits[8] 0      0      0      0      0      0      0      0
S:tx_credits[16]      0      0      0      0      0      0      0      0      0
S:tx_credits[24]      0      0      0      0      0      0      0      0      0
S:tx_credits[32]      0      0      0      0      0      0      0      0      0
S:rx_credits[0] 0      0      0      0      0      0      0      0
S:rx_credits[8] 0      0      0      0      0      0      0      0
S:rx_credits[16]      0      0      0      0      0      0      0      0      0
S:rx_credits[24]      0      0      0      0      0      0      0      0      0
S:rx_credits[32]      0      0      0      0      0      0      0      0      0
S:tx_mbc[0]      0      0      0      0      0      0      0      0
S:tx_mbc[8]      0      0      0      0      0      0      0      0
S:tx_mbc[16]     0      0      0      0      0      0      0      0
S:tx_mbc[24]     0      0      0      0      0      0      0      0
S:tx_mbc[32]     0      0      0      0      0      0      0      0
S:rx_mbc[0]      0      0      0      0      0      0      0      0
S:rx_mbc[8]      0      0      0      0      0      0      0      0
S:rx_mbc[16]     0      0      0      0      0      0      0      0
S:rx_mbc[24]     0      0      0      0      0      0      0      0
S:rx_mbc[32]     0      0      0      0      0      0      0      0

```

S:

S:C4 Chip Variables: c4_phyp->c4_chp = 0x97e28000

S:-----

S:version = 2.1

S:magic_id 0xc4234567 init_state 0x8

S:reset_reg_mem 0x1

S:ch_int0_en_bm 0x0 intr0_cause 0x0

S:ch_int1_en_bm 0x0 intr1_cause 0x0

S:ch_int2_en_bm 0x0 intr2_cause 0x0

S:ch 0x43010080 ch_cfg

0xb7013ba0

S:raslog_hdl.hndl 0x0 obj_halted 0x0

S:c4_chip_regp 0x80000000 c4_fpg_regp

0x81800000

S:num_chip_timer 0x5

S:hi_task_bm 0x0 lo_task_bm 0x0

S:c4_deferq.q_head 0x0 c4_deferq.q_tail 0x0

S:c4_tmrq.q_head 0x0 c4_tmrq.q_tail 0x0

slot_no 0

S:chip_inst 0 chip_idx 0

S:pll_initialized 1

pll_serdes_initialized 1

S:init_tries 0 init_ptEnableBM

0xba01b488

S:tick_polling 0xb980c9c0 sec_polling

0xb980c960

S:bb_fid 129

S:ecb_key_bm[0] 0x0 ecb_key_bm[1] 0x0

S:ecb_key_bm[2] 0x0 ecb_key_bm[3] 0x0

S:is_chip_enc_enabled 0

is_chip_comp_enabled 0x0

```

S:ftb_rsrcp->ftb_flags 0x0          act_rsrcp->act_flag 0x1
S:lue_rsrcp->lue_flags[0]          0x0          lue_rsrcp-
>lue_flags[1] 0x0
S:c4_phyp[00]: 0xb6ab0000 0xb6ab2080 0xb6ab4100 0xb6ab6180
S:c4_phyp[04]: 0xb6ab9040 0xb6abb0c0 0xb6abd140 0xb6ac0000
S:c4_phyp[08]: 0xb6ac2080 0xb6ac4100 0xb6ac6180 0xb6ac9040
S:c4_phyp[12]: 0xb6acbc0c 0xb6acd140 0xb6ad0000 0xb6ad2080
S:c4_phyp[16]: 0xb6ad4100 0xb6ad6180 0xb6ad9040 0xb6adb0c0
S:c4_phyp[20]: 0xb6add140 0xb6ae0000 0xb6ae2080 0xb6ae4100
S:c4_phyp[24]: 0xb6ae6180 0xb6ae9040 0xb6aeb0c0 0xb6aed140
S:c4_phyp[28]: 0xb6af0000 0xb6af2080 0xb6af4100 0xb6af6180
S:c4_phyp[32]: 0xb6af9040 0xb6afb0c0 0xb6afd140 0xb6b00000
S:c4_phyp[36]: 0xb6b02080 0xb6b04100 0xb6b06180 0xb6b09040
S:c4_phyp[40]: 0xb6b0b0c0 0xb6b0d140 0xb6b10000 0xb6b12080
S:c4_phyp[44]: 0xb6b14100 0xb6b16180 0xb6b19040 0xb6b1b0c0
S:c4_phyp[48]: 0xb6b1d140 0xb6b20000 0xb6b22080 0xb6b24100
S:c4_phyp[52]: 0xb6b26180 0xb6b29040 0xb6b2b0c0 0xb6b2d140
S:c4_phyp[56]: 0xb6b30000 0xb6b32080 0xb6b34100 0xb6b36180
S:c4_phyp[60]: 0xb6b39040 0xb6b3b0c0 0xb6b3d140 0xb6b40000
S:c4_lgcp[00]: 0x97f48000 0x97f4c000 0x97f50000 0x97f54000
S:c4_lgcp[04]: 0x97f58000 0x97f5c000 0x97f60000 0x97f64000
S:c4_lgcp[08]: 0x97f68000 0x97f6c000 0x97f70000 0x97f74000
S:c4_lgcp[12]: 0x97f78000 0x97f7c000 0x97f80000 0x97f84000
S:c4_lgcp[16]: 0x97f88000 0x97f8c000 0x97f90000 0x97f94000
S:c4_lgcp[20]: 0x97f98000 0x97f9c000 0x97fa0000 0x97fa4000
S:c4_lgcp[24]: 0x97fa8000 0x97fac000 0x97fb0000 0x97fb4000
S:c4_lgcp[28]: 0x97fb8000 0x97fbc000 0x97fc0000 0x97fc4000
S:c4_lgcp[32]: 0x97fc8000 0x97fcc000 0x97fd0000 0x97fd4000
S:c4_lgcp[36]: 0x97fd8000 0x97fdc000 0x97fe0000 0x97fe4000
S:c4_lgcp[40]: 0x97fe8000 0x97fec000 0x97ff0000 0x97ff4000
S:c4_lgcp[44]: 0x97ff8000 0x97ffc000 0x8e000000 0x8e004000
S:c4_lgcp[48]: 0x8e008000 0x8e00c000 0x8e010000 0x8e014000
S:c4_lgcp[52]: 0x8e018000 0x8e01c000 0x8e020000 0x8e024000
S:c4_lgcp[56]: 0x8e028000 0x8e02c000 0x8e030000 0x8e034000
S:c4_lgcp[60]: 0x8e038000 0x8e03c000 0x8e040000 0x8e044000
S:chip_timers[00]: 0xb980c720 0xb980c780 0xb980c7e0 0xb980c840
S:chip_timers[04]: 0xb980c8a0 0xb980c900
S:disc_trap_enable_required 0x0          rxlp_disc_log_stop
0x0
S:curr_rxlp_frm_cnt 0x0          curr_rxlp_disc_frm_cnt 0x0
S:sw_disc_frm_cnt 0x0          last_disc_frm_cnt 0x0
S:txq_nopop_pr_cnt 0x0          pollErrataDfe_ptBM
0xba01b4b0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][0] 0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][1] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][2] 0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][0] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][1] 0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][2] 0x0
S:
S:C4 Logical Port Variables
S:-----
-----
S:c4_lgc_regp 0x81c78000

```

```

S:c4_phyp:
S:      0xb6ad2080      0x0      0x0      0x0

S:      0x0      0x0      0x0      0x0

S:master_phyp      0xb6ad2080      if_id
0x4302000f
S:min_phyp      0x0      max_phyp      0x0
S:num_phy_ports      1      lgc_num      15
S:num_iu_to      0      sw_txq_bm
      0
S:port_fid      129      unused      0
S:port_group      1      lgc_stats_clear_ts
      1725611419

S:domain_tbl_sel      0      area_tbl_sel
      0
S:egid_tbl_sel      0
S:serv_lo_bm      0x0
S:
S:Proto Phy Variables:
S:-----
-----
S:magic_id      0xc4123456      asic_phyp
0xb6ad2080
S:port_id      0x4302800f      phy_cfg
      0xb6ad30c0
S:upsm_hdl      0xb8014460      physm_hdl
0xb80141e0
S:ov_snsn_hdl      0xb80140a0      sw_snsn_hdl
0xb8014140
S:ov_lksm_hdl      0xb8014280      sw_lksm_hdl
0xb8014320
S:trksm_hdl      0xb80143c0      lr_flag      0x0
S:lr_active      0x0      qsfm_txx_rate_sel
      0x0

S:
S:UPSM      UP00: UPST_PORT_DISABLED      --> UP00: UPST_PORT_DISABLED
S:SNSM(OV)      SN00: OV_SNST_STOPPED      --> SN00: OV_SNST_STOPPED
S:SNSM(SW)      SW00: SW_SNST_STAGE_WS      --> SW00: SW_SNST_STAGE_WS
S:PHYSM      PP00: PHYST_STOPPED      --> PP00: PHYST_STOPPED
S:LKSM(OV)      LK00: OV_LKST_INACTIVE      --> LK00: OV_LKST_INACTIVE
S:LKSM(SW)      SW13: INACTIVE      --> SW13: INACTIVE
S:TRKSM      TRK0: TRKST_INIT      --> TRK0: TRKST_INIT
S:
S:physm variables:
S:-----
-----
S:proto_phyp      0xb8808c60      physm_hdl
0xb80141e0
S:force_offline      0      copper      0
S:fault_reason      0: UNKNOWN
S:phy_media_present      0
S:
S:snsn variables:

```

```

S:-----
-----
S:speed                0xff          proto_phyp
0xb8808c60
S:hw_sn_tries_left    0x0          sw_sn_tries_left      0x0
S:curr_txsp_count     0x0          curr_tx_indx
S:tx_max              0x0
    0x0
S:curr_tx             0x0          curr_rxsp_count
    0x0
S:rx_max              0x0          curr_rx_indx
    0x0
S:curr_rx             0x0          rx_mem
    0x0
S:rxsp_rec_count     0x0
S:nc_start            0x0          tx_start              0x0
S:sync_start          0x0          sync_present          0x0
S:diag_auto           0x0          diag_speed            0xff
S:striped_wd_tov     3000          hw_wd_tov
    3000
S:step                0x0          qsfp28_speed_mode
    0x0
S:qsfp_mode0_hw_sn_tries_left 0x0
S:qsfp_mode1_hw_sn_tries_left 0x0
S:
S:lksm variables:
S:-----
-----
S:proto_phyp          0xb8808c60    ov_lksm_hdl
0xb8014280
sw_lksm_hdl          0xb8014320
num_lf1              0
S:hw_link_tries_left 0          sw_link_tries_left    0
S:buf_ptype          0x0          stored_entry_state     0x6
S:handshake_owner    0x0          mark_unsent
    0x0
S:busybuf_stuck      0x0          lr_wait                0x0
S:
S:trksm variables:
S:-----
-----
S:Not a trunk port
S:
S:upsm variables:
S:-----
-----
S:proto_phyp          0xb8808c60    upsm_hdl
0xb8014460
S:bb_credits          0          port_beacon            0
S:port_diag_flag     0          force_offline
    0
S:port_fault_rsn     0: PORT_NO_FAULT
S:retry_init_rsn     0: UNKNOWN
S:linit_reason        0          linit_result           0

```

```

S:ie_fctl_mode          0          fec_in_sync_tries_left  0
S:retry_sn_fail_init    0
retry_link_fail_init    0
S:excess_lr_count       0
S:
S:c4_ch_cfg
S:-----
-----
S:c4_desc_ring_size     256      292      256      256      292
292      2      292      292
S:thresh_def            0          16          1          0
S:intr_tries            500          cmem_pattern
0xdeadbeef
S:cmem_pattern_upwd     2          cmem_init_time          16
S:cmem_init_tries      5
S:ctrl_par_thresh      2          data_par_thresh
4
S:cam_par_thresh       4          buf_loss_thresh
12
S:crit_par_thresh      2          non_crit_par_thresh
6
S:pci_abort_thresh     10          pci_err_thresh          5
S:excess_chintr_thresh 8          sw_err_thresh           20
S:err_sample_period    300          intr_sleep
20000
S:frame_timeout        2500          proxy_dev          16384
S:vf_route             81920          qos          2048
S:stats 2048          f_redirect          2048
S:rsp_trap             2048          lun_zoning          20480
S:area_mode            0          ftb_max_loop[0]      0
S:ftb_max_loop[1]      6          ftb_max_loop[2]      9
S:ftb_max_loop[3]     10          ftb_max_loop[4]     10
S:ftb_max_loop[5]     5          ftb_max_loop[6]     6
S:ftb_seg_size[0]     0          ftb_seg_size[1]
16384
S:ftb_seg_size[2]     65536          ftb_seg_size[3]
16384
S:ftb_seg_size[4]     16384          ftb_seg_size[5]
65536
S:ftb_seg_size[6]     16384          ftb_seg_base[0]      0
S:ftb_seg_base[1]     0          ftb_seg_base[2]
65536
S:ftb_seg_base[3]     16384          ftb_seg_base[4]
32768
S:ftb_seg_base[5]     131072          ftb_seg_base[6]
49152
asic_err_monitor_period1 300
asic_err_monitor_period2 86400
zone_chk_to_poll_period 25
zone_chk_class2_reject_tov 220
S:
S:c4_phy_cfg
S:-----
-----

```

```

S:version = 2.1
S:pt          0x4302800f      fab_ptr
0x9a800000
S:fabattr          0x9a8000d4      fab_iop
      0x9a800050
S:cfgbm          0xbb83c384      port_ctrl
0xb6ad30d8
S:pcap.pcap_bm    0x8d215547      pcap.pcap2_bm
0x2588289
S:pcap.pcap3_bm    0x1bebe0c
ui_idx          53      S:slot_no
      0
is_icl          0      S:sw_usr_ports      400
S:neg_speed      0 0 0 0 0 0
S:my_domain      0x1      port_mode      0x0
S:hw_sn_maxtries      100      sw_sn_maxtries
      0
S:hw_link_maxtries      10      sw_link_maxtries      5
S:rx_cyc_tov      28      rttov      300
S:bufrdy_tov      300      busybuf_tov      286
S:mark_tov      300      lksm_tov      3000
S:buf_dealloc_wait      4      hw_wd_tov      3000
S:hw_lk_train_tov      540      hw_lk_test_tov
      150
S:syswait_tx_12_lips      1      lip_rx_tov      55
S:al_time_tov      15      lp_tov      2000
S:intr_tries_port      500      intr_mod_debounce
      250
S:intr_lsrflt_debounce      500      intr_efifo_debounce      100
S:port_no_fid      3      excess_ptintr_thresh      8
S:port_fault1_thresh      100      port_fault1_spur_thresh      250
S:port_fault1_disc_thresh      500
port_fault1_disc_spur_thresh      1000
S:port_fault2_thresh      5      losync_tov      100
S:port_sw_link_to      15      en_8g_scramble
      1
frc_hw_sn_mode      0x1
S:enc_poll_thresh      0      fec_enable
      0
S:fec_in_sync_to      50      fec_in_sync_try_max
      4
S:port_be_lto_threshold      100      port_be_lr_threshold
      2
S:be_cr_in_sync_to      5
port_credit_overrun_thresh      10
S:jda_sfp_losig_tov      400
jda_sfp_losig_try_max      30
S:striped_wd_tov      3000
no_sync_debounce      1200
S:
S:      fab_iop
S:=====
S:fab_iop->interop_mode      0x0      fab_iop->lab_mode      0x0
S:fab_iop->fl_bbc      0x0      fab_iop->fl_fan

```

```

    0x0
S:fab_iop->fl_cls          0x4          fab_iop->fl_rscn
    0x0
S:fab_iop->domain_id_offset 0x60          fab_iop-
>mcdt_fabric_mode      0x0
S:fab_iop->mcdt_default_zone 0x0          fab_iop-
>mcdt_safe_zone        0x0
S:
S:      port_ctrl
S:=====
S:port_ctrl.port_type    1          port_ctrl.port_grp    1
S:port_ctrl.port_number 53          port_ctrl.vc_mode      1
S:
S:      port_ctrl.lcap
S:=====
S:has_serdes            0          has_media              1
S:topology              1          skip_nego              0
S:skip_pnego            0          skip_init_event       0
S:en_shim                0          speed_neg              0
    1
S:loop_back             0          num_speeds            5
S:fec_enable            0
S:
S:      port_ctrl.speed_list array
S:=====
S:speed_list[0].auto_neg 1          speed_list[0].lnk_speed 0x0000000a
S:speed_list[1].auto_neg 1          speed_list[1].lnk_speed 0x00000008
S:speed_list[2].auto_neg 1          speed_list[2].lnk_speed 0x00000006
S:speed_list[3].auto_neg 1          speed_list[3].lnk_speed 0x00000005
S:speed_list[4].auto_neg 1          speed_list[4].lnk_speed 0x00000003
S:speed_list[5].auto_neg 0          speed_list[5].lnk_speed 0x00000000
S:
S:      port_ctrl.cm
S:=====
S:port_ctrl.cm.num_vcs      8
S:port_ctrl.cm.min_bufs    8
S:port_ctrl.cm.cr_shar_bufs 0
S:port_ctrl.vc_alloc
S:port_ctrl.vc_alloc        2 0 1 1 1 1 1 1
S:port_ctrl.vc_alloc        0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.norm_vc_alloc
S:port_ctrl.norm_vc_alloc   4 0 5 5 5 5 1 1
S:port_ctrl.norm_vc_alloc   0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.cm.skip_bb_credit 0
S:port_ctrl.cm.use_shim_based_sublist 0
S:
S:      port_ctrl.serdes_set
S:=====
S:serdes_type              0x8
S:serdes_data_t.ibm_hss_serdes.tx_drive_power 0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b_sign 0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b 0x0

```



```

S:serdes_data_t.ibm_hss_serdes.pre_emphasis_a      0x0
S:serdes_data_t.ibm_hss_serdes.rxeq              0x0
S:
S:      cfgbm
S:=====
S:old_distance      0x0          gport_lockdown      0x0
S:tport            0x1          speed                  0x0
S:disable_eport    0x0          fcacc                 0x0
S:lport_lockdown   0x0          0x0                  priv_lport_lockdown
0x0
S:vcxlt_linit      0x0          delay_flogi          0x0
S:isl_interop      0x0          distance              0x0
S:BufStarvFlag     0x0          credit_sharing       0x0
S:lport_halfduplex 0x0          lport_fairness       0x0
S:soft_neg         0x0          asn_frc_hwretry      0x0
S:cr_recov         0x0          fport_buffers        0x0
S:export           0x0          0x0                  export_mode
0x0
S:csctl_en         0x0          mirror_port          0x0
S:fault_delay      0x0          non_dfe              0x0
S:fec_configured*(0=ENAB) 0          0                    fec_tts
0
S:port_persistently_disabled (permanently) 0 (0)
S:
S:      cfg property
S:=====
S:priv_pcfg_bm      0x00000000    lgcl_pcfg_bm
0xbb83c3c4
S:fport_buffer      0x00000000
S:
S:
S:C4 Discard Cntrs: rxlp_stats = 0xb6ad2430
S:-----
-----
S:disc_mcast_wka    0x0          disc_inv_did         0x0
S:disc_cl1_cl4     0x0          disc_sid_chk_fail    0x0
S:disc_inv_dom_egid_txpt 0x0          disc_vft_hop_cnt_1
0x0
S:disc_classf       0x0          disc_fcp_cdb_inv     0x0
S:disc_vfid_trap_enabled 0x0          0x0
disc_vfid_hdr_chk_fail 0x0
S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err 0x0
S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err 0x0
S:disc_ftb_vm_mode  0x0          disc_ftb_agn_t2_miss 0x0
S:disc_ecb_de_pad_err 0x0          disc_ecb_de_tag_err   0x0
S:disc_ecb_de_seq_err 0x0          disc_ecb_err          0x0
S:disc_ftb_type4_match 0x0          disc_fcp_rsp_ftb_type4 0x0
S:disc_fcp_rsp_ftb_type4 0x0          disc_ftb_type5_match
0x0
S:disc_ftb_type3_match 0x0          disc_els_ftb_type3   0x0
S:disc_ftb_type1_match 0x0          disc_els_rsp_ex_port 0x0
S:disc_inv_drp_dps  0x0          disc_did_lookup_miss 0x0
S:disc_ftb_type2_match 0x0          disc_trpd_plogi_pdisc 0x0
S:disc_type2_lookup_miss 0x0          disc_ftb_type6_match

```

```

0x0
S:disc_els_rep_ex_port 0x0          disc_els_sid_lkup_bit1 0x0
S:disc_els_sid_lkup_bit0          0x0
disc_bls_frm_trap_bit1 0x0
S:disc_ftb_token_err 0x0          disc_asic_internal_err 0x0
S:disc_hard_zone_miss 0x0        disc_lun_zone_miss 0x0
S:disc_flt_frame_disc 0x0        disc_flt_parity_err 0x0
S:disc_frame_marked_du 0x0       disc_frame_marked_to 0x0
E:Connection type: FE
E:Port type: E_port
E:Trunk port: No
E:Configured Speed: AUTO_SPEED_NEGO
E:Max Capable Speed: 32G
E:Current SNSM Speed: UNDEFINED
E:Hardware TX Speed: 32G (0x00000004)
E:Hardware RX Speed: 32G (0x00000040)
E:
E:Interrupts: 0          Link_failure: 0
Loss_of_sync: 0          Loss_of_sig: 0
E:Lli: 0                 Invalid_word: 0
E:trapped_frm: 0         fwd_status_ok: 0
E:fwd_timeout: 0         fwd_tx_unavail: 0
E:fwd_unroutable: 0      fwd_zone_out: 0
E:fwd_other_err: 0       frm_err_discard: 0
E:Fltr listA: 0          Fltr listB: 0
E:Zone trap fwd: 0       Zone trap disc: 0
E:shim_csum: 0           RTE_perr: 0
E:Invalid_crc: 0         Delim_err: 0
E:Protocol_err: 0
E:Lr_in: 0               Lr_out: 0
E:Ols_in: 0              Ols_out: 0

```

filterportshow 53

FILTER DATA

```

Shadow settings:
Filter Enable: 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000

```

Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass: 0x00000000

Real settings:

Enable RAM: 0x00000000, 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass RAM: 0x00000000

Shadowed filters:

Filter 0: Not Installed (MIRROR1)(LISTA)
c4_fldenable[0] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[0] = 0x00000000,c4_fltr_config[0] = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
c4_fldenable[1] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[1] = 0x00000000,c4_fltr_config[1] = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
c4_fldenable[2] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[2] = 0x00000000,c4_fltr_config[2] = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
c4_fldenable[3] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[3] = 0x00000000,c4_fltr_config[3] = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
c4_fldenable[4] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[4] = 0x00000000,c4_fltr_config[4] = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
c4_fldenable[5] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[5] = 0x00000000,c4_fltr_config[5] = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
c4_fldenable[6] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[6] = 0x00000000,c4_fltr_config[6] = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
c4_fldenable[7] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[7] = 0x00000000,c4_fltr_config[7] = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
c4_fldenable[8] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[8] = 0x00000000,c4_fltr_config[8] = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
c4_fldenable[9] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[9] = 0x00000000,c4_fltr_config[9] = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
c4_fldenable[10] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[10] = 0x00000000,c4_fltr_config[10] =
0x00000000
Filter 11: Not Installed (SIM)(LISTA)
c4_fldenable[11] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[11] = 0x00000000,c4_fltr_config[11] =
0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
c4_fldenable[12] = 0x00000000 0x00000000 0x00000000

```
0x00000000
    c4_fldnegate[12] = 0x00000000,c4_fltr_config[12] =
0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
    c4_fldenable[13] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[13] = 0x00000000,c4_fltr_config[13] =
0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
    c4_fldenable[14] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[14] = 0x00000000,c4_fltr_config[14] =
0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
    c4_fldenable[15] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[15] = 0x00000000,c4_fltr_config[15] =
0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
    c4_fldenable[16] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[16] = 0x00000000,c4_fltr_config[16] =
0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
    c4_fldenable[17] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[17] = 0x00000000,c4_fltr_config[17] =
0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
    c4_fldenable[18] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[18] = 0x00000000,c4_fltr_config[18] =
0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
    c4_fldenable[19] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[19] = 0x00000000,c4_fltr_config[19] =
0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
    c4_fldenable[20] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[20] = 0x00000000,c4_fltr_config[20] =
0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
    c4_fldenable[21] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[21] = 0x00000000,c4_fltr_config[21] =
0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
    c4_fldenable[22] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[22] = 0x00000000,c4_fltr_config[22] =
0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
```

```
    c4_fldenable[23] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[23] = 0x00000000,c4_fltr_config[23] =
0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
    c4_fldenable[24] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[24] = 0x00000000,c4_fltr_config[24] =
0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
    c4_fldenable[25] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[25] = 0x00000000,c4_fltr_config[25] =
0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
    c4_fldenable[26] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[26] = 0x00000000,c4_fltr_config[26] =
0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
    c4_fldenable[27] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[27] = 0x00000000,c4_fltr_config[27] =
0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
    c4_fldenable[28] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[28] = 0x00000000,c4_fltr_config[28] =
0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
    c4_fldenable[29] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[29] = 0x00000000,c4_fltr_config[29] =
0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    c4_fldenable[30] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[30] = 0x00000000,c4_fltr_config[30] =
0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    c4_fldenable[31] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[31] = 0x00000000,c4_fltr_config[31] =
0x00000000
```

Real filters:

```
Filter 0: Not Installed (MIRROR1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
```

0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 11: Not Installed (SIM)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 15: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 16: Not Installed (PERF1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 17: Not Installed (PERF2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 18: Not Installed (PERF3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 19: Not Installed (PERF4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 20: Not Installed (PERF5)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 21: Not Installed (PERF6)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 22: Not Installed (PERF7)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 23: Not Installed (PERF8)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 24: Not Installed (PERF9)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 25: Not Installed (PERF10)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 26: Not Installed (PERF11)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 27: Not Installed (PERF12)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 28: Not Installed (OPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,


```
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter dirty indicator: 0x00000000
Performance filters: 0
Port Mirror filters: 0 (0x0)
```

FIELD DATA

Shadowed fields:

```
fldoffset[0] = 0x00, fldmask[0] = 0x00, fldvalue_dyna[0]: 0x00 0x00
0x00 0x00
fldcontrol[0].inuse = 0x0 fldcontrol[0].refcnt = 0x00 0x00 0x00
0x00
fldoffset[1] = 0x00, fldmask[1] = 0x00, fldvalue_dyna[1]: 0x00 0x00
0x00 0x00
fldcontrol[1].inuse = 0x0 fldcontrol[1].refcnt = 0x00 0x00 0x00
0x00
fldoffset[2] = 0x00, fldmask[2] = 0x00, fldvalue_dyna[2]: 0x00 0x00
0x00 0x00
fldcontrol[2].inuse = 0x0 fldcontrol[2].refcnt = 0x00 0x00 0x00
0x00
fldoffset[3] = 0x00, fldmask[3] = 0x00, fldvalue_dyna[3]: 0x00 0x00
0x00 0x00
fldcontrol[3].inuse = 0x0 fldcontrol[3].refcnt = 0x00 0x00 0x00
0x00
fldoffset[4] = 0x00, fldmask[4] = 0x00, fldvalue_dyna[4]: 0x00 0x00
0x00 0x00
fldcontrol[4].inuse = 0x0 fldcontrol[4].refcnt = 0x00 0x00 0x00
0x00
fldoffset[5] = 0x00, fldmask[5] = 0x00, fldvalue_dyna[5]: 0x00 0x00
0x00 0x00
fldcontrol[5].inuse = 0x0 fldcontrol[5].refcnt = 0x00 0x00 0x00
0x00
fldoffset[6] = 0x00, fldmask[6] = 0x00, fldvalue_dyna[6]: 0x00 0x00
0x00 0x00
fldcontrol[6].inuse = 0x0 fldcontrol[6].refcnt = 0x00 0x00 0x00
0x00
fldoffset[7] = 0x00, fldmask[7] = 0x00, fldvalue_dyna[7]: 0x00 0x00
```

```
0x00 0x00
fldcontrol[7].inuse = 0x0  fldcontrol[7].refcnt = 0x00 0x00 0x00
0x00
fldoffset[8] = 0x00, fldmask[8] = 0x00, fldvalue_dyna[8]:0x00 0x00
0x00 0x00
fldcontrol[8].inuse = 0x0  fldcontrol[8].refcnt = 0x00 0x00 0x00
0x00
fldoffset[9] = 0x00, fldmask[9] = 0x00, fldvalue_dyna[9]:0x00 0x00
0x00 0x00
fldcontrol[9].inuse = 0x0  fldcontrol[9].refcnt = 0x00 0x00 0x00
0x00
fldoffset[10] = 0x00, fldmask[10] = 0x00, fldvalue_dyna[10]:0x00 0x00
0x00 0x00
fldcontrol[10].inuse = 0x0  fldcontrol[10].refcnt = 0x00 0x00 0x00
0x00
fldoffset[11] = 0x00, fldmask[11] = 0x00, fldvalue_dyna[11]:0x00 0x00
0x00 0x00
fldcontrol[11].inuse = 0x0  fldcontrol[11].refcnt = 0x00 0x00 0x00
0x00
fldoffset[12] = 0x00, fldmask[12] = 0x00, fldvalue_dyna[12]:0x00 0x00
0x00 0x00
fldcontrol[12].inuse = 0x0  fldcontrol[12].refcnt = 0x00 0x00 0x00
0x00
fldoffset[13] = 0x00, fldmask[13] = 0x00, fldvalue_dyna[13]:0x00 0x00
0x00 0x00
fldcontrol[13].inuse = 0x0  fldcontrol[13].refcnt = 0x00 0x00 0x00
0x00
fldoffset[14] = 0x00, fldmask[14] = 0x00, fldvalue_dyna[14]:0x00 0x00
0x00 0x00
fldcontrol[14].inuse = 0x0  fldcontrol[14].refcnt = 0x00 0x00 0x00
0x00
fldoffset[15] = 0x00, fldmask[15] = 0x00, fldvalue_dyna[15]:0x00 0x00
0x00 0x00
fldcontrol[15].inuse = 0x0  fldcontrol[15].refcnt = 0x00 0x00 0x00
0x00
fldoffset[16] = 0x00, fldmask[16] = 0x00, fldvalue_dyna[16]:0x00 0x00
0x00 0x00
fldcontrol[16].inuse = 0x0  fldcontrol[16].refcnt = 0x00 0x00 0x00
0x00
fldoffset[17] = 0x00, fldmask[17] = 0x00, fldvalue_dyna[17]:0x00 0x00
0x00 0x00
fldcontrol[17].inuse = 0x0  fldcontrol[17].refcnt = 0x00 0x00 0x00
0x00
fldoffset[18] = 0x00, fldmask[18] = 0x00, fldvalue_dyna[18]:0x00 0x00
0x00 0x00
fldcontrol[18].inuse = 0x0  fldcontrol[18].refcnt = 0x00 0x00 0x00
0x00
fldoffset[19] = 0x00, fldmask[19] = 0x00, fldvalue_dyna[19]:0x00 0x00
0x00 0x00
fldcontrol[19].inuse = 0x0  fldcontrol[19].refcnt = 0x00 0x00 0x00
0x00
```

Real fields:

fldoffset RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000
fldmask RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000
fld value4 RAM:
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
Field dirty indicator: 0x00000000

FDB reference count fdb: 0 [0 0 0 0]
FDB reference count fdb: 1 [0 0 0 0]
FDB reference count fdb: 2 [0 0 0 0]
FDB reference count fdb: 3 [0 0 0 0]
FDB reference count fdb: 4 [0 0 0 0]
FDB reference count fdb: 5 [0 0 0 0]
FDB reference count fdb: 6 [0 0 0 0]
FDB reference count fdb: 7 [0 0 0 0]
FDB reference count fdb: 8 [0 0 0 0]
FDB reference count fdb: 9 [0 0 0 0]
FDB reference count fdb: 10 [0 0 0 0]
FDB reference count fdb: 11 [0 0 0 0]
FDB reference count fdb: 12 [0 0 0 0]
FDB reference count fdb: 13 [0 0 0 0]
FDB reference count fdb: 14 [0 0 0 0]
FDB reference count fdb: 15 [0 0 0 0]
FDB reference count fdb: 16 [0 0 0 0]
FDB reference count fdb: 17 [0 0 0 0]
FDB reference count fdb: 18 [0 0 0 0]
FDB reference count fdb: 19 [0 0 0 0]

Filter counters:
Filter counter 0: 0 (MIRROR1)
Filter counter 1: 0 (MIRROR2)
Filter counter 2: 0 (MIRROR3)
Filter counter 3: 0 (MIRROR4)
Filter counter 4: 0 (AEPORT_NON_MIRR_DROP)

Filter counter 5: 0 (ZONING TRAP)
Filter counter 6: 0 (FCR_EXPORT_DC)
Filter counter 7: 0 (TIN TRAP)
Filter counter 8: 0 (FICON CUP)
Filter counter 9: 0 (FICON CUP DST)
Filter counter 10: 0 (WELL KNOWN ADDR)
Filter counter 11: 0 (SIM)
Filter counter 12: 0 (UNUSED)
Filter counter 13: 0 (UNUSED)
Filter counter 14: 0 (UNUSED)
Filter counter 15: 0 (UNUSED)
Filter counter 16: 0 (PERF1)
Filter counter 17: 0 (PERF2)
Filter counter 18: 0 (PERF3)
Filter counter 19: 0 (PERF4)
Filter counter 20: 0 (PERF5)
Filter counter 21: 0 (PERF6)
Filter counter 22: 0 (PERF7)
Filter counter 23: 0 (PERF8)
Filter counter 24: 0 (PERF9)
Filter counter 25: 0 (PERF10)
Filter counter 26: 0 (PERF11)
Filter counter 27: 0 (PERF12)
Filter counter 28: 0 (OPM1)
Filter counter 29: 0 (OPM2)
Filter counter 30: 0 (IPM1)
Filter counter 31: 0 (IPM2)

ACL DATA

Logical port 15: Hard Zoning disabled, Soft Zoning disabled
Zone type: WWN Zoning
Frames with hard zone miss: 0

*** Please use filterportshow on user port 56 to display ACL hash tables and Mirroring resources of thischip.

***We show this data only for the first physical port which is an external port.

portFcPortCmdShow --slot 0 54 3
doing portFcPortCmdShow: arg1 = 3, arg2 = -2

portshow 54
portDisableReason: None
portCFlags: 0x0
portFlags: 0x4021 PRESENT U_PORT DISABLED LED
LocalSwcFlags: 0x0
portType: 26.0
POD Port: Need license to enable the port
portState: 2 Offline
Protocol: FC
portPhys: 2 No_Module portScn: 2 Offline
port generation number: 0
state transition count: 0

portId: 013600
portIfId: 4302000d
portWwn: 20:36:d8:1f:cc:2c:99:90
portWwn of device(s) connected:
16b Area list:
Distance: normal
portSpeed: N32Gbps

FEC: Inactive
Credit Recovery: Inactive
LE domain: 0
Peer beacon: Off
FC Fastwrite: OFF

| | | | | |
|-------------|---|---------------|---|-------|
| Interrupts: | 0 | Link_failure: | 0 | Frjt: |
| 0 | | | | |
| Unknown: | 0 | Loss_of_sync: | 0 | Fbsy: |
| 0 | | | | |
| Lli: | 0 | Loss_of_sig: | 0 | |
| Proc_rqrd: | 0 | Protocol_err: | 0 | |
| Timed_out: | 0 | Invalid_word: | 0 | |
| Tx_unavail: | 0 | Invalid_crc: | 0 | |
| Delim_err: | 0 | Address_err: | 0 | |
| Lr_in: | 0 | Ols_in: | 0 | |
| Lr_out: | 0 | Ols_out: | 0 | |

portloginshow 54

| Type | PID | World Wide Name | credit | df_sz | cos |
|-------|-----|-----------------|--------|-------|-----|
| ===== | | | | | |

portloginshow 54 -history

| Type | PID | World Wide Name | logout time |
|-------|-----|-----------------|-------------|
| ===== | | | |

portregshow 54

LED registers

=====

| | | | |
|-------------|---------------|----------|-------------|
| 0x81c6a000: | c4_led_status | 00000000 | 0x81c6a004: |
| | c4_led_ctl | 00000000 | |

FPL registers

=====

| | | | |
|-------------|-------------------|----------|-------------|
| 0x81c68200: | fpl_port_config | 23490000 | |
| 0x81c6820c: | fpl_port_id_ctl | 00000000 | 0x81c68210: |
| | fpl_port_id_addr | 00013600 | |
| 0x81c68214: | fpl_port_speed | 00000004 | 0x81c6821c: |
| | fpl_lli_ctl | 00000903 | |
| 0x81c68228: | fpl_lli_os_ctl | bc95b5b5 | 0x81c6822c: |
| | fpl_lli_send_word | bc95b5b5 | |
| 0x81c68230: | fpl_lli_mark_rx | 00000000 | 0x81c68234: |

```

fpl_lli_rnd_trip_time 00000000
0x81c68238: fpl_lli_ns_status 80070007 0x81c6823c:
fpl_lli_intr_status 80070007
0x81c68244: fpl_lli_def 00000000 0x81c68254:
fpl_lli_intr_enable_clr 00100000
0x81c68258: fpl_err_intr_status 00000000 0x81c68260:
fpl_err_intr_enable_clr 00000000
0x81c68268: fpl_err_first_error 00000000 0x81c6826c:
fpl_speed_neg_ctl 00000000
0x81c68270: fpl_speed_neg_stat 00000000 0x81c68274:
fpl_softasn_ctl 0000000f
0x81c68278: fpl_link_init_ctl 00000000 0x81c6827c:
fpl_link_init_stat 00000000
0x81c68280: fpl_aec_ctl 00051060 0x81c68284:
fpl_aec_ctl2 04009f60
0x81c68288: fpl_pcs_ctl 00000160 0x81c6828c:
fpl_fec_ctl 00000441
0x81c68290: fpl_fec_cor 00000000 0x81c68294:
fpl_fec_uncor 00000000
0x81c68298: fpl_hss_link_ctl 0031f040 0x81c6829c:
fpl_afifo_link_ctl 00000a86
0x81c682a0: fpl_echo_lb_ctl 0000028c 0x81c682a4:
fpl_scratch 00000121
0x81c682a8: fpl_debug 00030005 0x81c682ac:
fpl_misc_debug 00001800
0x00000000: SW_shadow_reg 00000000 0x00000000:
SW_c4_phy->cfgptr 00030000

```

per-fpg (per octet) registers

```

=====
0x8180b82c: fpg_serdes_ctla0 81a37be7 0x8180b830:
fpg_serdes_ctla1 81a37be7
0x8180b834: fpg_serdes_ctlb0 81a1c3c3 0x8180b838:
fpg_serdes_ctlb1 81a1c3c3
0x8180b83c: fpg_serdes_xgmii_1ms 00067c28 0x8180b840:
fpg_serdes_regtimctl 40e47946
0x8180b844: fpg_serdes_asnrsttimctl 00000102

```

HSS PLL registers

```

=====
0x8180b400: 00_hssplla_vco_coarse_cal0 00000000 0x8180b404:
01_hssplla_vco_coarse_cal1 00000014
0x8180b408: 02_hssplla_vco_coarse_cal2 00000000 0x8180b40c:
03_hssplla_vco_coarse_cal3 00000000
0x8180b410: 04_hssplla_vco_coarse_cal4 00000000 0x8180b424:
09_hssplla_power_ctl 00000000
0x8180b428: 0A_hssplla_charge_pump_ctl 00000004 0x8180b438:
0E_hssplla_pll_misc_ctl 00000000
0x8180b43c: 0F_hssplla_pclk_ctl 000000f8 0x8180b440:
10_hssplla_eyem_intv_ctl 00000000
0x8180b444: 11_hssplla_eyem_intv_lim1 00000000 0x8180b448:
12_hssplla_eyem_intv_lim2 00000000
0x8180b44c: 13_hssplla_eyem_intv_lim3 00000000 0x8180b450:
14_hssplla_eyem_intv_lim4 00000000

```

| | | | |
|-------------|----------------------------|----------|-------------|
| 0x8180b4f0: | 3C_hssplla_macro_tst_ctl4 | 00000000 | 0x8180b4f4: |
| | 3D_hssplla_macro_tst_ctl3 | 00000000 | |
| 0x8180b4f8: | 3E_hssplla_macro_tst_ctl2 | 00000000 | 0x8180b4fc: |
| | 3F_hssplla_macro_tst_ctl1 | 00000000 | |
| 0x8180b500: | 00_hsspllb_vco_coarse_cal0 | 0000000a | 0x8180b504: |
| | 01_hsspllb_vco_coarse_cal1 | 00000014 | |
| 0x8180b508: | 02_hsspllb_vco_coarse_cal2 | 00000000 | 0x8180b50c: |
| | 03_hsspllb_vco_coarse_cal3 | 00000000 | |
| 0x8180b510: | 04_hsspllb_vco_coarse_cal4 | 00000000 | 0x8180b524: |
| | 09_hsspllb_power_ctl | 00000000 | |
| 0x8180b528: | 0A_hsspllb_charge_pump_ctl | 00000004 | 0x8180b538: |
| | 0E_hsspllb_pll_misc_ctl | 00000000 | |
| 0x8180b53c: | 0F_hsspllb_pclk_ctl | 000000f8 | 0x8180b540: |
| | 10_hsspllb_eyem_intv_ctl | 00000000 | |
| 0x8180b544: | 11_hsspllb_eyem_intv_lim1 | 00000000 | 0x8180b548: |
| | 12_hsspllb_eyem_intv_lim2 | 00000000 | |
| 0x8180b54c: | 13_hsspllb_eyem_intv_lim3 | 00000000 | 0x8180b550: |
| | 14_hsspllb_eyem_intv_lim4 | 00000000 | |
| 0x8180b5f0: | 3C_hsspllb_macro_tst_ctl4 | 00000000 | 0x8180b5f4: |
| | 3D_hsspllb_macro_tst_ctl3 | 00000000 | |
| 0x8180b5f8: | 3E_hsspllb_macro_tst_ctl2 | 00000000 | 0x8180b5fc: |
| | 3F_hsspllb_macro_tst_ctl1 | 00000000 | |

HSS TX registers

=====

| | | | |
|-------------|----------------------------|----------|-------------|
| 0x8180a100: | 00_hsstx_cfg_mode_PHY | 00009f48 | 0x8180a104: |
| | 01_hsstx_test_ctl | 00000000 | |
| 0x8180a108: | 02_hsstx_coeff_ctl_INV | 00000000 | 0x8180a10c: |
| | 03_hsstx_drv_mode_ctl | 00000000 | |
| 0x8180a110: | 04_hsstx_drv_ovrd_ctl | 00000010 | 0x8180a114: |
| | 05_hsstx_dclk_align_ovrd | 00000080 | |
| 0x8180a118: | 06_hsstx_imp_cal_ovrd | 00000c0c | 0x8180a11c: |
| | 07_hsstx_dclk_drift_tol | 00000004 | |
| 0x8180a120: | 08_hsstx_tap0_coeff_TUNE | 00000000 | 0x8180a124: |
| | 09_hsstx_tap1_coeff_TUNE | 00000003 | |
| 0x8180a128: | 0A_hsstx_tap2_coeff_TUNE | 00000018 | 0x8180a12c: |
| | 0B_hsstx_tap3_coeff_TUNE | 0000000d | |
| 0x8180a134: | 0D_hsstx_pol_INV | 00000004 | 0x8180a138: |
| | 0E_hsstx_ae_cmd | 00000000 | |
| 0x8180a13c: | 0F_hsstx_ae_stat | 00000000 | 0x8180a140: |
| | 10_hsstx_ae_tap0_TUNE | 00000000 | |
| 0x8180a144: | 11_hsstx_ae_tap1_TUNE | 00000000 | 0x8180a148: |
| | 12_hsstx_ae_tap2_TUNE | 00000028 | |
| 0x8180a14c: | 13_hsstx_ae_tap3_TUNE | 00000000 | 0x8180a154: |
| | 15_hsstx_app_tune | 0000120e | |
| 0x8180a158: | 16_hsstx_analog_diag | 00000000 | 0x8180a160: |
| | 18_hsstx_4x_seg_app | 0000aafa | |
| 0x8180a164: | 19_hsstx_2x_seg_app | 00000000 | 0x8180a168: |
| | 1A_hsstx_1x_seg_app | 0000ff5d | |
| 0x8180a16c: | 1B_hsstx_seg_4x_term_app | 00000000 | 0x8180a170: |
| | 1C_hsstx_seg_2x1x_term_app | 00000f00 | |
| 0x8180a174: | 1D_hsstx_tap_sign_app | 00000004 | 0x8180a178: |
| | 1E_hsstx_ext_addr_data | 00000001 | |
| 0x8180a17c: | 1F_hsstx_ext_addr_addr | 00000000 | 0x8180a180: |

| | | | |
|---|----------|-------------|--|
| 20_hsstx_pat_buf_bytes_1_0 | 00000000 | | |
| 0x8180a184: 21_hsstx_pat_buf_bytes_3_2 | 00000000 | 0x8180a188: | |
| 22_hsstx_pat_buf_bytes_5_4 | 00000000 | | |
| 0x8180a18c: 23_hsstx_pat_buf_bytes_7_6 | 00000000 | 0x8180a19c: | |
| 27_hsstx_8023az_ctl | 00000000 | | |
| 0x8180a1a0: 28_hsstx_dcc_ctl | 000060c0 | 0x8180a1a4: | |
| 29_hsstx_dcc_ovrd | 00000000 | | |
| 0x8180a1a8: 2A_hsstx_dcc_app | 00000000 | 0x8180a1ac: | |
| 2B_hsstx_dcc_timeout | 0000ffff | | |
| 0x8180a1c0: 30_hsstx_tap_sign_ovrd | 00000000 | 0x8180a1c8: | |
| 32_hsstx_seg_4x_ovrd | 00000000 | | |
| 0x8180a1cc: 33_hsstx_seg_2x_ovrd | 00000000 | 0x8180a1d0: | |
| 34_hsstx_seg_1x_ovrd | 00000000 | | |
| 0x8180a1d8: 36_hsstx_tap_seg_4x_term_ovrd | 00000000 | 0x8180a1dc: | |
| 37_hsstx_tap_seg_2x_term_ovrd | 00000000 | | |
| 0x8180a1e0: 38_hsstx_tap_seg_1x_term_ovrd | 00000000 | 0x8180a1ec: | |
| 3B_hsstx_mac_test_ctl5 | 00000000 | | |
| 0x8180a1f0: 3C_hsstx_mac_test_ctl4 | 00000000 | 0x8180a1f4: | |
| 3D_hsstx_mac_test_ctl3 | 00000000 | | |
| 0x8180a1f8: 3E_hsstx_mac_test_ctl2 | 00000000 | 0x8180a1fc: | |
| 3F_hsstx_mac_test_ctl1 | 000000c6 | | |

HSS RX registers

=====

| | | | |
|---|----------|-------------|--|
| 0x8180a300: 00_hssrx_cfg_mode_PHY | 00009e78 | 0x8180a304: | |
| 01_hssrx_test_ctl | 00000000 | | |
| 0x8180a308: 02_hssrx_phs_rot_ctl | 0000cb80 | 0x8180a30c: | |
| 03_hssrx_phs_rot_ofs_ctl | 00000610 | | |
| 0x8180a310: 04_hssrx_phs_rot_posn1 | 00003a3a | 0x8180a314: | |
| 05_hssrx_phs_rot_posn2 | 0000002a | | |
| 0x8180a318: 06_hssrx_phs_rot_sta_ofs1 | 00000000 | 0x8180a31c: | |
| 07_hssrx_phs_rot_sta_ofs2 | 00000000 | | |
| 0x8180a320: 08_hssrx_dfe_ctl_PHY | 00002002 | 0x8180a324: | |
| 09_hssrx_dfe_smpl_snap1 | 00000000 | | |
| 0x8180a328: 0A_hssrx_dfe_smpl_snap2 | 00008000 | 0x8180a32c: | |
| 0B_hssrx_vga_ctl1 | 00004015 | | |
| 0x8180a330: 0C_hssrx_vga_ctl2 | 00007aa0 | 0x8180a334: | |
| 0D_hssrx_vga_ctl3 | 000009e4 | | |
| 0x8180a338: 0E_hssrx_pwr_mgmt_ctl | 0000001f | 0x8180a33c: | |
| 0F_hssrx_iqamp_ctl1 | 0000001a | | |
| 0x8180a340: 10_hssrx_iqamp_ctl2 | 00000006 | 0x8180a344: | |
| 11_hssrx_dacap_dacan_sel | 00000003 | | |
| 0x8180a348: 12_hssrx_dacap_dacan | 0000ffff | 0x8180a34c: | |
| 13_hssrx_daca_min | 00000000 | | |
| 0x8180a350: 14_hssrx_adac_ctl | 000000ff | 0x8180a354: | |
| 15_hssrx_ac_cp_ctl | 000031c3 | | |
| 0x8180a358: 16_hssrx_ac_cp_val | 00000050 | 0x8180a35c: | |
| 17_hssrx_dfe_h1h2h3_lcl_off_ch | 00000014 | | |
| 0x8180a360: 18_hssrx_dfe_h1h2h3_lcl_off_val | 00000000 | 0x8180a364: | |
| 19_hssrx_peaked_intg | 000000ff | | |
| 0x8180a368: 1A_hssrx_cdr_analog_sw | 0000ce00 | 0x8180a36c: | |
| 1B_hssrx_peaking_amp_init_c_PHY | 00000000 | | |
| 0x8180a370: 1C_hssrx_dac_dpc | 00000040 | 0x8180a374: | |
| 1D_hssrx_ddc | 00000000 | | |

| | | | |
|--|----------------|-------------|--|
| 0x8180a378: 1E_hssrx_int_stat_PHY | 0000c0f | 0x8180a37c: | |
| 1F_hssrx_dfe_func_ctl1_PHY | 0000ffff | | |
| 0x8180a380: 20_hssrx_dfe_func_ctl2_INV | 00007ebf | 0x8180a384: | |
| 21_hssrx_ofs_ch_dcc_qcc_idx | 00002000 | | |
| 0x8180a388: 22_hssrx_dfe_ofs_val | 0000097a | 0x8180a38c: | |
| 23_hssrx_h_coeff_bist | 0000043f | | |
| 0x8180a390: 24_hssrx_ac_cap_bist | 00000000 | 0x8180a394: | |
| 25_hssrx_max_gain_path_idx_res | 00007800 | | |
| 0x8180a398: 26_hssrx_loff_ctl | 00000054 | 0x8180a39c: | |
| 27_hssrx_sigdet_ctl | 00002180 | | |
| 0x8180a3a0: 28_hssrx_ana_ctl_sw | 00000000 | 0x8180a3a4: | |
| 29_hssrx_intg_dac_ofs | 0000dcd | | |
| 0x8180a3a8: 2A_hssrx_eye_ctl | 00000000 | 0x8180a3ac: | |
| 2B_hssrx_eye_met | 00000004 | | |
| 0x8180a3b0: 2C_hssrx_eye_met_err_cnt | 00000000 | 0x8180a3b4: | |
| 2D_hssrx_eye_met_pdf_eyec | 00000000 | | |
| 0x8180a3b8: 2E_hssrx_eye_met_pat_len | 0000007f | 0x8180a3bc: | |
| 2F_hssrx_dfe_func_ctl3 | 0000dfff | | |
| 0x8180a3c0: 30_hssrx_dfe_tap_ctl_idx_ptr | 00000008 | 0x8180a3c4: | |
| 31_hssrx_dfe_tap | 00003030 | | |
| 0x8180a3c8: 32_hssrx_lte_ctl_TUNE | 00001601 | 0x8180a3e4: | |
| 39_hssrx_int_stat2 | 000041ff | | |
| 0x8180a3e8: 3A_hssrx_ac_cpl_cur_src_adj | 00000040 | 0x8180a3ec: | |
| 3B_hssrx_dcd_ctl | 00007c54 | | |
| 0x8180a3f0: 3C_hssrx_dcc_ctl | 00000d84 | 0x8180a3f4: | |
| 3D_hssrx_qcc_ctl | 0000694e | | |
| 0x8180a3f8: 3E_hssrx_mac_test_ctl2 | 00000000 | 0x8180a3fc: | |
| 3F_hssrx_mac_test_ctl1 | 00000000 | | |
| 0x8180a348: 12_hssrx_dacap_dacan[02] | 00fd fffd | | |
| 0x8180a360: 18_hssrx_dfe_h1h2h3_lcl_off_va[00] | 0000 0000 0000 | | |
| 0000 0000 0000 0000 0000 | | | |
| 0x8180a360: 18_hssrx_dfe_h1h2h3_lcl_off_va[08] | 0000 0000 0000 | | |
| 0000 0000 0000 0000 0000 | | | |
| 0x8180a360: 18_hssrx_dfe_h1h2h3_lcl_off_va[16] | 0000 0000 0000 | | |
| 0000 0000 | | | |
| 0x8180a388: 22_hssrx_dfe_ofs_val[00][00] | 097a 7f00 0304 | | |
| 0000 7f09 007f | | | |
| 0x8180a388: 22_hssrx_dfe_ofs_val[03][00] | 0d01 7f00 7f09 | | |
| 007f 017e 7f00 | | | |
| 0x8180a388: 22_hssrx_dfe_ofs_val[06][00] | 7f7b 7f00 7907 | | |
| 007f 7c7f 7f00 | | | |
| 0x8180a388: 22_hssrx_dfe_ofs_val[09][00] | 057f 7f00 7b00 | | |
| 0000 7f0a 007f | | | |
| 0x8180a388: 22_hssrx_dfe_ofs_val[12][00] | 0509 007f 797f | | |
| 0000 7d79 0000 | | | |
| 0x8180a388: 22_hssrx_dfe_ofs_val[15][00] | 7b05 007f 077b | | |
| 0000 067d 0000 | | | |
| 0x8180a388: 22_hssrx_dfe_ofs_val[18][00] | 7a7d 0001 0101 | | |
| 0000 007b 0000 | | | |
| 0x8180a388: 22_hssrx_dfe_ofs_val[21][00] | 007b 0000 007b | | |
| 0000 007b 0000 | | | |
| 0x8180a388: 22_hssrx_dfe_ofs_val[24][00] | 017f 0000 7f01 | | |
| 0000 0001 0000 | | | |
| 0x8180a394: 25_hssrx_max_gain_path_idx_res[00] | 005d 0849 1107 | | |

```

18a3 20f0 28b0 3096 3800
0x8180a394: 25_hssrx_max_gain_path_idx_res[08]      40e0 48a0 5089
5800 6040 6800 70fa 7800
0x8180a3c4: 31_hssrx_dfe_tap[00]      fffe 8080 0000
0000 0030 0030 3030 3030
0x8180a3c4: 31_hssrx_dfe_tap[08]      3030 3030 3030
0000
0x8180a3e8: 3A_hssrx_ac_cpl_cur_src_adj[00]      0040 0040 0040
0040
0x8180a3ec: 3B_hssrx_dcd_ctl[00]      7c54 5c00 7c81
5c00 7c00
0x8180a3f0: 3C_hssrx_dcc_ctl[00]      0d84 0d00 0d00
0d41
0x8180a3f4: 3D_hssrx_qcc_ctl[00]      698a 694e

```

xfipcs, fec, aec, & aet registers

=====

```

0x81c68400: xfipcs_reg      [00] 00002040 00000080 00000000
00000000 00000001 00000008 00000000 00000000
0x81c68420: xfipcs_reg      [08] 00008c01 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c68440: xfipcs_reg      [16] 00000000 00000000 00000000
00000000 00000040 00000000 00000000 00000000
0x81c68460: xfipcs_reg      [24] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c68480: xfipcs_reg      [32] 00000004 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c68620: fec_32g_128g_reg [08] 00000000 00000000 00000000
00000000 00000000 00000000 00000000
0x81c68648: fec_32g_128g_reg [18] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c68a00: aec_reg      [00] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c68c00: aet_reg      [00] 00000000 00000000 00000000
00000000 00000000

```

bbc registers

=====

```

0x81c69800: bbc_trc      0 0 0 0 0 0 0
0
0x81c69840: bbc_trc      0 0 0 0 0 0 0
0
0x81c69880: bbc_trc      0 0 0 0 0 0 0
0
0x81c698c0: bbc_trc      0 0 0 0 0 0 0
0
0x81c69900: bbc_trc      0 0 0 0 0 0 0
0
0x81c69804: bbc_mbc      0 0 0 0 0 0 0
0
0x81c69844: bbc_mbc      0 0 0 0 0 0 0
0
0x81c69884: bbc_mbc      0 0 0 0 0 0 0
0

```

| | | | | | | | |
|-------------------------------------|----------|---|---|---|---|---|----------------------|
| 0x81c698c4: bbc_mbc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c69904: bbc_mbc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c69a00: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c69a20: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c69a40: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c69a60: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c69a80: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c69c00: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c69c20: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c69c40: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c69c60: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c69c80: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c69d00: bbc_fbpc | 00000000 | | | | | | |
| 00000000 | | | | | | | 0x81c69d04: bbc_csc |
| 0x81c69d08: bbc_rcc_inc | 00000000 | | | | | | 0x81c69d0c: |
| bbc_rqc_inc | 00000000 | | | | | | |
| 0x81c69d10: bbc_fbpc_inc | 00000000 | | | | | | 0x81c69d14: |
| bbc_tmc_inc | 00000000 | | | | | | |
| 0x81c69d18: bbc_threshold | 00080100 | | | | | | 0x81c69d1c: |
| bbc_counter_clr | 00000000 | | | | | | |
| 0x81c69d20: bbc_debug_en | 00000000 | | | | | | 0x81c69d24: bbc_ctrl |
| 00200020 | | | | | | | |
| 0x81c69d28: bbc_rqc_rcc_thresh | 00000055 | | | | | | 0x81c69d34: |
| bbc_bb_sc_n | 00000000 | | | | | | |
| 0x81c69d38: bbc_crd_reco_debug | 00000000 | | | | | | 0x81c69d3c: |
| bbc_crd_reco_debug_data | 00000000 | | | | | | |
| 0x81c69d40: bbc_multi_frm_loss_cnt | 00000000 | | | | | | 0x81c69d44: |
| bbc_multi_rdy_loss_cnt | 00000000 | | | | | | |
| 0x81c69d48: bbc_1frm_loss_recov_cnt | 00000000 | | | | | | 0x81c69d4c: |
| bbc_1rdy_loss_recov_cnt | 00000000 | | | | | | |
| 0x81c69d58: bbc_int_status | 00000000 | | | | | | 0x81c69d5c: |
| bbc_int_set | 00000000 | | | | | | |
| 0x81c69d60: bbc_int_first | 00000000 | | | | | | 0x81c69d64: |
| bbc_frm_rdy_rx_err_addr | 00000000 | | | | | | |
| 0x81c69d68: bbc_frm_rdy_tx_err_addr | 00000000 | | | | | | 0x81c69d6c: |
| bbc_trc_mbc_err_addr | 00000000 | | | | | | |
| 0x81c69d70: bbc_frm_rdy_rx_dbl_ecc | 00000000 | | | | | | 0x81c69d74: |
| bbc_frm_rdy_tx_dbl_ecc | 00000000 | | | | | | |
| 0x81c69d78: bbc_trc_mbc_dbl_ecc | 00000000 | | | | | | |
| 0x81c69d7c: bbc_fsm_status | 00001011 | | | | | | 0x81c69d80: |
| bbc_force_err | 00000000 | | | | | | |
| 0x81c69d84: bbc_crtd_avail0 | ffffffff | | | | | | 0x81c69d88: |

bbc_crdt_avail1 000000ff
0x81c69d8c: bbc_scratch 00000000

FPS registers

=====

0x81c68004: fps_er_enc_in 00000000 0x81c68008:
fps_er_crc 00000000
0x81c6800c: fps_er_trunc 00000000 0x81c68010:
fps_er_toolong 00000000
0x81c68014: fps_er_bad_eof 00000000 0x81c68018:
fps_er_enc_out 00000000
0x81c6801c: fps_er_bad_os 00000000 0x81c68020:
fps_er_flush 00000000
0x81c68024: fps_er_ifg 00000000 0x81c68038:
fps_er_crc_good_eof 00000000
0x81c6803c: fps_inv_arb 00000000 0x81c68040:
fps_slow_sts_status 00000000
0x81c68044: fps_tx_frm_cnt 00000000 0x81c68048:
fps_rx_frm_cnt 00000000
0x81c68050: fps_tx_word_cnt_hi 00000000 0x81c6804c:
fps_tx_word_cnt_lo 00000000
0x81c68058: fps_rx_word_cnt_hi 00000000 0x81c68054:
fps_rx_word_cnt_lo 00000000

BAL registers

=====

0x81c6f000: bal_desired_buf 00000000 0x81c6f004:
bal_alloc_buf 00000000
0x81c6f008: bal_busy_buf 00000000 0x81c6f00c:
bal_usable_buf 00000000
0x81c6f010: bal_max_bor_buf 00000000
0x81c6f014: bal_busy_buf_thresh 00000002

TXQ registers

=====

0x81c6b004: txq_phys_port_ctl 00450000
0x81c6b050: txq_link_skew 00000000
0x81c6b068: txq_cr_lk_dttm_intr_sts [00] 00000000 00000000
0x81c6b070: txq_cr_lk_dttm_intr_en [00] 00000000 00000000
0x81c6b024: txq_disc_frm_trap_cnt 00000014

FDS registers

=====

0x81c6c000: fds_rxf_ctl 00000002 0x81c6c004:
fds_rxf_wait_thresh 00000909
0x81c6c018: fds_rxf_first_error 00000000 0x81c6c01c:
fds_rxf_first_error_info 00000000
0x81c6c020: fds_rxf_inout_pkt_cnt 00000000
0x81c6c008: fds_rxf_err_int_status 00000000 0x81c6c024:
fds_rxf_fifo_status 00888888
0x81c6d000: fds_txf_ctl 0000003a 0x81c6d004:
fds_txf_wait_ifg_thresh 00a00106
0x81c6d008: fds_txf_err_int_status 00000000 0x81c6d024:
fds_txf_fifo_status 00088888

0x81c6d02c: fds_txf_bbc_scs 00000000

Logical TXQ registers

=====

| | | |
|------------------------------------|----------|----------------------------|
| 0x81c6b000: txq_log_port_ctl | 00000002 | 0x81c6b008: |
| txq_port_status | 00000000 | |
| 0x81c6b00c: txq_todo_flags | [00] | 00000000 00000000 |
| 0x81c6b014: txq_spd_match_desc | [00] | 00000000 00000000 00000000 |
| 00000000 | | |
| 0x81c6b024: txq_spd_match_desc | [04] | 00000014 |
| 0x81c6b028: txq_vc_weight | [00] | 01010101 01010101 01010101 |
| 01010101 | | |
| 0x81c6b038: txq_vc_weight | [04] | 01010101 01010101 01010101 |
| 01010101 | | |
| 0x81c6b048: txq_vc_weight | [08] | 01010101 00010101 |
| 0x81c6b054: txq_cong_dttm_ctrl | 00000000 | |
| 0x81c6b058: txq_cong_dttm_intr_sts | [00] | 00000000 00000000 |
| 0x81c6b060: txq_cong_dttm_intr_en | [00] | 00000000 00000000 |
| 0x81c6b078: txq_bw_limit_en_reg | [00] | 00000000 00000000 |
| 0x81c6b080: txq_bw_gua_en_reg | [00] | 00000000 00000000 |
| 0x81c6b088: txq_vc_group | [00] | 03030300 03030303 03030303 |
| 03030303 | | |
| 0x81c6b098: txq_vc_group | [04] | 03030303 03030303 03030303 |
| 03030303 | | |
| 0x81c6b0a8: txq_vc_group | [08] | 03030303 03030303 00000000 |
| 00000000 | | |
| 0x81c6b0b0: txq_bw_thresh_group | [00] | 00000000 00000000 00000000 |
| 00000000 | | |
| 0x81c6b0c0: txq_bw_thresh_group | [04] | 00000000 00000000 00000000 |
| 00000000 | | |
| 0x81c6b0d0: txq_bw_thresh_group | [08] | 00000000 00000000 00000000 |
| 00000000 | | |
| 0x81c6b0e0: txq_bw_thresh_group | [12] | 00000000 00000000 00000000 |
| 00000000 | | |
| 0x81c6b0f0: txq_bw_thresh_group | [16] | 00000000 00000000 00000000 |
| 00000000 | | |
| 0x81c6b100: txq_bw_thresh_group | [20] | 00000000 00000000 00000000 |
| 00000000 | | |
| 0x81c6b110: txq_bw_thresh_group | [24] | 00000000 00000000 00000000 |
| 00000000 | | |
| 0x81c6b120: txq_bw_thresh_group | [28] | 00000000 00000000 00000000 |
| 00000000 | | |
| 0x81c6b130: txq_bw_thresh_group | [32] | 00000000 00000000 00000000 |
| 00000000 | | |
| 0x81c6b140: txq_bw_thresh_group | [36] | 00000000 00000000 00000000 |
| 00000000 | | |

txq Congestion detection Statistics RAM

=====

| | | |
|-------------------|----------|-------------------|
| 0x81090820: vc[0] | 00000000 | 0x81090824: vc[1] |
| 00000000 | | |
| 0x81090828: vc[2] | 00000000 | 0x8109082c: vc[3] |
| 00000000 | | |
| 0x81090830: vc[4] | 00000000 | 0x81090834: vc[5] |

```

00000000
0x81090838: vc[6]      00000000      0x8109083c: vc[7]
00000000
0x81090840: vc[8]      00000000      0x81090844: vc[9]
00000000
0x81090848: vc[10]     00000000      0x8109084c: vc[11]
00000000
0x81090850: vc[12]     00000000      0x81090854: vc[13]
00000000
0x81090858: vc[14]     00000000      0x8109085c: vc[15]
00000000
0x81090860: vc[16]     00000000      0x81090864: vc[17]
00000000
0x81090868: vc[18]     00000000      0x8109086c: vc[19]
00000000
0x81090870: vc[20]     00000000      0x81090874: vc[21]
00000000
0x81090878: vc[22]     00000000      0x8109087c: vc[23]
00000000
0x81090880: vc[24]     00000000      0x81090884: vc[25]
00000000
0x81090888: vc[26]     00000000      0x8109088c: vc[27]
00000000
0x81090890: vc[28]     00000000      0x81090894: vc[29]
00000000
0x81090898: vc[30]     00000000      0x8109089c: vc[31]
00000000
0x810908a0: vc[32]     00000000      0x810908a4: vc[33]
00000000
0x810908a8: vc[34]     00000000      0x810908ac: vc[35]
00000000
0x810908b0: vc[36]     00000000      0x810908b4: vc[37]
00000000
0x810908b8: vc[38]     00000000      0x810908bc: vc[39]
00000000

```

Logical STS registers

=====

```

0x81584a44: sts_ftb_type1_miss      00000000
0x81584a48: sts_ftb_type2_miss      00000000
0x81584a4c: sts_ftb_type6_miss      00000000
0x81584a50: sts_hard_zoning_miss    00000000
0x81584a54: sts_lun_zoning_miss     00000000
0x81584a5c: sts_unroutable          00000000
0x81581a74: sts_rte_cl2              00000000      0x81581a78:
sts_rte_cl3              00000000      0x81581a7c: sts_rte_link_ctl
00000000      0x81584a68: sts_tx_timeout          00000000

```

Logical STS filter registers

=====

```

0x815849c0: stsflt_trig      [00] 00000000 00000000 00000000
00000000
0x815849d0: stsflt_trig      [04] 00000000 00000000 00000000

```

```

00000000
0x815849e0: stsflt_trig [08] 00000000 00000000 00000000
00000000
0x815849f0: stsflt_trig [12] 00000000 00000000 00000000
00000000
0x81584a00: stsflt_trig [16] 00000000 00000000 00000000
00000000
0x81584a10: stsflt_trig [20] 00000000 00000000 00000000
00000000
0x81584a20: stsflt_trig [24] 00000000 00000000 00000000
00000000
0x81584a30: stsflt_trig [28] 00000000 00000000 00000000
00000000
0x81584a40: stsflt_trig [32]

```

Logical STS discard registers

=====

```

0x815822e4: disc_mcast_wka 00000000 0x815822e8:
disc_inv_did 00000000
0x815822ec: disc_cl1_cl4 00000000 0x815822f0:
disc_sid_chk_fail 00000000
0x815822f4: disc_inv_dom_egid_txpt 00000000 0x815822f8:
disc_vft_hop_cnt_1 00000000
0x815822fc: disc_classf 00000000 0x81582300:
disc_fcp_cdb_inv 00000000
0x81582304: disc_vfid_trap_enabled 00000000 0x81582308:
disc_vfid_hdr_chk_fail 00000000
0x8158230c: disc_shim_cksum_fail 00000000 0x81582310:
disc_fed_edit_cmd_err 00000000
0x81582314: disc_ftb_vm_mode 00000000 0x81582318:
disc_ftb_agn_t2_miss 00000000
0x8158231c: disc_ecb_reserved 00000000 0x81582320:
disc_ecb_de_pad_err 00000000
0x81582324: disc_ecb_de_tag_err 00000000 0x81582328:
disc_ecb_de_seq_err 00000000
0x8158232c: disc_ecb_err 00000000 0x81582330:
disc_ftb_type4_match 00000000
0x81582334: disc_fcp_rsp_ftb_type4 00000000 0x81582338:
disc_ftb_type5_match 00000000
0x8158233c: disc_ftb_type3_match 00000000 0x81582340:
disc_els_ftb_type3 00000000
0x81582344: disc_ftb_type1_match 00000000 0x81582348:
disc_els_rsp_ex_port 00000000
0x8158234c: disc_inv_drp_dps 00000000 0x81582350:
disc_did_lookup_miss 00000000
0x81582354: disc_ftb_type2_match 00000000 0x81582358:
disc_trpd_plogi_pdisc 00000000
0x8158235c: disc_type2_lookup_miss 00000000 0x81582360:
disc_ftb_type6_match 00000000
0x81582364: disc_els_rep_ex_port 00000000 0x81582368:
disc_els_sid_lkup_bit1 00000000
0x8158236c: disc_els_sid_lkup_bit0 00000000 0x81582370:
disc_bls_frm_trap_bit1 00000000
0x81582374: disc_ftb_token_err 00000000 0x81582378:

```

```

disc_asic_internal_err 00000000
0x8158237c: disc_hard_zone_miss 00000000 0x81582380:
disc_lun_zone_miss 00000000
0x81582384: disc_flt_frame_disc 00000000 0x81582388:
disc_flt_parity_err 00000000
0x8158238c: disc_frame_marked_du 00000000 0x81582390:
disc_frame_marked_to 00000000
0x81582394: disc_lkup_rte_prty_err 00000000

```

portstatsshow 54

```

stat_wtx 0 4-byte words transmitted
stat_wrx 0 4-byte words received
stat_ftx 0 Frames transmitted
stat_frx 0 Frames received
stat_c2_frx 0 Class 2 frames received
stat_c3_frx 0 Class 3 frames received
stat_lc_rx 0 Link control frames
received
stat_mc_rx 0 Multicast frames
received
stat_mc_to 0 Multicast timeouts
stat_mc_tx 0 Multicast frames
transmitted
tim_txcrd_z 0 Time TX Credit Zero
(2.5Us ticks)
tim_txcrd_z_vc 0- 3: 0 0 0 0
tim_txcrd_z_vc 4- 7: 0 0 0 0
tim_txcrd_z_vc 8-11: 0 0 0 0
tim_txcrd_z_vc 12-15: 0 0 0 0
lat_tot_pkt_vc 0- 3: 1 1 1 1
lat_tot_pkt_vc 4- 7: 1 1 1 1
lat_tot_pkt_vc 8-11: 1 1 1 1
lat_tot_pkt_vc 12-15: 1 1 1 1
lat_hi_time_vc 0- 3: 0 0 0 0
lat_hi_time_vc 4- 7: 0 0 0 0
lat_hi_time_vc 8-11: 0 0 0 0
lat_hi_time_vc 12-15: 0 0 0 0
lat_lo_time_vc 0- 3: 1 1 1 1
lat_lo_time_vc 4- 7: 1 1 1 1
lat_lo_time_vc 8-11: 1 1 1 1
lat_lo_time_vc 12-15: 1 1 1 1
max_latency_vc 0- 3: 1 1 1 1
max_latency_vc 4- 7: 1 1 1 1
max_latency_vc 8-11: 1 1 1 1
max_latency_vc 12-15: 1 1 1 1
latency_dma_ts 09-09-2024 UTC Mon 08:47:26 TXQ
Latency DMA TimeStamp
fec_cor_detected 0 Count of blocks that
were corrected by FEC
fec_uncor_detected 0 Count of blocks that
were left uncorrected by FEC
er_enc_in 0 Encoding errors inside
of frames

```


| | | |
|--------------------------|-----------------------------|--------------------------|
| er_crc | 0 | Frames with CRC errors |
| er_trunc | 0 | Frames shorter than |
| minimum | | |
| er_toolong | 0 | Frames longer than |
| maximum | | |
| er_bad_eof | 0 | Frames with bad end-of- |
| frame | | |
| er_enc_out | 0 | Encoding error outside |
| of frames | | |
| er_bad_os | 0 | Invalid ordered set |
| er_pcs_blk | 0 | PCS block errors |
| er_rx_c3_timeout | 0 | Class 3 receive frames |
| discarded due to timeout | | |
| er_tx_c3_timeout | 0 | Class 3 transmit frames |
| discarded due to timeout | | |
| er_unroutable | 0 | Frames that are |
| unroutable | | |
| er_unreachable | 0 | Frame with unreachable |
| destination | | |
| er_other_discard | 0 | Other discards |
| er_type1_miss | 0 | frames with FTB type 1 |
| miss | | |
| er_type2_miss | 0 | frames with FTB type 2 |
| miss | | |
| er_type6_miss | 0 | frames with FTB type 6 |
| miss | | |
| er_zone_miss | 0 | frames with hard zoning |
| miss | | |
| er_lun_zone_miss | 0 | frames with LUN zoning |
| miss | | |
| er_crc_good_eof | 0 | Crc error with good eof |
| er_inv_arb | 0 | Invalid ARB |
| er_single_credit_loss | 0 | Single vcrdy/frame loss |
| on link | | |
| er_multi_credit_loss | 0 | Multiple vcrdy/frame |
| loss on link | | |
| other_credit_loss | 0 | Link timeout/complete |
| credit loss | | |
| phy_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | Timestamp of |
| phy_port stats clear | | |
| lgc_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | Timestamp of |
| lgc_port stats clear | | |
| fec_corrected_rate | 0 | FEC Corrected blocks per |
| second | | |

portstats64show 54

| | | |
|------------|---|---------------------------------------|
| stat64_wtx | 0 | top_int : 4-byte words transmitted |
| | 0 | bottom_int : 4-byte words transmitted |
| stat64_wrx | 0 | top_int : 4-byte words received |
| | 0 | bottom_int : 4-byte words received |
| stat64_ftx | 0 | top_int : Frames transmitted |
| | 0 | bottom_int : Frames transmitted |
| stat64_frx | 0 | top_int : Frames received |
| | 0 | bottom_int : Frames received |

| | | |
|------------------------------|---|--|
| stat64_c2_frx | 0 | top_int : Class 2 frames received |
| | 0 | bottom_int : Class 2 frames received |
| stat64_c3_frx | 0 | top_int : Class 3 frames received |
| | 0 | bottom_int : Class 3 frames received |
| stat64_lc_rx | 0 | top_int : Link control frames received |
| | 0 | bottom_int : Link control frames |
| received | | |
| stat64_mc_rx | 0 | top_int : Multicast frames received |
| | 0 | bottom_int : Multicast frames received |
| stat64_mc_to | 0 | top_int : Multicast timeouts |
| | 0 | bottom_int : Multicast timeouts |
| stat64_mc_tx | 0 | top_int : Multicast frames transmitted |
| | 0 | bottom_int : Multicast frames |
| transmitted | | |
| tim64_rdy_pri | 0 | top_int : Time R_RDY high priority |
| | 0 | bottom_int : Time R_RDY high priority |
| tim64_txcrd_z | 0 | top_int : Time BB_credit zero |
| | 0 | bottom_int : Time BB_credit zero |
| er64_enc_in | 0 | top_int : Encoding errors inside of |
| frames | 0 | bottom_int : Encoding errors inside of |
| frames | | |
| er64_crc | 0 | top_int : Frames with CRC errors |
| | 0 | bottom_int : Frames with CRC errors |
| er64_trunc | 0 | top_int : Frames shorter than minimum |
| | 0 | bottom_int : Frames shorter than minimum |
| er64_toolong | 0 | top_int : Frames longer than maximum |
| | 0 | bottom_int : Frames longer than maximum |
| er64_bad_eof | 0 | top_int : Frames with bad end-of-frame |
| | 0 | bottom_int : Frames with bad end-of- |
| frame | | |
| er64_enc_out | 0 | top_int : Encoding error outside of |
| frames | 0 | bottom_int : Encoding error outside of |
| frames | | |
| er64_disc_c3 | 0 | top_int : Class 3 frames discarded |
| | 0 | bottom_int : Class 3 frames discarded |
| er64_pcs_blk | 0 | top_int : PCS block errors |
| | 0 | bottom_int : PCS block errors |
| stat64_rateTxFrame | 0 | Tx frame rate (fr/sec) |
| stat64_rateRxFrame | 0 | Rx frame rate (fr/sec) |
| stat64_rateTxPeakFrame | 0 | Tx peak frame rate (fr/sec) |
| stat64_rateRxPeakFrame | 0 | Rx peak frame rate (fr/sec) |
| stat64_rateTxWord | 0 | Tx Word rate (words/sec) |
| stat64_rateRxWord | 0 | Rx Word rate (words/sec) |
| stat64_rateTxPeakWord | 0 | Tx peak Word rate (words/sec) |
| stat64_rateRxPeakWord | 0 | Rx peak Word rate (words/sec) |
| stat64_PRJTFrames | 0 | top_int : Number of PRJT frames |
| returned to this port | 0 | bottom_int : Number of PRJT |
| frames returned to this port | | |
| stat64_PBSYFrames | 0 | top_int : Number of PBSY frames |
| returned to this port | 0 | bottom_int : Number of PBSY |

```

frames returned to this port
stat64_inputBuffersFull 0          top_int : Number of occurrences
when all input buffers full
                                0          bottom_int : Number of
occurrences when all input buffers full
stat64_rxClass1Frames 0          top_int : Number of class 1
frames received
                                0          bottom_int : Number of class 1
frames received
stat64_aveTxFrameSize 0          Average Tx Frame size
stat64_aveRxFrameSize 0          Average Rx Frame size
Lr_in      0          top_int
                                0          bottom_int
Ols_in     0          top_int
                                0          bottom_int
Lr_out     0          top_int
                                0          bottom_int
Ols_out    0          top_int
                                0          bottom_int
Link_failure 0          top_int
                                0          bottom_int
Invalid_CRC 0          top_int
                                0          bottom_int
Invalid_word 0          top_int
                                0          bottom_int
Protocol_err 0          top_int
                                0          bottom_int
Loss_of_sig 0          top_int
                                0          bottom_int
Loss_of_sync 0          top_int
                                0          bottom_int
er_bad_os  0          top_int : Invalid ordered set
                                0          bottom_int: Invalid ordered set

```

```

portrouteshow 54
port address ID: 0x013600
external unicast routing table:
  0: Embedded
 255: Embedded
internal unicast routing table:
  0: Embedded

```

```
portcamshow 54
```

```

-----
Port  SID used  DID used  SID entries  DID entries
54    0         0        000000     000000
-----

```

```

ptbufshow, ptcreditshow, ptdatashow, ptstatsshow 54
S:
S:VF Enable:          1
S:
S:C4 Global Variable:

```

```

S:-----
-----
S:trace_stop:          0
S:
S:C4 Phy Data Pointers: c4_phyp = 0xb6acd140
S:-----
-----
S:tnodep              0xbb83a000      pt
   0x4302800d
S:proto_phyp          0xb88085a0      phy_cfg
0xb6ace180
S:c4_chp              0x97e28000      c4_lgcp
0x97f7c000
S:c4_phy_regp         0x81c68000      proc_dir
0xb8517820
S:-----
-----
S:magic_id            0xc4345678      num_port_timer      12
S:prev_if_id         0x4302000d      S:ftx                0
   tov              0
S:initialized         0      port_idx            13
S:ui_idx              54      slot_no
   0
S:blade_idx          13      sw_usr_ports        400
S:unused              0      intr_debounced
   0
S:aec_status          0x0      reason_code
   0
S:debug               0x00000004      debug_trc_line      0
S:rxbuf_list_head    0xffffffff      rxbuf_list_tail
0xffffffff
S:isAePort            0      port_misc_data
   0
S:num_fault1_rx_disc  0      num_fault2_rx_disc  0
S:p_llli_cause0       0      p_sig_regained      0
S:p_sync_regained     0      enc_out
   0x0
S:cached_fps_status   0      cached_sts_status   0
S:cached_er_crc_good_eof 0
S:cached_er_bad_os    0      cached_er_too_long  0
S:cached_er_trunc     0
cached_tot_er_crc_good_eof 0
S:num_pt_excess_intr  0      num_no_fid          0
S:num_fault1_cnt      0      num_fault2_cnt
   0
S:num_fault_lip       0      num_fault_llli      0
S:num_fault_rx_fifo   0      num_fault_hss       0
S:num_fault_bwait     0      lli_intr_prim
   0
S:num_sw_link_to      0
be_link_err_mon_count 0
S:ecb_enc_enabled     0      ecb_comp_enabled
   0
S:ecb_rsv_enc         0      ecb_rsv_comp        0

```

```

S:ecb_enc_bm          0x0          ecb_key_index
0xffffffff
S:fab_idx            4
S:num_be_lto         0          lto_count_reset_intvl
0
S:lr_count_reset_intvl      0          num_be_lr
0
S:num_fault_qsfp      0          check_lto
0
S:credit_loaded       0          num_credit_overrun
0
S:fec_enabled        0x0          fec_los_to_flag          0x0
S:phy_stats_clear_ts    1725611419      pcs_err_online
0
S:pcs_err_light_det    0          pcs_err_ignore
0
S:pcs_blk_err        0          pcs_hiber          0
S:phy_port_status     0          ecb_enc_lr_count
0
S:dport_mode         0          avoid_lto_det          0
S:sn_debounced       0x0          sn_started_kr_reqd     0
S:major_timer_started  0x0          ready_bm              0x0
S:parln_1_bm         0x0          parln_0_bm            0x0
S:be_los_of_sync_event_intvl
be_los_of_sync_event  0
S:errataPtenable_cntr  0          errataPoll_cntr
0
S:jda_rx_sig_loss_det  0          jda_rx_sig_loss_cnt
0
S:encrypt_blk_error   0
S:
S:      c4_trunk
S:=====
S:mark_ts            0x0          deskew          0x0
S:master_phyp       0x0
S:
S:adelay[00]: 0x00000000 0x00000000 0x00000000 0x00000000
S:adelay[04]: 0x00000000 0x00000000 0x00000000 0x00000000
S:
S:      c4_buf
S:=====
S:tx_csc            0          rx_csc
0
S:ld_vc_credits     0          tx_flag          0x0
S:alloc_buffers     0          req_buffers      0
S:est_buffers       20          ld_use_est       0
S:bb_sc_n           0          rx_bb_sc_n
0
S:data_cr           5          nondata_cr
6
S:cr_enable         0
S:ld_nondata_cr     6          tnodep
0xbb83a0e0
S:tx_credits[0] 0 0 0 0 0 0 0 0

```

```

S:tx_credits[8] 0 0 0 0 0 0 0 0
S:tx_credits[16] 0 0 0 0 0 0 0 0 0 0
S:tx_credits[24] 0 0 0 0 0 0 0 0 0 0
S:tx_credits[32] 0 0 0 0 0 0 0 0 0 0
S:rx_credits[0] 0 0 0 0 0 0 0 0
S:rx_credits[8] 0 0 0 0 0 0 0 0
S:rx_credits[16] 0 0 0 0 0 0 0 0 0 0
S:rx_credits[24] 0 0 0 0 0 0 0 0 0 0
S:rx_credits[32] 0 0 0 0 0 0 0 0 0 0
S:tx_mbc[0] 0 0 0 0 0 0 0 0
S:tx_mbc[8] 0 0 0 0 0 0 0 0
S:tx_mbc[16] 0 0 0 0 0 0 0 0
S:tx_mbc[24] 0 0 0 0 0 0 0 0
S:tx_mbc[32] 0 0 0 0 0 0 0 0
S:rx_mbc[0] 0 0 0 0 0 0 0 0
S:rx_mbc[8] 0 0 0 0 0 0 0 0
S:rx_mbc[16] 0 0 0 0 0 0 0 0
S:rx_mbc[24] 0 0 0 0 0 0 0 0
S:rx_mbc[32] 0 0 0 0 0 0 0 0

```

S:

S:C4 Chip Variables: c4_phy->c4_chp = 0x97e28000

S:-----

S:version = 2.1

S:magic_id 0xc4234567 init_state 0x8

S:reset_reg_mem 0x1

S:ch_int0_en_bm 0x0 intr0_cause 0x0

S:ch_int1_en_bm 0x0 intr1_cause 0x0

S:ch_int2_en_bm 0x0 intr2_cause 0x0

S:ch 0x43010080 ch_cfg

0xb7013ba0

S:raslog_hdl.hndl 0x0 obj_halted 0x0

S:c4_chip_regp 0x80000000 c4_fpg_regp

0x81800000

S:num_chip_timer 0x5

S:hi_task_bm 0x0 lo_task_bm 0x0

S:c4_deferq.q_head 0x0 c4_deferq.q_tail 0x0

S:c4_tmrq.q_head 0x0 c4_tmrq.q_tail 0x0

slot_no 0

S:chip_inst 0 chip_idx 0

S:pll_initialized 1

pll_serdes_initialized 1

S:init_tries 0 init_ptEnableBM

0xba01b488

S:tick_polling 0xb980c9c0 sec_polling

0xb980c960

S:bb_fid 129

S:ecb_key_bm[0] 0x0 ecb_key_bm[1] 0x0

S:ecb_key_bm[2] 0x0 ecb_key_bm[3] 0x0

S:is_chip_enc_enabled 0

is_chip_comp_enabled 0x0

S:ftb_rsrcp->ftb_flags 0x0 act_rsrcp->act_flag 0x1

S:lue_rsrcp->lue_flags[0] 0x0 lue_rsrcp-

>lue_flags[1] 0x0

```

S:c4_phyp[00]: 0xb6ab0000 0xb6ab2080 0xb6ab4100 0xb6ab6180
S:c4_phyp[04]: 0xb6ab9040 0xb6abb0c0 0xb6abd140 0xb6ac0000
S:c4_phyp[08]: 0xb6ac2080 0xb6ac4100 0xb6ac6180 0xb6ac9040
S:c4_phyp[12]: 0xb6acb0c0 0xb6acd140 0xb6ad0000 0xb6ad2080
S:c4_phyp[16]: 0xb6ad4100 0xb6ad6180 0xb6ad9040 0xb6adb0c0
S:c4_phyp[20]: 0xb6add140 0xb6ae0000 0xb6ae2080 0xb6ae4100
S:c4_phyp[24]: 0xb6ae6180 0xb6ae9040 0xb6aeb0c0 0xb6aed140
S:c4_phyp[28]: 0xb6af0000 0xb6af2080 0xb6af4100 0xb6af6180
S:c4_phyp[32]: 0xb6af9040 0xb6afb0c0 0xb6afd140 0xb6b00000
S:c4_phyp[36]: 0xb6b02080 0xb6b04100 0xb6b06180 0xb6b09040
S:c4_phyp[40]: 0xb6b0b0c0 0xb6b0d140 0xb6b10000 0xb6b12080
S:c4_phyp[44]: 0xb6b14100 0xb6b16180 0xb6b19040 0xb6b1b0c0
S:c4_phyp[48]: 0xb6b1d140 0xb6b20000 0xb6b22080 0xb6b24100
S:c4_phyp[52]: 0xb6b26180 0xb6b29040 0xb6b2b0c0 0xb6b2d140
S:c4_phyp[56]: 0xb6b30000 0xb6b32080 0xb6b34100 0xb6b36180
S:c4_phyp[60]: 0xb6b39040 0xb6b3b0c0 0xb6b3d140 0xb6b40000
S:c4_lgcp[00]: 0x97f48000 0x97f4c000 0x97f50000 0x97f54000
S:c4_lgcp[04]: 0x97f58000 0x97f5c000 0x97f60000 0x97f64000
S:c4_lgcp[08]: 0x97f68000 0x97f6c000 0x97f70000 0x97f74000
S:c4_lgcp[12]: 0x97f78000 0x97f7c000 0x97f80000 0x97f84000
S:c4_lgcp[16]: 0x97f88000 0x97f8c000 0x97f90000 0x97f94000
S:c4_lgcp[20]: 0x97f98000 0x97f9c000 0x97fa0000 0x97fa4000
S:c4_lgcp[24]: 0x97fa8000 0x97fac000 0x97fb0000 0x97fb4000
S:c4_lgcp[28]: 0x97fb8000 0x97fbc000 0x97fc0000 0x97fc4000
S:c4_lgcp[32]: 0x97fc8000 0x97fcc000 0x97fd0000 0x97fd4000
S:c4_lgcp[36]: 0x97fd8000 0x97fdc000 0x97fe0000 0x97fe4000
S:c4_lgcp[40]: 0x97fe8000 0x97fec000 0x97ff0000 0x97ff4000
S:c4_lgcp[44]: 0x97ff8000 0x97ffc000 0x8e000000 0x8e004000
S:c4_lgcp[48]: 0x8e008000 0x8e00c000 0x8e010000 0x8e014000
S:c4_lgcp[52]: 0x8e018000 0x8e01c000 0x8e020000 0x8e024000
S:c4_lgcp[56]: 0x8e028000 0x8e02c000 0x8e030000 0x8e034000
S:c4_lgcp[60]: 0x8e038000 0x8e03c000 0x8e040000 0x8e044000
S:chip_timers[00]: 0xb980c720 0xb980c780 0xb980c7e0 0xb980c840
S:chip_timers[04]: 0xb980c8a0 0xb980c900
S:disc_trap_enable_required      0x0          rxlp_disc_log_stop
          0x0
S:curr_rxlp_frm_cnt      0x0          curr_rxlp_disc_frm_cnt  0x0
S:sw_disc_frm_cnt      0x0          last_disc_frm_cnt      0x0
S:txq_nopop_pr_cnt      0x0          pollErrataDfe_ptBM
0xba01b4b0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][0]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][1] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][2]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][0] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][1]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][2] 0x0
S:
S:C4 Logical Port Variables
S:-----
-----
S:c4_lgc_regp      0x81c68000
S:c4_phyp:
S:      0xb6acd140      0x0          0x0          0x0

```

```

S:      0x0          0x0          0x0          0x0

S:master_phyp      0xb6acd140      if_id
0x4302000d
S:min_phyp          0x0          max_phyp          0x0
S:num_phy_ports    1          lgc_num          13
S:num_iu_to        0          sw_txq_bm
0
S:port_fid         129          unused          0
S:port_group       1          lgc_stats_clear_ts
1725611419
S:domain_tbl_sel   0          area_tbl_sel
0
S:egid_tbl_sel     0
S:serv_lo_bm       0x0
S:
S:Proto Phy Variables:
S:-----
-----
S:magic_id         0xc4123456      asic_phyp
0xb6acd140
S:port_id          0x4302800d      phy_cfg
0xb6ace180
S:upsm_hdl         0xb80138c0      physm_hdl
0xb8013640
S:ov_snsn_hdl      0xb8013500      sw_snsn_hdl
0xb80135a0
S:ov_lksm_hdl      0xb80136e0      sw_lksm_hdl
0xb8013780
S:trksm_hdl        0xb8013820      lr_flag          0x0
S:lr_active        0x0          qsfp_txxr_rate_sel
0x0
S:
S:UPSM            UP00: UPST_PORT_DISABLED    --> UP00: UPST_PORT_DISABLED
S:SNSM(OV)        SN00: OV_SNST_STOPPED      --> SN00: OV_SNST_STOPPED
S:SNSM(SW)        SW00: SW_SNST_STAGE_WS  --> SW00: SW_SNST_STAGE_WS
S:PHYSM           PP00: PHYST_STOPPED      --> PP00: PHYST_STOPPED
S:LKSM(OV)        LK00: OV_LKST_INACTIVE    --> LK00: OV_LKST_INACTIVE
S:LKSM(SW)        SW13: INACTIVE      --> SW13: INACTIVE
S:TRKSM           TRK0: TRKST_INIT      --> TRK0: TRKST_INIT
S:
S:physm variables:
S:-----
-----
S:proto_phyp       0xb88085a0      physm_hdl
0xb8013640
S:force_offline    0          copper          0
S:fault_reason     0: UNKNOWN
S:phy_media_present 0
S:
S:snsn variables:
S:-----
-----
S:speed            0xff          proto_phyp

```



```

0xb88085a0
S:hw_sn_tries_left      0x0          sw_sn_tries_left      0x0
S:curr_txsp_count      0x0          curr_tx_indx
S:tx_max                0x0          curr_rxsp_count
      0x0
S:curr_tx               0x0          curr_rx_indx
      0x0
S:rx_max                0x0          rx_mem
      0x0
S:curr_rx               0x0
      0x0
S:rxsp_rec_count       0x0
S:nc_start              0x0          tx_start              0x0
S:sync_start           0x0          sync_present          0x0
S:diag_auto            0x0          diag_speed            0xff
S:striped_wd_tov       3000          hw_wd_tov
      3000
S:step                  0x0          qsfp28_speed_mode
      0x0
S:qsfp_mode0_hw_sn_tries_left 0x0
S:qsfp_mode1_hw_sn_tries_left 0x0
S:
S:lksm variables:
S:-----
-----
S:proto_phyph          0xb88085a0    ov_lksm_hdl
0xb80136e0
sw_lksm_hdl            0xb8013780
num_lf1                0
S:hw_link_tries_left  0          sw_link_tries_left   0
S:buf_ptype            0x0          stored_entry_state   0x6
S:handshake_owner      0x0          mark_unsent
      0x0
S:busybuf_stuck        0x0          lr_wait              0x0
S:
S:trksm variables:
S:-----
-----
S:Not a trunk port
S:
S:upsm variables:
S:-----
-----
S:proto_phyph          0xb88085a0    upsm_hdl
0xb80138c0
S:bb_credits           0          port_beacon          0
S:port_diag_flag       0          force_offline
      0
S:port_fault_rsn       0: PORT_NO_FAULT
S:retry_init_rsn       0: UNKNOWN
S:limit_reason         0          linit_result         0
S:ie_fctl_mode         0          fec_in_sync_tries_left 0
S:retry_sn_fail_init   0
retry_link_fail_init   0

```

```

S:excess_lr_count      0
S:
S:c4_ch_cfg
S:-----
-----
S:c4_desc_ring_size   256      292      256      256      292
292      2      292      292
S:thresh_def          0      16      1      0
S:intr_tries          500      cmem_pattern
0xdeadbeef
S:cmem_pattern_upwd   2      cmem_init_time      16
S:cmem_init_tries     5
S:ctrl_par_thresh     2      data_par_thresh
4
S:cam_par_thresh      4      buf_loss_thresh
12
S:crit_par_thresh     2      non_crit_par_thresh
6
S:pci_abort_thresh    10      pci_err_thresh      5
S:excess_chintr_thresh 8      sw_err_thresh      20
S:err_sample_period   300      intr_sleep
20000
S:frame_timeout       2500      proxy_dev      16384
S:vf_route            81920      qos      2048
S:stats 2048          f_redirect      2048
S:rsp_trap            2048      lun_zoning      20480
S:area_mode           0      ftb_max_loop[0]    0
S:ftb_max_loop[1]     6      ftb_max_loop[2]    9
S:ftb_max_loop[3]     10     ftb_max_loop[4]    10
S:ftb_max_loop[5]     5      ftb_max_loop[6]    6
S:ftb_seg_size[0]     0      ftb_seg_size[1]
16384
S:ftb_seg_size[2]     65536     ftb_seg_size[3]
16384
S:ftb_seg_size[4]     16384     ftb_seg_size[5]
65536
S:ftb_seg_size[6]     16384     ftb_seg_base[0]    0
S:ftb_seg_base[1]     0      ftb_seg_base[2]
65536
S:ftb_seg_base[3]     16384     ftb_seg_base[4]
32768
S:ftb_seg_base[5]     131072    ftb_seg_base[6]
49152
asic_err_monitor_period1 300
asic_err_monitor_period2 86400
zone_chk_to_poll_period 25
zone_chk_class2_reject_tov 220
S:
S:c4_phy_cfg
S:-----
-----
S:version = 2.1
S:pt                  0x4302800d      fab_ptr
0x9a800000

```

```

S:fabattr                                0x9a8000d4      fab_iop
      0x9a800050
S:cfgbm                                  0xbb839e04      port_ctrl
0xb6ace198
S:pcap.pcap_bm                            0x8d215547      pcap.pcap2_bm
0x2588289
S:pcap.pcap3_bm                            0x1bebe0c
ui_idx                                     54              S:slot_no
      0
is_icl                                     0              S:sw_usr_ports      400
S:neg_speed                               0 0 0 0 0 0
S:my_domain                               0x1              port_mode            0x0
S:hw_sn_maxtries                           100             sw_sn_maxtries
      0
S:hw_link_maxtries                         10              sw_link_maxtries    5
S:rx_cyc_tov                              28              rttov               300
S:bufrdy_tov                              300             busybuf_tov         286
S:mark_tov                                300             lksm_tov            3000
S:buf_dealloc_wait                         4              hw_wd_tov           3000
S:hw_lk_train_tov                         540             hw_lk_test_tov
      150
S:syswait_tx_12_lips                      1              lip_rx_tov          55
S:al_time_tov                             15             lp_tov              2000
S:intr_tries_port                         500             intr_mod_debounce
      250
S:intr_lsrflt_debounce                    500             intr_efifo_debounce 100
S:port_no_fid                             3              excess_ptintr_thresh 8
S:port_fault1_thresh                      100             port_fault1_spur_thresh 250
S:port_fault1_disc_thresh                  500
port_fault1_disc_spur_thresh              1000
S:port_fault2_thresh                       5              losync_tov          100
S:port_sw_link_to                         15             en_8g_scramble
      1
frc_hw_sn_mode                            0x1
S:enc_poll_thresh                         0              fec_enable
      0
S:fec_in_sync_to                          50             fec_in_sync_try_max
      4
S:port_be_lto_threshold                    100             port_be_lr_threshold
      2
S:be_cr_in_sync_to                        5
port_credit_overnrun_thresh               10
S:jda_sfp_losig_tov                       400
jda_sfp_losig_try_max                     30
S:striped_wd_tov                          3000
no_sync_debounce                          1200
S:
S:      fab_iop
S:=====
S:fab_iop->interop_mode 0x0                fab_iop->lab_mode    0x0
S:fab_iop->fl_bbc                        0x0                fab_iop->fl_fan
      0x0
S:fab_iop->fl_cls                         0x4                fab_iop->fl_rscn
      0x0

```

```

S:fab_iop->domain_id_offset      0x60          fab_iop-
>mcmt_fabric_mode      0x0
S:fab_iop->mcmt_default_zone      0x0          fab_iop-
>mcmt_safe_zone      0x0
S:
S:      port_ctrl
S:=====
S:port_ctrl.port_type      1          port_ctrl.port_grp      1
S:port_ctrl.port_number 54          port_ctrl.vc_mode      1
S:
S:      port_ctrl.lcap
S:=====
S:has_serdes      0          has_media      1
S:topology      1          skip_nego      0
S:skip_pnego      0          skip_init_event      0
S:en_shim      0          speed_neg
      1
S:loop_back      0          num_speeds      5
S:fec_enable      0
S:
S:      port_ctrl.speed_list array
S:=====
S:speed_list[0].auto_neg 1          speed_list[0].lnk_speed 0x0000000a
S:speed_list[1].auto_neg 1          speed_list[1].lnk_speed 0x00000008
S:speed_list[2].auto_neg 1          speed_list[2].lnk_speed 0x00000006
S:speed_list[3].auto_neg 1          speed_list[3].lnk_speed 0x00000005
S:speed_list[4].auto_neg 1          speed_list[4].lnk_speed 0x00000003
S:speed_list[5].auto_neg 0          speed_list[5].lnk_speed 0x00000000
S:
S:      port_ctrl.cm
S:=====
S:port_ctrl.cm.num_vcs      8
S:port_ctrl.cm.min_bufs      8
S:port_ctrl.cm.cr_shar_bufs 0
S:port_ctrl.vc_alloc
S:port_ctrl.vc_alloc      2 0 1 1 1 1 1 1
S:port_ctrl.vc_alloc      0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.norm_vc_alloc
S:port_ctrl.norm_vc_alloc      4 0 5 5 5 5 1 1
S:port_ctrl.norm_vc_alloc      0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.cm.skip_bb_credit      0
S:port_ctrl.cm.use_shim_based_sublist      0
S:
S:      port_ctrl.serdes_set
S:=====
S:serdes_type      0x8
S:serdes_data_t.ibm_hss_serdes.tx_drive_power      0x1
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b_sign      0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b      0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_a      0x0
S:serdes_data_t.ibm_hss_serdes.rxeq      0x0
S:

```

```

S:      cfgbm
S:=====
S:old_distance      0x0          gport_lockdown      0x0
S:tpport            0x1          speed                0x0
S:disable_eport     0x0          fcacc                0x0
S:lport_lockdown    0x0          0x0                  priv_lport_lockdown
                        0x0
S:vcxlt_linit       0x0          delay_flogi          0x0
S:isl_interop       0x0          distance              0x0
S:BufStarvFlag      0x0          credit_sharing        0x0
S:lport_halfduplex  0x0          lport_fairness        0x0
S:soft_neg          0x0          asn_frc_hwretry       0x0
S:cr_recov          0x0          fport_buffers         0x0
S:export            0x0          0x0                  export_mode
                        0x0
S:csctl_en          0x0          mirror_port          0x0
S:fault_delay       0x0          non_dfe               0x0
S:fec_configured*(0=ENAB) 0          0                    fec_tts
                        0
S:port_persistently_disabled (permanently) 0 (0)
S:
S:      cfg property
S:=====
S:priv_pcfg_bm      0x00000000          lgcl_pcfg_bm
0xbb839e44
S:fport_buffer      0x00000000
S:
S:
S:C4 Discard Cntrs: rxlp_stats = 0xb6acd4f0
S:-----
-----
S:disc_mcast_wka    0x0          disc_inv_did          0x0
S:disc_cl1_cl4      0x0          disc_sid_chk_fail     0x0
S:disc_inv_dom_egid_txpt 0x0          0x0                  disc_vft_hop_cnt_1
                        0x0
S:disc_classf       0x0          0x0                  disc_fcp_cdb_inv      0x0
S:disc_vfid_trap_enabled 0x0          0x0
disc_vfid_hdr_chk_fail 0x0
S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err 0x0
S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err 0x0
S:disc_ftb_vm_mode  0x0          disc_ftb_agnt2_miss   0x0
S:disc_ecb_de_pad_err 0x0          disc_ecb_de_tag_err   0x0
S:disc_ecb_de_seq_err 0x0          disc_ecb_err           0x0
S:disc_ftb_type4_match 0x0          disc_fcp_rsp_ftb_type4 0x0
S:disc_fcp_rsp_ftb_type4 0x0          0x0                  disc_ftb_type5_match
                        0x0
S:disc_ftb_type3_match 0x0          disc_els_ftb_type3    0x0
S:disc_ftb_type1_match 0x0          disc_els_rsp_ex_port  0x0
S:disc_inv_drp_dps  0x0          disc_did_lookup_miss  0x0
S:disc_ftb_type2_match 0x0          disc_trpd_plogi_pdisc 0x0
S:disc_type2_lookup_miss 0x0          0x0                  disc_ftb_type6_match
                        0x0
S:disc_els_rep_ex_port 0x0          disc_els_sid_lkup_bit1 0x0
S:disc_els_sid_lkup_bit0 0x0          0x0

```

```

disc_bls_frm_trap_bit1 0x0
S:disc_ftb_token_err 0x0
S:disc_hard_zone_miss 0x0
S:discflt_frame_disc 0x0
S:disc_frame_marked_du 0x0
E:Connection type: FE
E:Port type: E_port
E:Trunk port: No
E:Configured Speed: AUTO_SPEED_NEGO
E:Max Capable Speed: 32G
E:Current SNSM Speed: UNDEFINED
E:Hardware TX Speed: 32G (0x00000004)
E:Hardware RX Speed: 32G (0x00000040)
E:
E:Interrupts: 0 Link_failure: 0
Loss_of_sync: 0 Loss_of_sig: 0
E:Lli: 0 Invalid_word: 0
E:trapped_frm: 0 fwd_status_ok: 0
E:fwd_timeout: 0 fwd_tx_unavail: 0
E:fwd_unroutable: 0 fwd_zone_out: 0
E:fwd_other_err: 0 frm_err_discard: 0
E:Fltr listA: 0 Fltr listB: 0
E:Zone trap fwd: 0 Zone trap disc: 0
E:shim_csum: 0 RTE_perr: 0
E:Invalid_crc: 0 Delim_err: 0
E:Protocol_err: 0
E:Lr_in: 0 Lr_out: 0
E:Ols_in: 0 Ols_out: 0

```

filterportshow 54

FILTER DATA

```

-----
Shadow settings:
Filter Enable: 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000

```

Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass: 0x00000000

Real settings:

Enable RAM: 0x00000000, 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass RAM: 0x00000000

Shadowed filters:

Filter 0: Not Installed (MIRROR1)(LISTA)

```
    c4_fldenable[0] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[0] = 0x00000000,c4_fltr_config[0] = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
    c4_fldenable[1] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[1] = 0x00000000,c4_fltr_config[1] = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
    c4_fldenable[2] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[2] = 0x00000000,c4_fltr_config[2] = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
    c4_fldenable[3] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[3] = 0x00000000,c4_fltr_config[3] = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
    c4_fldenable[4] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[4] = 0x00000000,c4_fltr_config[4] = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
    c4_fldenable[5] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[5] = 0x00000000,c4_fltr_config[5] = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
    c4_fldenable[6] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[6] = 0x00000000,c4_fltr_config[6] = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
    c4_fldenable[7] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[7] = 0x00000000,c4_fltr_config[7] = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
    c4_fldenable[8] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[8] = 0x00000000,c4_fltr_config[8] = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
    c4_fldenable[9] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[9] = 0x00000000,c4_fltr_config[9] = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
    c4_fldenable[10] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[10] = 0x00000000,c4_fltr_config[10] =
0x00000000
Filter 11: Not Installed (SIM)(LISTA)
    c4_fldenable[11] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[11] = 0x00000000,c4_fltr_config[11] =
0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
    c4_fldenable[12] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[12] = 0x00000000,c4_fltr_config[12] =
0x00000000
```


Filter 13: Not Installed (UNUSED)(LISTA)
c4_fldenable[13] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[13] = 0x00000000,c4_fltr_config[13] =
0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
c4_fldenable[14] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[14] = 0x00000000,c4_fltr_config[14] =
0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
c4_fldenable[15] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[15] = 0x00000000,c4_fltr_config[15] =
0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
c4_fldenable[16] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[16] = 0x00000000,c4_fltr_config[16] =
0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
c4_fldenable[17] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[17] = 0x00000000,c4_fltr_config[17] =
0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
c4_fldenable[18] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[18] = 0x00000000,c4_fltr_config[18] =
0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
c4_fldenable[19] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[19] = 0x00000000,c4_fltr_config[19] =
0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
c4_fldenable[20] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[20] = 0x00000000,c4_fltr_config[20] =
0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
c4_fldenable[21] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[21] = 0x00000000,c4_fltr_config[21] =
0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
c4_fldenable[22] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[22] = 0x00000000,c4_fltr_config[22] =
0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
c4_fldenable[23] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[23] = 0x00000000,c4_fltr_config[23] =

```
0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
    c4_fldenable[24] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[24] = 0x00000000,c4_fltr_config[24] =
0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
    c4_fldenable[25] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[25] = 0x00000000,c4_fltr_config[25] =
0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
    c4_fldenable[26] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[26] = 0x00000000,c4_fltr_config[26] =
0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
    c4_fldenable[27] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[27] = 0x00000000,c4_fltr_config[27] =
0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
    c4_fldenable[28] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[28] = 0x00000000,c4_fltr_config[28] =
0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
    c4_fldenable[29] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[29] = 0x00000000,c4_fltr_config[29] =
0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    c4_fldenable[30] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[30] = 0x00000000,c4_fltr_config[30] =
0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    c4_fldenable[31] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[31] = 0x00000000,c4_fltr_config[31] =
0x00000000
```

Real filters:

```
Filter 0: Not Installed (MIRROR1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
```

```
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 11: Not Installed (SIM)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
```

fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 29: Not Installed (OPM2)(LISTA)

```
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter dirty indicator: 0x00000000
Performance filters: 0
Port Mirror filters: 0 (0x0)
```

FIELD DATA

Shadowed fields:

```
fldoffset[0] = 0x00, fldmask[0] = 0x00, fldvalue_dyna[0]: 0x00 0x00
0x00 0x00
fldcontrol[0].inuse = 0x0  fldcontrol[0].refcnt = 0x00 0x00 0x00
0x00
fldoffset[1] = 0x00, fldmask[1] = 0x00, fldvalue_dyna[1]: 0x00 0x00
0x00 0x00
fldcontrol[1].inuse = 0x0  fldcontrol[1].refcnt = 0x00 0x00 0x00
0x00
fldoffset[2] = 0x00, fldmask[2] = 0x00, fldvalue_dyna[2]: 0x00 0x00
0x00 0x00
fldcontrol[2].inuse = 0x0  fldcontrol[2].refcnt = 0x00 0x00 0x00
0x00
fldoffset[3] = 0x00, fldmask[3] = 0x00, fldvalue_dyna[3]: 0x00 0x00
0x00 0x00
fldcontrol[3].inuse = 0x0  fldcontrol[3].refcnt = 0x00 0x00 0x00
0x00
fldoffset[4] = 0x00, fldmask[4] = 0x00, fldvalue_dyna[4]: 0x00 0x00
0x00 0x00
fldcontrol[4].inuse = 0x0  fldcontrol[4].refcnt = 0x00 0x00 0x00
0x00
fldoffset[5] = 0x00, fldmask[5] = 0x00, fldvalue_dyna[5]: 0x00 0x00
0x00 0x00
fldcontrol[5].inuse = 0x0  fldcontrol[5].refcnt = 0x00 0x00 0x00
0x00
fldoffset[6] = 0x00, fldmask[6] = 0x00, fldvalue_dyna[6]: 0x00 0x00
0x00 0x00
fldcontrol[6].inuse = 0x0  fldcontrol[6].refcnt = 0x00 0x00 0x00
0x00
fldoffset[7] = 0x00, fldmask[7] = 0x00, fldvalue_dyna[7]: 0x00 0x00
0x00 0x00
fldcontrol[7].inuse = 0x0  fldcontrol[7].refcnt = 0x00 0x00 0x00
0x00
```

```
fldoffset[8] = 0x00, fldmask[8] = 0x00, fldvalue_dyna[8]:0x00 0x00
0x00 0x00
fldcontrol[8].inuse = 0x0 fldcontrol[8].refcnt = 0x00 0x00 0x00
0x00
fldoffset[9] = 0x00, fldmask[9] = 0x00, fldvalue_dyna[9]:0x00 0x00
0x00 0x00
fldcontrol[9].inuse = 0x0 fldcontrol[9].refcnt = 0x00 0x00 0x00
0x00
fldoffset[10] = 0x00, fldmask[10] = 0x00, fldvalue_dyna[10]:0x00 0x00
0x00 0x00
fldcontrol[10].inuse = 0x0 fldcontrol[10].refcnt = 0x00 0x00 0x00
0x00
fldoffset[11] = 0x00, fldmask[11] = 0x00, fldvalue_dyna[11]:0x00 0x00
0x00 0x00
fldcontrol[11].inuse = 0x0 fldcontrol[11].refcnt = 0x00 0x00 0x00
0x00
fldoffset[12] = 0x00, fldmask[12] = 0x00, fldvalue_dyna[12]:0x00 0x00
0x00 0x00
fldcontrol[12].inuse = 0x0 fldcontrol[12].refcnt = 0x00 0x00 0x00
0x00
fldoffset[13] = 0x00, fldmask[13] = 0x00, fldvalue_dyna[13]:0x00 0x00
0x00 0x00
fldcontrol[13].inuse = 0x0 fldcontrol[13].refcnt = 0x00 0x00 0x00
0x00
fldoffset[14] = 0x00, fldmask[14] = 0x00, fldvalue_dyna[14]:0x00 0x00
0x00 0x00
fldcontrol[14].inuse = 0x0 fldcontrol[14].refcnt = 0x00 0x00 0x00
0x00
fldoffset[15] = 0x00, fldmask[15] = 0x00, fldvalue_dyna[15]:0x00 0x00
0x00 0x00
fldcontrol[15].inuse = 0x0 fldcontrol[15].refcnt = 0x00 0x00 0x00
0x00
fldoffset[16] = 0x00, fldmask[16] = 0x00, fldvalue_dyna[16]:0x00 0x00
0x00 0x00
fldcontrol[16].inuse = 0x0 fldcontrol[16].refcnt = 0x00 0x00 0x00
0x00
fldoffset[17] = 0x00, fldmask[17] = 0x00, fldvalue_dyna[17]:0x00 0x00
0x00 0x00
fldcontrol[17].inuse = 0x0 fldcontrol[17].refcnt = 0x00 0x00 0x00
0x00
fldoffset[18] = 0x00, fldmask[18] = 0x00, fldvalue_dyna[18]:0x00 0x00
0x00 0x00
fldcontrol[18].inuse = 0x0 fldcontrol[18].refcnt = 0x00 0x00 0x00
0x00
fldoffset[19] = 0x00, fldmask[19] = 0x00, fldvalue_dyna[19]:0x00 0x00
0x00 0x00
fldcontrol[19].inuse = 0x0 fldcontrol[19].refcnt = 0x00 0x00 0x00
0x00
```

Real fields:

```
fldoffset RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000
```

```
fldmask RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
```

0x00000000
fld value4 RAM:
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000

Field dirty indicator: 0x00000000

FDB reference count fdb: 0 [0 0 0 0]
FDB reference count fdb: 1 [0 0 0 0]
FDB reference count fdb: 2 [0 0 0 0]
FDB reference count fdb: 3 [0 0 0 0]
FDB reference count fdb: 4 [0 0 0 0]
FDB reference count fdb: 5 [0 0 0 0]
FDB reference count fdb: 6 [0 0 0 0]
FDB reference count fdb: 7 [0 0 0 0]
FDB reference count fdb: 8 [0 0 0 0]
FDB reference count fdb: 9 [0 0 0 0]
FDB reference count fdb: 10 [0 0 0 0]
FDB reference count fdb: 11 [0 0 0 0]
FDB reference count fdb: 12 [0 0 0 0]
FDB reference count fdb: 13 [0 0 0 0]
FDB reference count fdb: 14 [0 0 0 0]
FDB reference count fdb: 15 [0 0 0 0]
FDB reference count fdb: 16 [0 0 0 0]
FDB reference count fdb: 17 [0 0 0 0]
FDB reference count fdb: 18 [0 0 0 0]
FDB reference count fdb: 19 [0 0 0 0]

Filter counters:

Filter counter 0: 0 (MIRROR1)
Filter counter 1: 0 (MIRROR2)
Filter counter 2: 0 (MIRROR3)
Filter counter 3: 0 (MIRROR4)
Filter counter 4: 0 (AEPORT_NON_MIRR_DROP)
Filter counter 5: 0 (ZONING TRAP)
Filter counter 6: 0 (FCR_EXPORT_DC)
Filter counter 7: 0 (TIN TRAP)

Filter counter 8: 0 (FICON CUP)
Filter counter 9: 0 (FICON CUP DST)
Filter counter 10: 0 (WELL KNOWN ADDR)
Filter counter 11: 0 (SIM)
Filter counter 12: 0 (UNUSED)
Filter counter 13: 0 (UNUSED)
Filter counter 14: 0 (UNUSED)
Filter counter 15: 0 (UNUSED)
Filter counter 16: 0 (PERF1)
Filter counter 17: 0 (PERF2)
Filter counter 18: 0 (PERF3)
Filter counter 19: 0 (PERF4)
Filter counter 20: 0 (PERF5)
Filter counter 21: 0 (PERF6)
Filter counter 22: 0 (PERF7)
Filter counter 23: 0 (PERF8)
Filter counter 24: 0 (PERF9)
Filter counter 25: 0 (PERF10)
Filter counter 26: 0 (PERF11)
Filter counter 27: 0 (PERF12)
Filter counter 28: 0 (OPM1)
Filter counter 29: 0 (OPM2)
Filter counter 30: 0 (IPM1)
Filter counter 31: 0 (IPM2)

ACL DATA

Logical port 13: Hard Zoning disabled, Soft Zoning disabled
Zone type: WWN Zoning
Frames with hard zone miss: 0

*** Please use filterportshow on user port 56 to display ACL hash
tables and Mirroring resources of thischip.
***We show this data only for the first physical port which is an
external port.

portFcPortCmdShow --slot 0 55 3
doing portFcPortCmdShow: arg1 = 3, arg2 = -2

portshow 55
portDisableReason: None
portCFlags: 0x0
portFlags: 0x4021 PRESENT U_PORT DISABLED LED
LocalSwcFlags: 0x0
portType: 26.0
POD Port: Need license to enable the port
portState: 2 Offline
Protocol: FC
portPhys: 2 No_Module portScn: 2 Offline
port generation number: 0
state transition count: 0

portId: 013700
portIfId: 4302000e

portWwn: 20:37:d8:1f:cc:2c:99:90
portWwn of device(s) connected:
16b Area list:
Distance: normal
portSpeed: N32Gbps

FEC: Inactive
Credit Recovery: Inactive
LE domain: 0
Peer beacon: Off
FC Fastwrite: OFF

| | | | | |
|-------------|---|---------------|---|-------|
| Interrupts: | 0 | Link_failure: | 0 | Frjt: |
| 0 | | | | |
| Unknown: | 0 | Loss_of_sync: | 0 | Fbsy: |
| 0 | | | | |
| Lli: | 0 | Loss_of_sig: | 0 | |
| Proc_rqrd: | 0 | Protocol_err: | 0 | |
| Timed_out: | 0 | Invalid_word: | 0 | |
| Tx_unavail: | 0 | Invalid_crc: | 0 | |
| Delim_err: | 0 | Address_err: | 0 | |
| Lr_in: | 0 | 0ls_in: | 0 | |
| Lr_out: | 0 | 0ls_out: | 0 | |

portloginshow 55

| Type | PID | World Wide Name | credit | df_sz | cos |
|-------|-----|-----------------|--------|-------|-----|
| ===== | | | | | |

portloginshow 55 -history

| Type | PID | World Wide Name | logout time |
|-------|-----|-----------------|-------------|
| ===== | | | |

portregshow 55

LED registers

=====

| | | | |
|-------------|---------------|----------|-------------|
| 0x81c72000: | c4_led_status | 00000000 | 0x81c72004: |
| | c4_led_ctl | 00000000 | |

FPL registers

=====

| | | | |
|-------------|-----------------------|----------|-------------|
| 0x81c70200: | fpl_port_config | 23490000 | |
| 0x81c7020c: | fpl_port_id_ctl | 00000000 | 0x81c70210: |
| | fpl_port_id_addr | 00013700 | |
| 0x81c70214: | fpl_port_speed | 00000004 | 0x81c7021c: |
| | fpl_lli_ctl | 00000903 | |
| 0x81c70228: | fpl_lli_os_ctl | bc95b5b5 | 0x81c7022c: |
| | fpl_lli_send_word | bc95b5b5 | |
| 0x81c70230: | fpl_lli_mark_rx | 00000000 | 0x81c70234: |
| | fpl_lli_rnd_trip_time | 00000000 | |
| 0x81c70238: | fpl_lli_ns_status | 80070007 | 0x81c7023c: |
| | fpl_lli_intr_status | 80070007 | |

| | | |
|---------------------------------|----------|-------------|
| 0x81c70244: fpl_lli_def | 00000000 | 0x81c70254: |
| fpl_lli_intr_enable_clr | 00100000 | |
| 0x81c70258: fpl_err_intr_status | 00000000 | 0x81c70260: |
| fpl_err_intr_enable_clr | 00000000 | |
| 0x81c70268: fpl_err_first_error | 00000000 | 0x81c7026c: |
| fpl_speed_neg_ctl | 00000000 | |
| 0x81c70270: fpl_speed_neg_stat | 00000000 | 0x81c70274: |
| fpl_softasn_ctl | 0000000f | |
| 0x81c70278: fpl_link_init_ctl | 00000000 | 0x81c7027c: |
| fpl_link_init_stat | 00000000 | |
| 0x81c70280: fpl_aec_ctl | 00051060 | 0x81c70284: |
| fpl_aec_ctl2 | 04009f60 | |
| 0x81c70288: fpl_pcs_ctl | 00000160 | 0x81c7028c: |
| fpl_fec_ctl | 00000441 | |
| 0x81c70290: fpl_fec_cor | 00000000 | 0x81c70294: |
| fpl_fec_uncor | 00000000 | |
| 0x81c70298: fpl_hss_link_ctl | 0031f040 | 0x81c7029c: |
| fpl_afifo_link_ctl | 00000a86 | |
| 0x81c702a0: fpl_echo_lb_ctl | 0000028c | 0x81c702a4: |
| fpl_scratch | 00000121 | |
| 0x81c702a8: fpl_debug | 00030005 | 0x81c702ac: |
| fpl_misc_debug | 00001800 | |
| 0x00000000: SW_shadow_reg | 00000000 | 0x00000000: |
| SW_c4_phyp->cfgptr | 00030000 | |

per-fpg (per octet) registers

=====

| | | |
|-------------------------------------|----------|-------------|
| 0x8180b82c: fpg_serdes_ctla0 | 81a37be7 | 0x8180b830: |
| fpg_serdes_ctla1 | 81a37be7 | |
| 0x8180b834: fpg_serdes_ctlb0 | 81a1c3c3 | 0x8180b838: |
| fpg_serdes_ctlb1 | 81a1c3c3 | |
| 0x8180b83c: fpg_serdes_xgmii_1ms | 00067c28 | 0x8180b840: |
| fpg_serdes_regtimctl | 40e47946 | |
| 0x8180b844: fpg_serdes_asnrsttimctl | 00000102 | |

HSS PLL registers

=====

| | | |
|--|----------|-------------|
| 0x8180b400: 00_hssplla_vco_coarse_cal0 | 00000000 | 0x8180b404: |
| 01_hssplla_vco_coarse_cal1 | 00000014 | |
| 0x8180b408: 02_hssplla_vco_coarse_cal2 | 00000000 | 0x8180b40c: |
| 03_hssplla_vco_coarse_cal3 | 00000000 | |
| 0x8180b410: 04_hssplla_vco_coarse_cal4 | 00000000 | 0x8180b424: |
| 09_hssplla_power_ctl | 00000000 | |
| 0x8180b428: 0A_hssplla_charge_pump_ctl | 00000004 | 0x8180b438: |
| 0E_hssplla_pll_misc_ctl | 00000000 | |
| 0x8180b43c: 0F_hssplla_pclk_ctl | 000000f8 | 0x8180b440: |
| 10_hssplla_eyem_intv_ctl | 00000000 | |
| 0x8180b444: 11_hssplla_eyem_intv_lim1 | 00000000 | 0x8180b448: |
| 12_hssplla_eyem_intv_lim2 | 00000000 | |
| 0x8180b44c: 13_hssplla_eyem_intv_lim3 | 00000000 | 0x8180b450: |
| 14_hssplla_eyem_intv_lim4 | 00000000 | |
| 0x8180b4f0: 3C_hssplla_macro_tst_ctl4 | 00000000 | 0x8180b4f4: |
| 3D_hssplla_macro_tst_ctl3 | 00000000 | |
| 0x8180b4f8: 3E_hssplla_macro_tst_ctl2 | 00000000 | 0x8180b4fc: |

| | | | |
|--|----------|-------------|--|
| 3F_hssplla_macro_tst_ctl1 | 00000000 | | |
| 0x8180b500: 00_hsspllb_vco_coarse_cal0 | 0000000a | 0x8180b504: | |
| 01_hsspllb_vco_coarse_cal1 | 00000014 | | |
| 0x8180b508: 02_hsspllb_vco_coarse_cal2 | 00000000 | 0x8180b50c: | |
| 03_hsspllb_vco_coarse_cal3 | 00000000 | | |
| 0x8180b510: 04_hsspllb_vco_coarse_cal4 | 00000000 | 0x8180b524: | |
| 09_hsspllb_power_ctl | 00000000 | | |
| 0x8180b528: 0A_hsspllb_charge_pump_ctl | 00000004 | 0x8180b538: | |
| 0E_hsspllb_pll_misc_ctl | 00000000 | | |
| 0x8180b53c: 0F_hsspllb_pclk_ctl | 000000f8 | 0x8180b540: | |
| 10_hsspllb_eyem_intv_ctl | 00000000 | | |
| 0x8180b544: 11_hsspllb_eyem_intv_lim1 | 00000000 | 0x8180b548: | |
| 12_hsspllb_eyem_intv_lim2 | 00000000 | | |
| 0x8180b54c: 13_hsspllb_eyem_intv_lim3 | 00000000 | 0x8180b550: | |
| 14_hsspllb_eyem_intv_lim4 | 00000000 | | |
| 0x8180b5f0: 3C_hsspllb_macro_tst_ctl4 | 00000000 | 0x8180b5f4: | |
| 3D_hsspllb_macro_tst_ctl3 | 00000000 | | |
| 0x8180b5f8: 3E_hsspllb_macro_tst_ctl2 | 00000000 | 0x8180b5fc: | |
| 3F_hsspllb_macro_tst_ctl1 | 00000000 | | |

HSS TX registers

=====

| | | | |
|--|----------|-------------|--|
| 0x8180a400: 00_hsstx_cfg_mode_PHY | 00009f48 | 0x8180a404: | |
| 01_hsstx_test_ctl | 00000000 | | |
| 0x8180a408: 02_hsstx_coeff_ctl_INV | 00000000 | 0x8180a40c: | |
| 03_hsstx_drv_mode_ctl | 00000000 | | |
| 0x8180a410: 04_hsstx_drv_ovrd_ctl | 00000010 | 0x8180a414: | |
| 05_hsstx_dclk_align_ovrd | 00000080 | | |
| 0x8180a418: 06_hsstx_imp_cal_ovrd | 00000c0c | 0x8180a41c: | |
| 07_hsstx_dclk_drift_tol | 00000004 | | |
| 0x8180a420: 08_hsstx_tap0_coeff_TUNE | 00000000 | 0x8180a424: | |
| 09_hsstx_tap1_coeff_TUNE | 00000003 | | |
| 0x8180a428: 0A_hsstx_tap2_coeff_TUNE | 00000018 | 0x8180a42c: | |
| 0B_hsstx_tap3_coeff_TUNE | 0000000d | | |
| 0x8180a434: 0D_hsstx_pol_INV | 0000000a | 0x8180a438: | |
| 0E_hsstx_ae_cmd | 00000000 | | |
| 0x8180a43c: 0F_hsstx_ae_stat | 00000000 | 0x8180a440: | |
| 10_hsstx_ae_tap0_TUNE | 00000000 | | |
| 0x8180a444: 11_hsstx_ae_tap1_TUNE | 00000000 | 0x8180a448: | |
| 12_hsstx_ae_tap2_TUNE | 00000028 | | |
| 0x8180a44c: 13_hsstx_ae_tap3_TUNE | 00000000 | 0x8180a454: | |
| 15_hsstx_app_tune | 0000120e | | |
| 0x8180a458: 16_hsstx_analog_diag | 00000000 | 0x8180a460: | |
| 18_hsstx_4x_seg_app | 0000aafa | | |
| 0x8180a464: 19_hsstx_2x_seg_app | 00000000 | 0x8180a468: | |
| 1A_hsstx_1x_seg_app | 0000ff5d | | |
| 0x8180a46c: 1B_hsstx_seg_4x_term_app | 00000000 | 0x8180a470: | |
| 1C_hsstx_seg_2x1x_term_app | 00000f00 | | |
| 0x8180a474: 1D_hsstx_tap_sign_app | 0000000a | 0x8180a478: | |
| 1E_hsstx_ext_addr_data | 00000001 | | |
| 0x8180a47c: 1F_hsstx_ext_addr_addr | 00000000 | 0x8180a480: | |
| 20_hsstx_pat_buf_bytes_1_0 | 00000000 | | |
| 0x8180a484: 21_hsstx_pat_buf_bytes_3_2 | 00000000 | 0x8180a488: | |
| 22_hsstx_pat_buf_bytes_5_4 | 00000000 | | |

| | | |
|---|----------|-------------|
| 0x8180a48c: 23_hsstx_pat_buf_bytes_7_6 | 00000000 | 0x8180a49c: |
| 27_hsstx_8023az_ctl | 00000000 | |
| 0x8180a4a0: 28_hsstx_dcc_ctl | 000060c0 | 0x8180a4a4: |
| 29_hsstx_dcc_ovrd | 00001000 | |
| 0x8180a4a8: 2A_hsstx_dcc_app | 00000000 | 0x8180a4ac: |
| 2B_hsstx_dcc_timeout | 0000ffff | |
| 0x8180a4c0: 30_hsstx_tap_sign_ovrd | 00000000 | 0x8180a4c8: |
| 32_hsstx_seg_4x_ovrd | 00000000 | |
| 0x8180a4cc: 33_hsstx_seg_2x_ovrd | 00000000 | 0x8180a4d0: |
| 34_hsstx_seg_1x_ovrd | 00000000 | |
| 0x8180a4d8: 36_hsstx_tap_seg_4x_term_ovrd | 00000000 | 0x8180a4dc: |
| 37_hsstx_tap_seg_2x_term_ovrd | 00000000 | |
| 0x8180a4e0: 38_hsstx_tap_seg_1x_term_ovrd | 00000000 | 0x8180a4ec: |
| 3B_hsstx_mac_test_ctl5 | 00000000 | |
| 0x8180a4f0: 3C_hsstx_mac_test_ctl4 | 00000000 | 0x8180a4f4: |
| 3D_hsstx_mac_test_ctl3 | 00000000 | |
| 0x8180a4f8: 3E_hsstx_mac_test_ctl2 | 00000000 | 0x8180a4fc: |
| 3F_hsstx_mac_test_ctl1 | 000000c6 | |

HSS RX registers

=====

| | | |
|---|----------|-------------|
| 0x8180a600: 00_hssrx_cfg_mode_PHY | 00009e78 | 0x8180a604: |
| 01_hssrx_test_ctl | 00000000 | |
| 0x8180a608: 02_hssrx_phs_rot_ctl | 0000cb80 | 0x8180a60c: |
| 03_hssrx_phs_rot_ofs_ctl | 00000610 | |
| 0x8180a610: 04_hssrx_phs_rot_posn1 | 00000c2b | 0x8180a614: |
| 05_hssrx_phs_rot_posn2 | 0000001a | |
| 0x8180a618: 06_hssrx_phs_rot_sta_ofs1 | 00000102 | 0x8180a61c: |
| 07_hssrx_phs_rot_sta_ofs2 | 00000001 | |
| 0x8180a620: 08_hssrx_dfe_ctl_PHY | 00002002 | 0x8180a624: |
| 09_hssrx_dfe_smpl_snap1 | 00000000 | |
| 0x8180a628: 0A_hssrx_dfe_smpl_snap2 | 00008000 | 0x8180a62c: |
| 0B_hssrx_vga_ctl1 | 00004004 | |
| 0x8180a630: 0C_hssrx_vga_ctl2 | 00007ba0 | 0x8180a634: |
| 0D_hssrx_vga_ctl3 | 000009e4 | |
| 0x8180a638: 0E_hssrx_pwr_mgmt_ctl | 0000001f | 0x8180a63c: |
| 0F_hssrx_iqamp_ctl1 | 00000019 | |
| 0x8180a640: 10_hssrx_iqamp_ctl2 | 00000004 | 0x8180a644: |
| 11_hssrx_dacap_dacan_sel | 00000003 | |
| 0x8180a648: 12_hssrx_dacap_dacan | 0000fefc | 0x8180a64c: |
| 13_hssrx_daca_min | 00000000 | |
| 0x8180a650: 14_hssrx_adac_ctl | 00000000 | 0x8180a654: |
| 15_hssrx_ac_cp_ctl | 000031c3 | |
| 0x8180a658: 16_hssrx_ac_cp_val | 00008055 | 0x8180a65c: |
| 17_hssrx_dfe_h1h2h3_lcl_off_ch | 00000014 | |
| 0x8180a660: 18_hssrx_dfe_h1h2h3_lcl_off_val | 00000000 | 0x8180a664: |
| 19_hssrx_peaked_intg | 000000ff | |
| 0x8180a668: 1A_hssrx_cdr_analog_sw | 0000ce00 | 0x8180a66c: |
| 1B_hssrx_peaking_amp_init_c_PHY | 00000000 | |
| 0x8180a670: 1C_hssrx_dac_dpc | 00000040 | 0x8180a674: |
| 1D_hssrx_ddc | 00000000 | |
| 0x8180a678: 1E_hssrx_int_stat_PHY | 00000c0f | 0x8180a67c: |
| 1F_hssrx_dfe_func_ctl1_PHY | 0000ffff | |
| 0x8180a680: 20_hssrx_dfe_func_ctl2_INV | 00007ebf | 0x8180a684: |

| | | | |
|--|----------|-----------|-------------|
| 21_hssrx_ofs_ch_dcc_qcc_idx | 00002000 | | |
| 0x8180a688: 22_hssrx_dfe_ofs_val | | 00007e01 | 0x8180a68c: |
| 23_hssrx_h_coeff_bist | 00000401 | | |
| 0x8180a690: 24_hssrx_ac_cap_bist | | 00000031 | 0x8180a694: |
| 25_hssrx_max_gain_path_idx_res | 00007800 | | |
| 0x8180a698: 26_hssrx_loff_ctl | | 00000055 | 0x8180a69c: |
| 27_hssrx_sigdet_ctl | 00004a80 | | |
| 0x8180a6a0: 28_hssrx_ana_ctl_sw | | 00000000 | 0x8180a6a4: |
| 29_hssrx_intg_dac_ofs | 0000ddd9 | | |
| 0x8180a6a8: 2A_hssrx_eye_ctl | | 00000000 | 0x8180a6ac: |
| 2B_hssrx_eye_met | 00000004 | | |
| 0x8180a6b0: 2C_hssrx_eye_met_err_cnt | | 00000000 | 0x8180a6b4: |
| 2D_hssrx_eye_met_pdf_eyec | 00000000 | | |
| 0x8180a6b8: 2E_hssrx_eye_met_pat_len | | 0000007f | 0x8180a6bc: |
| 2F_hssrx_dfe_func_ctl3 | 0000dfff | | |
| 0x8180a6c0: 30_hssrx_dfe_tap_ctl_idx_ptr | | 00000008 | 0x8180a6c4: |
| 31_hssrx_dfe_tap | 00003030 | | |
| 0x8180a6c8: 32_hssrx_lte_ctl_TUNE | | 00001601 | 0x8180a6e4: |
| 39_hssrx_int_stat2 | 000041ff | | |
| 0x8180a6e8: 3A_hssrx_ac_cpl_cur_src_adj | | 00000042 | 0x8180a6ec: |
| 3B_hssrx_dcd_ctl | 00007c00 | | |
| 0x8180a6f0: 3C_hssrx_dcc_ctl | | 00000d44 | 0x8180a6f4: |
| 3D_hssrx_qcc_ctl | 00006991 | | |
| 0x8180a6f8: 3E_hssrx_mac_test_ctl2 | | 00000000 | 0x8180a6fc: |
| 3F_hssrx_mac_test_ctl1 | 00000000 | | |
| 0x8180a648: 12_hssrx_dacap_dacan[02] | | 00fd fefd | |
| 0x8180a660: 18_hssrx_dfe_h1h2h3_lcl_off_va[00] | | 0000 0000 | 0000 |
| 0000 0000 0000 0000 0000 | | | |
| 0x8180a660: 18_hssrx_dfe_h1h2h3_lcl_off_va[08] | | 0000 0000 | 0000 |
| 0000 0000 0000 0000 0000 | | | |
| 0x8180a660: 18_hssrx_dfe_h1h2h3_lcl_off_va[16] | | 0000 0000 | 0000 |
| 0000 0000 | | | |
| 0x8180a688: 22_hssrx_dfe_ofs_val[00][00] | | 7e01 0000 | 7d7f |
| 0000 0705 7f00 | | | |
| 0x8180a688: 22_hssrx_dfe_ofs_val[03][00] | | 7f7b 0000 | 027f |
| 7f00 0102 0000 | | | |
| 0x8180a688: 22_hssrx_dfe_ofs_val[06][00] | | 0107 0000 | 0602 |
| 0000 7f04 0100 | | | |
| 0x8180a688: 22_hssrx_dfe_ofs_val[09][00] | | 0000 0000 | 097b |
| 7f00 0579 7f00 | | | |
| 0x8180a688: 22_hssrx_dfe_ofs_val[12][00] | | 7d7b 0000 | 7d01 |
| 0000 017b 0000 | | | |
| 0x8180a688: 22_hssrx_dfe_ofs_val[15][00] | | 7a7d 0000 | 0905 |
| 7f7f 7f7d 0000 | | | |
| 0x8180a688: 22_hssrx_dfe_ofs_val[18][00] | | 7b7d 0000 | 7f7d |
| 0000 0002 0000 | | | |
| 0x8180a688: 22_hssrx_dfe_ofs_val[21][00] | | 0002 0000 | 0002 |
| 0000 0002 0000 | | | |
| 0x8180a688: 22_hssrx_dfe_ofs_val[24][00] | | 0101 0000 | 0404 |
| 0000 037d 0000 | | | |
| 0x8180a694: 25_hssrx_max_gain_path_idx_res[00] | | 006b 0853 | 1110 |
| 18a5 20ef 28a5 3089 3800 | | | |
| 0x8180a694: 25_hssrx_max_gain_path_idx_res[08] | | 40bf 488a | 5076 |
| 5800 6040 6800 70f9 7800 | | | |

```

0x8180a6c4: 31_hssrx_dfe_tap[00]          fffe 8080  0000
0000  0030 0030  3030 3030
0x8180a6c4: 31_hssrx_dfe_tap[08]          3030 3030  3030
0000
0x8180a6e8: 3A_hssrx_ac_cpl_cur_src_adj[00]    0042 0042  0042
0042
0x8180a6ec: 3B_hssrx_dcd_ctl[00]              7c00 5c00  7c82
5c00  7c00
0x8180a6f0: 3C_hssrx_dcc_ctl[00]              0d44 0d00  0d42
0d43
0x8180a6f4: 3D_hssrx_qcc_ctl[00]              6986 6991

```

xfipcs, fec, aec, & aet registers

=====

```

0x81c70400: xfipcs_reg          [00] 00002040 00000080 00000000
00000000  00000001 00000008 00000000 00000000
0x81c70420: xfipcs_reg          [08] 00008c01 00000000 00000000
00000000  00000000 00000000 00000000 00000000
0x81c70440: xfipcs_reg          [16] 00000000 00000000 00000000
00000000  00000040 00000000 00000000 00000000
0x81c70460: xfipcs_reg          [24] 00000000 00000000 00000000
00000000  00000000 00000000 00000000 00000000
0x81c70480: xfipcs_reg          [32] 00000004 00000000 00000000
00000000  00000000 00000000 00000000 00000000
0x81c70620: fec_32g_128g_reg   [08] 00000000 00000000 00000000
00000000  00000000 00000000 00000000
0x81c70648: fec_32g_128g_reg   [18] 00000000 00000000 00000000
00000000  00000000 00000000 00000000 00000000
0x81c70a00: aec_reg             [00] 00000000 00000000 00000000
00000000  00000000 00000000 00000000 00000000
0x81c70c00: aet_reg             [00] 00000000 00000000 00000000
00000000  00000000

```

bbc registers

=====

```

0x81c71800: bbc_trc             0  0  0  0  0  0  0
0
0x81c71840: bbc_trc             0  0  0  0  0  0  0
0
0x81c71880: bbc_trc             0  0  0  0  0  0  0
0
0x81c718c0: bbc_trc             0  0  0  0  0  0  0
0
0x81c71900: bbc_trc             0  0  0  0  0  0  0
0
0x81c71804: bbc_mbc             0  0  0  0  0  0  0
0
0x81c71844: bbc_mbc             0  0  0  0  0  0  0
0
0x81c71884: bbc_mbc             0  0  0  0  0  0  0
0
0x81c718c4: bbc_mbc             0  0  0  0  0  0  0
0
0x81c71904: bbc_mbc             0  0  0  0  0  0  0

```

| | | | | | | | |
|-------------------------------------|----------|---|---|---|---|----------------------|---|
| 0 | | | | | | | |
| 0x81c71a00: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c71a20: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c71a40: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c71a60: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c71a80: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c71c00: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c71c20: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c71c40: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c71c60: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c71c80: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c71d00: bbc_fbpc | 00000000 | | | | | 0x81c71d04: bbc_csc | |
| 00000000 | | | | | | | |
| 0x81c71d08: bbc_rcc_inc | 00000000 | | | | | 0x81c71d0c: | |
| bbc_rqc_inc | 00000000 | | | | | | |
| 0x81c71d10: bbc_fbpc_inc | 00000000 | | | | | 0x81c71d14: | |
| bbc_tmc_inc | 00000000 | | | | | | |
| 0x81c71d18: bbc_threshold | 00080100 | | | | | 0x81c71d1c: | |
| bbc_counter_clr | 00000000 | | | | | | |
| 0x81c71d20: bbc_debug_en | 00000000 | | | | | 0x81c71d24: bbc_ctrl | |
| 00200020 | | | | | | | |
| 0x81c71d28: bbc_rqc_rcc_thresh | 00000055 | | | | | 0x81c71d34: | |
| bbc_bb_sc_n | 00000000 | | | | | | |
| 0x81c71d38: bbc_crd_reco_debug | 00000000 | | | | | 0x81c71d3c: | |
| bbc_crd_reco_debug_data | 00000000 | | | | | | |
| 0x81c71d40: bbc_multi_frm_loss_cnt | 00000000 | | | | | 0x81c71d44: | |
| bbc_multi_rdy_loss_cnt | 00000000 | | | | | | |
| 0x81c71d48: bbc_1frm_loss_recov_cnt | 00000000 | | | | | 0x81c71d4c: | |
| bbc_1rdy_loss_recov_cnt | 00000000 | | | | | | |
| 0x81c71d58: bbc_int_status | 00000000 | | | | | 0x81c71d5c: | |
| bbc_int_set | 00000000 | | | | | | |
| 0x81c71d60: bbc_int_first | 00000000 | | | | | 0x81c71d64: | |
| bbc_frm_rdy_rx_err_addr | 00000000 | | | | | | |
| 0x81c71d68: bbc_frm_rdy_tx_err_addr | 00000000 | | | | | 0x81c71d6c: | |
| bbc_trc_mbc_err_addr | 00000000 | | | | | | |
| 0x81c71d70: bbc_frm_rdy_rx_dbl_ecc | 00000000 | | | | | 0x81c71d74: | |
| bbc_frm_rdy_tx_dbl_ecc | 00000000 | | | | | | |
| 0x81c71d78: bbc_trc_mbc_dbl_ecc | 00000000 | | | | | | |
| 0x81c71d7c: bbc_fsm_status | 00001011 | | | | | 0x81c71d80: | |
| bbc_force_err | 00000000 | | | | | | |
| 0x81c71d84: bbc_crdt_avail0 | ffffffff | | | | | 0x81c71d88: | |
| bbc_crdt_avail1 | 000000ff | | | | | | |
| 0x81c71d8c: bbc_scratch | 00000000 | | | | | | |

FPS registers

=====

| | | |
|--------------------------------|----------|-------------|
| 0x81c70004: fps_er_enc_in | 00000000 | 0x81c70008: |
| fps_er_crc | 00000000 | |
| 0x81c7000c: fps_er_trunc | 00000000 | 0x81c70010: |
| fps_er_toolong | 00000000 | |
| 0x81c70014: fps_er_bad_eof | 00000000 | 0x81c70018: |
| fps_er_enc_out | 00000000 | |
| 0x81c7001c: fps_er_bad_os | 00000000 | 0x81c70020: |
| fps_er_flush | 00000000 | |
| 0x81c70024: fps_er_ifg | 00000000 | 0x81c70038: |
| fps_er_crc_good_eof | 00000000 | |
| 0x81c7003c: fps_inv_arb | 00000000 | 0x81c70040: |
| fps_slow_sts_status | 00000000 | |
| 0x81c70044: fps_tx_frm_cnt | 00000000 | 0x81c70048: |
| fps_rx_frm_cnt | 00000000 | |
| 0x81c70050: fps_tx_word_cnt_hi | 00000000 | 0x81c7004c: |
| fps_tx_word_cnt_lo | 00000000 | |
| 0x81c70058: fps_rx_word_cnt_hi | 00000000 | 0x81c70054: |
| fps_rx_word_cnt_lo | 00000000 | |

BAL registers

=====

| | | |
|---------------------------------|----------|-------------|
| 0x81c77000: bal_desired_buf | 00000000 | 0x81c77004: |
| bal_alloc_buf | 00000000 | |
| 0x81c77008: bal_busy_buf | 00000000 | 0x81c7700c: |
| bal_usable_buf | 00000000 | |
| 0x81c77010: bal_max_bor_buf | 00000000 | |
| 0x81c77014: bal_busy_buf_thresh | 00000002 | |

TXQ registers

=====

| | | |
|-------------------------------------|------------------------|--|
| 0x81c73004: txq_phys_port_ctl | 00460000 | |
| 0x81c73050: txq_link_skew | 00000000 | |
| 0x81c73068: txq_cr_lk_dttm_intr_sts | [00] 00000000 00000000 | |
| 0x81c73070: txq_cr_lk_dttm_intr_en | [00] 00000000 00000000 | |
| 0x81c73024: txq_disc_frm_trap_cnt | 00000014 | |

FDS registers

=====

| | | |
|------------------------------------|----------|-------------|
| 0x81c74000: fds_rxf_ctl | 00000002 | 0x81c74004: |
| fds_rxf_wait_thresh | 00000909 | |
| 0x81c74018: fds_rxf_first_error | 00000000 | 0x81c7401c: |
| fds_rxf_first_error_info | 00000000 | |
| 0x81c74020: fds_rxf_inout_pkt_cnt | 00000000 | |
| 0x81c74008: fds_rxf_err_int_status | 00000000 | 0x81c74024: |
| fds_rxf_fifo_status | 00888888 | |
| 0x81c75000: fds_txf_ctl | 0000003a | 0x81c75004: |
| fds_txf_wait_ifg_thresh | 00a00106 | |
| 0x81c75008: fds_txf_err_int_status | 00000000 | 0x81c75024: |
| fds_txf_fifo_status | 00088888 | |
| 0x81c7502c: fds_txf_bbc_scs | 00000000 | |

Logical TXQ registers


```

=====
0x81c73000: txq_log_port_ctl          00000002      0x81c73008:
txq_port_status          00000000
0x81c7300c: txq_todo_flags          [00] 00000000 00000000
0x81c73014: txq_spd_match_desc        [00] 00000000 00000000 00000000
00000000
0x81c73024: txq_spd_match_desc        [04] 00000014
0x81c73028: txq_vc_weight          [00] 01010101 01010101 01010101
01010101
0x81c73038: txq_vc_weight          [04] 01010101 01010101 01010101
01010101
0x81c73048: txq_vc_weight          [08] 01010101 00010101
0x81c73054: txq_cong_dttm_ctrl      00000000
0x81c73058: txq_cong_dttm_intr_sts     [00] 00000000 00000000
0x81c73060: txq_cong_dttm_intr_en       [00] 00000000 00000000
0x81c73078: txq_bw_limit_en_reg         [00] 00000000 00000000
0x81c73080: txq_bw_gua_en_reg          [00] 00000000 00000000
0x81c73088: txq_vc_group              [00] 03030300 03030303 03030303
03030303
0x81c73098: txq_vc_group              [04] 03030303 03030303 03030303
03030303
0x81c730a8: txq_vc_group              [08] 03030303 03030303 00000000
00000000
0x81c730b0: txq_bw_thresh_group     [00] 00000000 00000000 00000000
00000000
0x81c730c0: txq_bw_thresh_group     [04] 00000000 00000000 00000000
00000000
0x81c730d0: txq_bw_thresh_group     [08] 00000000 00000000 00000000
00000000
0x81c730e0: txq_bw_thresh_group     [12] 00000000 00000000 00000000
00000000
0x81c730f0: txq_bw_thresh_group     [16] 00000000 00000000 00000000
00000000
0x81c73100: txq_bw_thresh_group     [20] 00000000 00000000 00000000
00000000
0x81c73110: txq_bw_thresh_group     [24] 00000000 00000000 00000000
00000000
0x81c73120: txq_bw_thresh_group     [28] 00000000 00000000 00000000
00000000
0x81c73130: txq_bw_thresh_group     [32] 00000000 00000000 00000000
00000000
0x81c73140: txq_bw_thresh_group     [36] 00000000 00000000 00000000
00000000

```

txq Congestion detection Statistics RAM

```

=====
0x810908c0: vc[0]          00000000      0x810908c4: vc[1]
00000000
0x810908c8: vc[2]          00000000      0x810908cc: vc[3]
00000000
0x810908d0: vc[4]          00000000      0x810908d4: vc[5]
00000000
0x810908d8: vc[6]          00000000      0x810908dc: vc[7]
00000000

```

| | | |
|--------------------|----------|--------------------|
| 0x810908e0: vc[8] | 00000000 | 0x810908e4: vc[9] |
| 00000000 | | |
| 0x810908e8: vc[10] | 00000000 | 0x810908ec: vc[11] |
| 00000000 | | |
| 0x810908f0: vc[12] | 00000000 | 0x810908f4: vc[13] |
| 00000000 | | |
| 0x810908f8: vc[14] | 00000000 | 0x810908fc: vc[15] |
| 00000000 | | |
| 0x81090900: vc[16] | 00000000 | 0x81090904: vc[17] |
| 00000000 | | |
| 0x81090908: vc[18] | 00000000 | 0x8109090c: vc[19] |
| 00000000 | | |
| 0x81090910: vc[20] | 00000000 | 0x81090914: vc[21] |
| 00000000 | | |
| 0x81090918: vc[22] | 00000000 | 0x8109091c: vc[23] |
| 00000000 | | |
| 0x81090920: vc[24] | 00000000 | 0x81090924: vc[25] |
| 00000000 | | |
| 0x81090928: vc[26] | 00000000 | 0x8109092c: vc[27] |
| 00000000 | | |
| 0x81090930: vc[28] | 00000000 | 0x81090934: vc[29] |
| 00000000 | | |
| 0x81090938: vc[30] | 00000000 | 0x8109093c: vc[31] |
| 00000000 | | |
| 0x81090940: vc[32] | 00000000 | 0x81090944: vc[33] |
| 00000000 | | |
| 0x81090948: vc[34] | 00000000 | 0x8109094c: vc[35] |
| 00000000 | | |
| 0x81090950: vc[36] | 00000000 | 0x81090954: vc[37] |
| 00000000 | | |
| 0x81090958: vc[38] | 00000000 | 0x8109095c: vc[39] |
| 00000000 | | |

Logical STS registers

=====

| | | |
|----------------------------------|----------------------------|------------------------------|
| 0x81584b04: sts_ftb_type1_miss | 00000000 | |
| 0x81584b08: sts_ftb_type2_miss | 00000000 | |
| 0x81584b0c: sts_ftb_type6_miss | 00000000 | |
| 0x81584b10: sts_hard_zoning_miss | 00000000 | |
| 0x81584b14: sts_lun_zoning_miss | 00000000 | |
| 0x81584b1c: sts_unroutable | 00000000 | |
| 0x81581b34: sts_rte_cl2 | 00000000 | 0x81581b38: |
| sts_rte_cl3 | 00000000 | 0x81581b3c: sts_rte_link_ctl |
| 00000000 | 0x81584b28: sts_tx_timeout | 00000000 |

Logical STS filter registers

=====

| | | | | |
|-------------------------|------|----------|----------|----------|
| 0x81584a80: stsflt_trig | [00] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584a90: stsflt_trig | [04] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584aa0: stsflt_trig | [08] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |

| | | | | |
|-------------------------|------|----------|----------|----------|
| 0x81584ab0: stsflt_trig | [12] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584ac0: stsflt_trig | [16] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584ad0: stsflt_trig | [20] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584ae0: stsflt_trig | [24] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584af0: stsflt_trig | [28] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584b00: stsflt_trig | [32] | | | |

Logical STS discard registers

=====

| | | |
|------------------------------------|----------|-------------|
| 0x81582458: disc_mcast_wka | 00000000 | 0x8158245c: |
| disc_inv_did | 00000000 | |
| 0x81582460: disc_cl1_cl4 | 00000000 | 0x81582464: |
| disc_sid_chk_fail | 00000000 | |
| 0x81582468: disc_inv_dom_egid_txpt | 00000000 | 0x8158246c: |
| disc_vft_hop_cnt_1 | 00000000 | |
| 0x81582470: disc_classf | 00000000 | 0x81582474: |
| disc_fcp_cdb_inv | 00000000 | |
| 0x81582478: disc_vfid_trap_enabled | 00000000 | 0x8158247c: |
| disc_vfid_hdr_chk_fail | 00000000 | |
| 0x81582480: disc_shim_cksum_fail | 00000000 | 0x81582484: |
| disc_fed_edit_cmd_err | 00000000 | |
| 0x81582488: disc_ftb_vm_mode | 00000000 | 0x8158248c: |
| disc_ftb_agnt2_miss | 00000000 | |
| 0x81582490: disc_ecb_reserved | 00000000 | 0x81582494: |
| disc_ecb_de_pad_err | 00000000 | |
| 0x81582498: disc_ecb_de_tag_err | 00000000 | 0x8158249c: |
| disc_ecb_de_seq_err | 00000000 | |
| 0x815824a0: disc_ecb_err | 00000000 | 0x815824a4: |
| disc_ftb_type4_match | 00000000 | |
| 0x815824a8: disc_fcp_rsp_ftb_type4 | 00000000 | 0x815824ac: |
| disc_ftb_type5_match | 00000000 | |
| 0x815824b0: disc_ftb_type3_match | 00000000 | 0x815824b4: |
| disc_els_ftb_type3 | 00000000 | |
| 0x815824b8: disc_ftb_type1_match | 00000000 | 0x815824bc: |
| disc_els_rsp_ex_port | 00000000 | |
| 0x815824c0: disc_inv_drp_dps | 00000000 | 0x815824c4: |
| disc_did_lookup_miss | 00000000 | |
| 0x815824c8: disc_ftb_type2_match | 00000000 | 0x815824cc: |
| disc_trpd_plogi_pdisc | 00000000 | |
| 0x815824d0: disc_type2_lookup_miss | 00000000 | 0x815824d4: |
| disc_ftb_type6_match | 00000000 | |
| 0x815824d8: disc_els_rep_ex_port | 00000000 | 0x815824dc: |
| disc_els_sid_lkup_bit1 | 00000000 | |
| 0x815824e0: disc_els_sid_lkup_bit0 | 00000000 | 0x815824e4: |
| disc_bls_frm_trap_bit1 | 00000000 | |
| 0x815824e8: disc_ftb_token_err | 00000000 | 0x815824ec: |
| disc_asic_internal_err | 00000000 | |
| 0x815824f0: disc_hard_zone_miss | 00000000 | 0x815824f4: |
| disc_lun_zone_miss | 00000000 | |

```

0x815824f8: discflt_frame_disc      00000000    0x815824fc:
discflt_parity_err      00000000
0x81582500: disc_frame_marked_du      00000000    0x81582504:
disc_frame_marked_to    00000000
0x81582508: disc_lkup_rte_prty_err  00000000

```

portstatsshow 55

```

stat_wtx      0      4-byte words transmitted
stat_wrx      0      4-byte words received
stat_ftx      0      Frames transmitted
stat_frx      0      Frames received
stat_c2_frx   0      Class 2 frames received
stat_c3_frx   0      Class 3 frames received
stat_lc_rx    0      Link control frames
received
stat_mc_rx    0      Multicast frames
received
stat_mc_to    0      Multicast timeouts
stat_mc_tx    0      Multicast frames
transmitted
tim_txcrd_z   0      Time TX Credit Zero
(2.5Us ticks)
tim_txcrd_z_vc 0- 3: 0      0      0      0
tim_txcrd_z_vc 4- 7: 0      0      0      0
tim_txcrd_z_vc 8-11: 0     0      0      0
tim_txcrd_z_vc 12-15: 0    0      0      0
lat_tot_pkt_vc 0- 3: 1      1      1      1
lat_tot_pkt_vc 4- 7: 1      1      1      1
lat_tot_pkt_vc 8-11: 1     1      1      1
lat_tot_pkt_vc 12-15: 1    1      1      1
lat_hi_time_vc 0- 3: 0      0      0      0
lat_hi_time_vc 4- 7: 0      0      0      0
lat_hi_time_vc 8-11: 0     0      0      0
lat_hi_time_vc 12-15: 0    0      0      0
lat_lo_time_vc 0- 3: 1      1      1      1
lat_lo_time_vc 4- 7: 1      1      1      1
lat_lo_time_vc 8-11: 1     1      1      1
lat_lo_time_vc 12-15: 1    1      1      1
max_latency_vc 0- 3: 1      1      1      1
max_latency_vc 4- 7: 1      1      1      1
max_latency_vc 8-11: 1     1      1      1
max_latency_vc 12-15: 1    1      1      1
latency_dma_ts 09-09-2024 UTC Mon 08:47:26      TXQ
Latency DMA TimeStamp
fec_cor_detected 0      Count of blocks that
were corrected by FEC
fec_uncor_detected 0     Count of blocks that
were left uncorrected by FEC
er_enc_in      0      Encoding errors inside
of frames
er_crc         0      Frames with CRC errors
er_trunc       0      Frames shorter than
minimum

```

| | | |
|---|-----------------------------|--------------------------|
| er_toolong maximum | 0 | Frames longer than |
| er_bad_eof frame | 0 | Frames with bad end-of- |
| er_enc_out of frames | 0 | Encoding error outside |
| er_bad_os | 0 | Invalid ordered set |
| er_pcs_blk | 0 | PCS block errors |
| er_rx_c3_timeout discarded due to timeout | 0 | Class 3 receive frames |
| er_tx_c3_timeout discarded due to timeout | 0 | Class 3 transmit frames |
| er_unroutable unroutable | 0 | Frames that are |
| er_unreachable destination | 0 | Frame with unreachable |
| er_other_discard | 0 | Other discards |
| er_type1_miss miss | 0 | frames with FTB type 1 |
| er_type2_miss miss | 0 | frames with FTB type 2 |
| er_type6_miss miss | 0 | frames with FTB type 6 |
| er_zone_miss miss | 0 | frames with hard zoning |
| er_lun_zone_miss miss | 0 | frames with LUN zoning |
| er_crc_good_eof | 0 | Crc error with good eof |
| er_inv_arb | 0 | Invalid ARB |
| er_single_credit_loss on link | 0 | Single vcrdy/frame loss |
| er_multi_credit_loss loss on link | 0 | Multiple vcrdy/frame |
| other_credit_loss credit loss | 0 | Link timeout/complete |
| phy_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | Timestamp of |
| phy_port stats clear | | |
| lgc_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | Timestamp of |
| lgc_port stats clear | | |
| fec_corrected_rate second | 0 | FEC Corrected blocks per |

portstats64show 55

| | | |
|---------------|---|---------------------------------------|
| stat64_wtx | 0 | top_int : 4-byte words transmitted |
| | 0 | bottom_int : 4-byte words transmitted |
| stat64_wrx | 0 | top_int : 4-byte words received |
| | 0 | bottom_int : 4-byte words received |
| stat64_ftx | 0 | top_int : Frames transmitted |
| | 0 | bottom_int : Frames transmitted |
| stat64_frx | 0 | top_int : Frames received |
| | 0 | bottom_int : Frames received |
| stat64_c2_frx | 0 | top_int : Class 2 frames received |
| | 0 | bottom_int : Class 2 frames received |
| stat64_c3_frx | 0 | top_int : Class 3 frames received |

| | | |
|------------------------------|---|--|
| stat64_lc_rx | 0 | bottom_int : Class 3 frames received |
| | 0 | top_int : Link control frames received |
| | 0 | bottom_int : Link control frames |
| received | | |
| stat64_mc_rx | 0 | top_int : Multicast frames received |
| | 0 | bottom_int : Multicast frames received |
| stat64_mc_to | 0 | top_int : Multicast timeouts |
| | 0 | bottom_int : Multicast timeouts |
| stat64_mc_tx | 0 | top_int : Multicast frames transmitted |
| | 0 | bottom_int : Multicast frames |
| transmitted | | |
| tim64_rdy_pri | 0 | top_int : Time R_RDY high priority |
| | 0 | bottom_int : Time R_RDY high priority |
| tim64_txcrd_z | 0 | top_int : Time BB_credit zero |
| | 0 | bottom_int : Time BB_credit zero |
| er64_enc_in | 0 | top_int : Encoding errors inside of |
| frames | 0 | bottom_int : Encoding errors inside of |
| frames | | |
| er64_crc | 0 | top_int : Frames with CRC errors |
| | 0 | bottom_int : Frames with CRC errors |
| er64_trunc | 0 | top_int : Frames shorter than minimum |
| | 0 | bottom_int : Frames shorter than minimum |
| er64_toolong | 0 | top_int : Frames longer than maximum |
| | 0 | bottom_int : Frames longer than maximum |
| er64_bad_eof | 0 | top_int : Frames with bad end-of-frame |
| | 0 | bottom_int : Frames with bad end-of- |
| frame | | |
| er64_enc_out | 0 | top_int : Encoding error outside of |
| frames | 0 | bottom_int : Encoding error outside of |
| frames | | |
| er64_disc_c3 | 0 | top_int : Class 3 frames discarded |
| | 0 | bottom_int : Class 3 frames discarded |
| er64_pcs_blk | 0 | top_int : PCS block errors |
| | 0 | bottom_int : PCS block errors |
| stat64_rateTxFrame | 0 | Tx frame rate (fr/sec) |
| stat64_rateRxFrame | 0 | Rx frame rate (fr/sec) |
| stat64_rateTxPeakFrame | 0 | Tx peak frame rate (fr/sec) |
| stat64_rateRxPeakFrame | 0 | Rx peak frame rate (fr/sec) |
| stat64_rateTxWord | 0 | Tx Word rate (words/sec) |
| stat64_rateRxWord | 0 | Rx Word rate (words/sec) |
| stat64_rateTxPeakWord | 0 | Tx peak Word rate (words/sec) |
| stat64_rateRxPeakWord | 0 | Rx peak Word rate (words/sec) |
| stat64_PRJTFrames | 0 | top_int : Number of PRJT frames |
| returned to this port | 0 | bottom_int : Number of PRJT |
| frames returned to this port | | |
| stat64_PBSYFrames | 0 | top_int : Number of PBSY frames |
| returned to this port | 0 | bottom_int : Number of PBSY |
| frames returned to this port | | |
| stat64_inputBuffersFull | 0 | top_int : Number of occurrences |
| when all input buffers full | | |

```

0 bottom_int : Number of
occurrences when all input buffers full
stat64_rxClass1Frames 0 top_int : Number of class 1
frames received
0 bottom_int : Number of class 1
frames received
stat64_aveTxFrameSize 0 Average Tx Frame size
stat64_aveRxFrameSize 0 Average Rx Frame size
Lr_in 0 top_int
0 bottom_int
Ols_in 0 top_int
0 bottom_int
Lr_out 0 top_int
0 bottom_int
Ols_out 0 top_int
0 bottom_int
Link_failure 0 top_int
0 bottom_int
Invalid_CRC 0 top_int
0 bottom_int
Invalid_word 0 top_int
0 bottom_int
Protocol_err 0 top_int
0 bottom_int
Loss_of_sig 0 top_int
0 bottom_int
Loss_of_sync 0 top_int
0 bottom_int
er_bad_os 0 top_int : Invalid ordered set
0 bottom_int: Invalid ordered set

```

```

portrouteshow 55
port address ID: 0x013700
external unicast routing table:
0: Embedded
255: Embedded
internal unicast routing table:
0: Embedded

```

```
portcamshow 55
```

```

-----
Port  SID used  DID used  SID entries  DID entries
55    0          0         000000      000000
-----

```

```
ptbufshow, ptcreditshow, ptdatashow, ptstatsshow 55
```

```
S:
S:VF Enable: 1
```

```
S:
S:C4 Global Variable:
```

```
S:-----
```

```
-----
S:trace_stop: 0
```

```

S:
S:C4 Phy Data Pointers: c4_phyp = 0xb6ad0000
S:-----
-----
S:tnodep                0xbb83b2a0      pt
    0x4302800e
S:proto_phyp            0xb8808900      phy_cfg
0xb6ad1040
S:c4_chp                0x97e28000      c4_lgcp
0x97f80000
S:c4_phy_regp           0x81c70000      proc_dir
0xb8517f00
S:-----
-----
S:magic_id              0xc4345678      num_port_timer    12
S:prev_if_id            0x4302000e      S:ftx              0
    tov              0
S:initialized           0                port_idx           14
S:ui_idx                55              slot_no
    0
S:blade_idx             14              sw_usr_ports       400
S:unused                0                intr_debounced
    0
S:aec_status            0x0             reason_code
    0
S:debug                 0x00000004      debug_trc_line     0
S:rxbuf_list_head       0xffffffff      rxbuf_list_tail
0xffffffff
S:isAePort              0                port_misc_data
    0
S:num_fault1_rx_disc    0                num_fault2_rx_disc 0
S:p_lli_cause0          0                p_sig_regained     0
S:p_sync_regained       0                enc_out
    0x0
S:cached_fps_status     0                cached_sts_status  0
S:cached_er_crc_good_eof 0
S:cached_er_bad_os      0                cached_er_too_long 0
S:cached_er_trunc       0
cached_tot_er_crc_good_eof 0
S:num_pt_excess_intr    0                num_no_fid         0
S:num_fault1_cnt        0                num_fault2_cnt
    0
S:num_fault_lip         0                num_fault_lli      0
S:num_fault_rx_fifo     0                num_fault_hss      0
S:num_fault_bwait       0                lli_intr_prim
    0
S:num_sw_link_to        0
be_link_err_mon_count   0
S:ecb_enc_enabled       0                ecb_comp_enabled
    0
S:ecb_rsv_enc           0                ecb_rsv_comp       0
S:ecb_enc_bm            0x0             ecb_key_index
0xffffffff
S:fab_idx               4

```



```

S:num_be_lto          0          lto_count_reset_intvl
  0
S:lr_count_reset_intvl      0          num_be_lr
  0
S:num_fault_qsfp          0          check_lto
  0
S:credit_loaded          0          num_credit_overrun
  0
S:fec_enabled          0x0          fec_los_to_flag          0x0
S:phy_stats_clear_ts      1725611419          pcs_err_online
  0
S:pcs_err_light_det      0          pcs_err_ignore
  0
S:pcs_blk_err          0          pcs_hiber          0
S:phy_port_status      0          ecb_enc_lr_count
  0

S:dport_mode          0          avoid_lto_det          0
S:sn_debounced          0x0          sn_started_kr_reqd          0
S:major_timer_started    0x0          ready_bm          0x0
S:parln_1_bm           0x0          parln_0_bm          0x0
S:be_los_of_sync_event_intvl
be_los_of_sync_event      0          0
S:errataPtenable_cntr    0          errataPoll_cntr
  0
S:jda_rx_sig_loss_det    0          jda_rx_sig_loss_cnt
  0

S:encrypt_blk_error      0

S:
S:      c4_trunk
S:=====
S:mark_ts              0x0          deskew          0x0
S:master_phyp          0x0
S:
S:adelay[00]: 0x00000000 0x00000000 0x00000000 0x00000000
S:adelay[04]: 0x00000000 0x00000000 0x00000000 0x00000000
S:
S:      c4_buf
S:=====
S:tx_csc              0          rx_csc
  0
S:ld_vc_credits        0          tx_flag          0x0
S:alloc_buffers        0          req_buffers          0
S:est_buffers          20          ld_use_est          0
S:bb_sc_n              0          rx_bb_sc_n
  0
S:data_cr              5          nondata_cr
  6
S:cr_enable            0
S:ld_nondata_cr        6          tnodep
0xbb83b380
S:tx_credits[0] 0      0      0      0      0      0      0
S:tx_credits[8] 0      0      0      0      0      0      0
S:tx_credits[16]      0      0      0      0      0      0      0      0
S:tx_credits[24]      0      0      0      0      0      0      0      0

```

```

S:tx_credits[32]      0      0      0      0      0      0      0      0      0
S:rx_credits[0] 0    0    0    0    0    0    0    0    0
S:rx_credits[8] 0    0    0    0    0    0    0    0    0
S:rx_credits[16]      0      0      0      0      0      0      0      0      0
S:rx_credits[24]      0      0      0      0      0      0      0      0      0
S:rx_credits[32]      0      0      0      0      0      0      0      0      0
S:tx_mbc[0]      0    0    0    0    0    0    0    0    0
S:tx_mbc[8]      0    0    0    0    0    0    0    0    0
S:tx_mbc[16]     0    0    0    0    0    0    0    0    0
S:tx_mbc[24]     0    0    0    0    0    0    0    0    0
S:tx_mbc[32]     0    0    0    0    0    0    0    0    0
S:rx_mbc[0]      0    0    0    0    0    0    0    0    0
S:rx_mbc[8]      0    0    0    0    0    0    0    0    0
S:rx_mbc[16]     0    0    0    0    0    0    0    0    0
S:rx_mbc[24]     0    0    0    0    0    0    0    0    0
S:rx_mbc[32]     0    0    0    0    0    0    0    0    0

```

S:

S:C4 Chip Variables: c4_phyp->c4_chp = 0x97e28000

S:-----

S:version = 2.1

S:magic_id 0xc4234567 init_state 0x8

S:reset_reg_mem 0x1

S:ch_int0_en_bm 0x0 intr0_cause 0x0

S:ch_int1_en_bm 0x0 intr1_cause 0x0

S:ch_int2_en_bm 0x0 intr2_cause 0x0

S:ch 0x43010080 ch_cfg

0xb7013ba0

S:raslog_hndl.hndl 0x0 obj_halted 0x0

S:c4_chip_regp 0x80000000 c4_fpg_regp

0x81800000

S:num_chip_timer 0x5

S:hi_task_bm 0x0 lo_task_bm 0x0

S:c4_deferq.q_head 0x0 c4_deferq.q_tail 0x0

S:c4_tmrq.q_head 0x0 c4_tmrq.q_tail 0x0

slot_no 0

S:chip_inst 0 chip_idx 0

S:pll_initialized 1

pll_serdes_initialized 1

S:init_tries 0 init_ptEnableBM

0xba01b488

S:tick_polling 0xb980c9c0 sec_polling

0xb980c960

S:bb_fid 129

S:ecb_key_bm[0] 0x0 ecb_key_bm[1] 0x0

S:ecb_key_bm[2] 0x0 ecb_key_bm[3] 0x0

S:is_chip_enc_enabled 0

is_chip_comp_enabled 0x0

S:ftb_rsrcp->ftb_flags 0x0 act_rsrcp->act_flag 0x1

S:lue_rsrcp->lue_flags[0] 0x0 lue_rsrcp-

>lue_flags[1] 0x0

S:c4_phyp[00]: 0xb6ab0000 0xb6ab2080 0xb6ab4100 0xb6ab6180

S:c4_phyp[04]: 0xb6ab9040 0xb6abb0c0 0xb6abd140 0xb6ac0000

S:c4_phyp[08]: 0xb6ac2080 0xb6ac4100 0xb6ac6180 0xb6ac9040

```

S:c4_phyp[12]: 0xb6acb0c0 0xb6acd140 0xb6ad0000 0xb6ad2080
S:c4_phyp[16]: 0xb6ad4100 0xb6ad6180 0xb6ad9040 0xb6adb0c0
S:c4_phyp[20]: 0xb6add140 0xb6ae0000 0xb6ae2080 0xb6ae4100
S:c4_phyp[24]: 0xb6ae6180 0xb6ae9040 0xb6aeb0c0 0xb6aed140
S:c4_phyp[28]: 0xb6af0000 0xb6af2080 0xb6af4100 0xb6af6180
S:c4_phyp[32]: 0xb6af9040 0xb6afb0c0 0xb6afd140 0xb6b00000
S:c4_phyp[36]: 0xb6b02080 0xb6b04100 0xb6b06180 0xb6b09040
S:c4_phyp[40]: 0xb6b0b0c0 0xb6b0d140 0xb6b10000 0xb6b12080
S:c4_phyp[44]: 0xb6b14100 0xb6b16180 0xb6b19040 0xb6b1b0c0
S:c4_phyp[48]: 0xb6b1d140 0xb6b20000 0xb6b22080 0xb6b24100
S:c4_phyp[52]: 0xb6b26180 0xb6b29040 0xb6b2b0c0 0xb6b2d140
S:c4_phyp[56]: 0xb6b30000 0xb6b32080 0xb6b34100 0xb6b36180
S:c4_phyp[60]: 0xb6b39040 0xb6b3b0c0 0xb6b3d140 0xb6b40000
S:c4_lgcp[00]: 0x97f48000 0x97f4c000 0x97f50000 0x97f54000
S:c4_lgcp[04]: 0x97f58000 0x97f5c000 0x97f60000 0x97f64000
S:c4_lgcp[08]: 0x97f68000 0x97f6c000 0x97f70000 0x97f74000
S:c4_lgcp[12]: 0x97f78000 0x97f7c000 0x97f80000 0x97f84000
S:c4_lgcp[16]: 0x97f88000 0x97f8c000 0x97f90000 0x97f94000
S:c4_lgcp[20]: 0x97f98000 0x97f9c000 0x97fa0000 0x97fa4000
S:c4_lgcp[24]: 0x97fa8000 0x97fac000 0x97fb0000 0x97fb4000
S:c4_lgcp[28]: 0x97fb8000 0x97fbc000 0x97fc0000 0x97fc4000
S:c4_lgcp[32]: 0x97fc8000 0x97fcc000 0x97fd0000 0x97fd4000
S:c4_lgcp[36]: 0x97fd8000 0x97fdc000 0x97fe0000 0x97fe4000
S:c4_lgcp[40]: 0x97fe8000 0x97fec000 0x97ff0000 0x97ff4000
S:c4_lgcp[44]: 0x97ff8000 0x97ffc000 0x8e000000 0x8e004000
S:c4_lgcp[48]: 0x8e008000 0x8e00c000 0x8e010000 0x8e014000
S:c4_lgcp[52]: 0x8e018000 0x8e01c000 0x8e020000 0x8e024000
S:c4_lgcp[56]: 0x8e028000 0x8e02c000 0x8e030000 0x8e034000
S:c4_lgcp[60]: 0x8e038000 0x8e03c000 0x8e040000 0x8e044000
S:chip_timers[00]: 0xb980c720 0xb980c780 0xb980c7e0 0xb980c840
S:chip_timers[04]: 0xb980c8a0 0xb980c900
S:disc_trap_enable_required      0x0          rxlp_disc_log_stop
          0x0
S:curr_rxlp_frm_cnt      0x0          curr_rxlp_disc_frm_cnt  0x0
S:sw_disc_frm_cnt      0x0          last_disc_frm_cnt      0x0
S:txq_nopop_pr_cnt      0x0          pollErrataDfe_ptBM
0xba01b4b0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][0]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][1] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][2]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][0] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][1]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][2] 0x0
S:
S:C4 Logical Port Variables
S:-----
-----
S:c4_lgc_regp      0x81c70000
S:c4_phyp:
S:      0xb6ad0000      0x0          0x0          0x0

S:      0x0          0x0          0x0          0x0

S:master_phyp      0xb6ad0000      if_id

```

```

0x4302000e
S:min_phyp                0x0          max_phyp                0x0
S:num_phy_ports           1            lgc_num                 14
S:num_iu_to               0            sw_txq_bm
0
S:port_fid                129         unused                  0
S:port_group             1            lgc_stats_clear_ts
1725611419
S:domain_tbl_sel         0            area_tbl_sel
0
S:egid_tbl_sel           0
S:serv_lo_bm             0x0
S:

```

S:Proto Phy Variables:

S:-----

```

S:magic_id                0xc4123456   asic_phyp
0xb6ad0000
S:port_id                 0x4302800e   phy_cfg
0xb6ad1040
S:upsm_hdl                0xb8013e60   physm_hdl
0xb8013be0
S:ov_snsn_hdl            0xb8013aa0   sw_snsn_hdl
0xb8013b40
S:ov_lksm_hdl            0xb8013c80   sw_lksm_hdl
0xb8013d20
S:trksm_hdl              0xb8013dc0   lr_flag                 0x0
S:lr_active              0x0          qsfm_txxrx_rate_sel
0x0

```

S:

```

S:UPSM      UP00: UPST_PORT_DISABLED  --> UP00: UPST_PORT_DISABLED
S:SNSM(OV)  SN00: OV_SNST_STOPPED           --> SN00: OV_SNST_STOPPED
S:SNSM(SW)  SW00: SW_SNST_STAGE_WS    --> SW00: SW_SNST_STAGE_WS
S:PHYSM     PP00: PHYST_STOPPED       --> PP00: PHYST_STOPPED
S:LKSM(OV)  LK00: OV_LKST_INACTIVE    --> LK00: OV_LKST_INACTIVE
S:LKSM(SW)  SW13: INACTIVE            --> SW13: INACTIVE
S:TRKSM     TRK0: TRKST_INIT          --> TRK0: TRKST_INIT

```

S:physm variables:

S:-----

```

S:proto_phyp             0xb8808900   physm_hdl
0xb8013be0
S:force_offline         0            copper                  0
S:fault_reason          0: UNKNOWN
S:phy_media_present     0
S:

```

S:snsn variables:

S:-----

```

S:speed                0xff         proto_phyp
0xb8808900
S:hw_sn_tries_left     0x0          sw_sn_tries_left       0x0
S:curr_txsp_count      0x0          0x0

```

```

S:tx_max          0x0          curr_tx_indx
   0x0
S:curr_tx         0x0          curr_rxsp_count
   0x0
S:rx_max         0x0          curr_rx_indx
   0x0
S:curr_rx        0x0          rx_mem
   0x0
S:rxsp_rec_count 0x0
S:nc_start       0x0          tx_start          0x0
S:sync_start     0x0          sync_present    0x0
S:diag_auto      0x0          diag_speed      0xff
S:striped_wd_tov 3000          hw_wd_tov
   3000
S:step           0x0          qsfp28_speed_mode
   0x0
S:qsfp_mode0_hw_sn_tries_left 0x0
S:qsfp_mode1_hw_sn_tries_left 0x0
S:
S:lksm variables:
S:-----
-----
S:proto_phyp     0xb8808900    ov_lksm_hdl
0xb8013c80
sw_lksm_hdl     0xb8013d20
num_lf1         0
S:hw_link_tries_left 0          sw_link_tries_left 0
S:buf_ptype      0x0          stored_entry_state 0x6
S:handshake_owner 0x0          mark_unsent
   0x0
S:busybuf_stuck  0x0          lr_wait          0x0
S:
S:trksm variables:
S:-----
-----
S:Not a trunk port
S:
S:upsm variables:
S:-----
-----
S:proto_phyp     0xb8808900    upsm_hdl
0xb8013e60
S:bb_credits     0          port_beacon        0
S:port_diag_flag 0          force_offline
   0
S:port_fault_rsn 0: PORT_NO_FAULT
S:retry_init_rsn 0: UNKNOWN
S:limit_reason   0          limit_result        0
S:ie_fctl_mode   0          fec_in_sync_tries_left 0
S:retry_sn_fail_init 0
retry_link_fail_init 0
S:excess_lr_count 0
S:
S:c4_ch_cfg

```

```

S:-----
-----
S:c4_desc_ring_size      256      292      256      256      292
292      2      292      292
S:thresh_def            0      16      1      0
S:intr_tries            500      cmem_pattern
0xdeadbeef
S:cmem_pattern_upwd     2      cmem_init_time      16
S:cmem_init_tries      5
S:ctrl_par_thresh      2      data_par_thresh
4
S:cam_par_thresh       4      buf_loss_thresh
12
S:crit_par_thresh      2      non_crit_par_thresh
6
S:pci_abort_thresh     10      pci_err_thresh      5
S:excess_chintr_thresh 8      sw_err_thresh      20
S:err_sample_period    300      intr_sleep
20000
S:frame_timeout        2500      proxy_dev      16384
S:vf_route             81920      qos      2048
S:stats 2048          f_redirect      2048
S:rsp_trap             2048      lun_zoning      20480
S:area_mode            0      ftb_max_loop[0]    0
S:ftb_max_loop[1]      6      ftb_max_loop[2]    9
S:ftb_max_loop[3]      10     ftb_max_loop[4]    10
S:ftb_max_loop[5]      5      ftb_max_loop[6]    6
S:ftb_seg_size[0]      0      ftb_seg_size[1]
16384
S:ftb_seg_size[2]      65536     ftb_seg_size[3]
16384
S:ftb_seg_size[4]      16384     ftb_seg_size[5]
65536
S:ftb_seg_size[6]      16384     ftb_seg_base[0]    0
S:ftb_seg_base[1]      0      ftb_seg_base[2]
65536
S:ftb_seg_base[3]      16384     ftb_seg_base[4]
32768
S:ftb_seg_base[5]      131072    ftb_seg_base[6]
49152
asic_err_monitor_period1 300
asic_err_monitor_period2 86400
zone_chk_to_poll_period 25
zone_chk_class2_reject_tov
S:
S:c4_phy_cfg
S:-----
-----
S:version = 2.1
S:pt                    0x4302800e      fab_ptr
0x9a800000
S:fabattr                0x9a8000d4      fab_iop
0x9a800050
S:cfgbm                  0xbb83b0e4      port_ctrl

```

```

0xb6ad1058
S:pcap.pcap_bm          0x8d215547      pcap.pcap2_bm
0x2588289
S:pcap.pcap3_bm        0x1bebe0c
ui_idx                  55              S:slot_no
    0
is_icl                  0              S:sw_usr_ports      400
S:neg_speed             0 0 0 0 0
S:my_domain             0x1
S:hw_sn_maxtries        100            sw_sn_maxtries
    0
S:hw_link_maxtries     10             sw_link_maxtries    5
S:rx_cyc_tov            28            rttov               300
S:bufrdy_tov           300           busybuf_tov         286
S:mark_tov              300           lksm_tov             3000
S:buf_dealloc_wait     4             hw_wd_tov           3000
S:hw_lk_train_tov      540           hw_lk_test_tov
    150
S:syswait_tx_12_lips   1             lip_rx_tov           55
S:al_time_tov           15            lp_tov              2000
S:intr_tries_port      500           intr_mod_debounce
    250
S:intr_lsrflt_debounce 500           intr_efifo_debounce 100
S:port_no_fid           3             excess_ptintr_thresh 8
S:port_fault1_thresh   100          port_fault1_spur_thresh 250
S:port_fault1_disc_thresh 500
port_fault1_disc_spur_thresh 1000
S:port_fault2_thresh   5             losync_tov           100
S:port_sw_link_to      15            en_8g_scramble
    1
frc_hw_sn_mode          0x1
S:enc_poll_thresh       0             fec_enable
    0
S:fec_in_sync_to        50            fec_in_sync_try_max
    4
S:port_be_lto_threshold 100           port_be_lr_threshold
    2
S:be_cr_in_sync_to     5
port_credit_overrun_thresh 10
S:jda_sfp_losig_tov    400
jda_sfp_losig_try_max  30
S:striped_wd_tov       3000
no_sync_debounce       1200
S:
S:    fab_iop
S:=====
S:fab_iop->interop_mode 0x0      fab_iop->lab_mode    0x0
S:fab_iop->fl_bbc        0x0      fab_iop->fl_fan
    0x0
S:fab_iop->fl_cls        0x4      fab_iop->fl_rscn
    0x0
S:fab_iop->domain_id_offset 0x60    fab_iop-
>mcdt_fabric_mode      0x0
S:fab_iop->mcdt_default_zone 0x0      fab_iop-

```

```

>mcdt_safe_zone          0x0
S:
S:   port_ctrl
S:=====
S:port_ctrl.port_type    1          port_ctrl.port_grp      1
S:port_ctrl.port_number 55          port_ctrl.vc_mode        1
S:
S:   port_ctrl.lcap
S:=====
S:has_serdes             0          has_media                 1
S:topology               1          skip_nego                 0
S:skip_pnego             0          skip_init_event          0
S:en_shim                 0          speed_neg                 0
S:en_shim                 1
S:loop_back              0          num_speeds                5
S:fec_enable              0
S:
S:   port_ctrl.speed_list array
S:=====
S:speed_list[0].auto_neg 1          speed_list[0].lnk_speed  0x0000000a
S:speed_list[1].auto_neg 1          speed_list[1].lnk_speed  0x00000008
S:speed_list[2].auto_neg 1          speed_list[2].lnk_speed  0x00000006
S:speed_list[3].auto_neg 1          speed_list[3].lnk_speed  0x00000005
S:speed_list[4].auto_neg 1          speed_list[4].lnk_speed  0x00000003
S:speed_list[5].auto_neg 0          speed_list[5].lnk_speed  0x00000000
S:
S:   port_ctrl.cm
S:=====
S:port_ctrl.cm.num_vcs      8
S:port_ctrl.cm.min_bufs    8
S:port_ctrl.cm.cr_shar_bufs 0
S:port_ctrl.vc_alloc
S:port_ctrl.vc_alloc      2 0 1 1 1 1 1 1
S:port_ctrl.vc_alloc      0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.norm_vc_alloc
S:port_ctrl.norm_vc_alloc  4 0 5 5 5 5 1 1
S:port_ctrl.norm_vc_alloc  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.cm.skip_bb_credit      0
S:port_ctrl.cm.use_shim_based_sublist 0
S:
S:   port_ctrl.serdes_set
S:=====
S:serdes_type              0x8
S:serdes_data_t.ibm_hss_serdes.tx_drive_power      0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b_sign 0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b      0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_a      0x0
S:serdes_data_t.ibm_hss_serdes.rxeq                0x0
S:
S:   cfgbm
S:=====
S:old_distance             0x0          gport_lockdown          0x0

```



```

S:tport          0x1          speed          0x0
S:disable_eport  0x0          fcacc          0x0
S:lport_lockdown 0x0          0x0          priv_lport_lockdown
          0x0
S:vcxlt_linit   0x0          delay_flogi    0x0
S:isl_interop   0x0          distance       0x0
S:BufStarvFlag  0x0          credit_sharing 0x0
S:lport_halfduplex 0x0          lport_fairness 0x0
S:soft_neg      0x0          asn_frc_hwretry 0x0
S:cr_recov      0x0          fport_buffers  0x0
S:export        0x0          0x0          export_mode
          0x0
S:csctl_en      0x0          mirror_port    0x0
S:fault_delay   0x0          non_dfe        0x0
S:fec_configured*(0=ENAB) 0          0          fec_tts
          0
S:port_persistently_disabled (permanently) 0 (0)
S:
S:      cfg property
S:=====
S:priv_pcfg_bm  0x00000000  lgcl_pcfg_bm
0xbb83b124
S:fport_buffer  0x00000000
S:
S:
S:C4 Discard Cntrs: rxlp_stats = 0xb6ad03b0
S:-----
-----
S:disc_mcast_wka 0x0          disc_inv_did   0x0
S:disc_cl1_cl4   0x0          disc_sid_chk_fail 0x0
S:disc_inv_dom_egid_txpt 0x0          0x0          disc_vft_hop_cnt_1
          0x0
S:disc_classf    0x0          0x0          disc_fcp_cdb_inv  0x0
S:disc_vfid_trap_enabled 0x0          0x0
disc_vfid_hdr_chk_fail 0x0
S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err 0x0
S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err 0x0
S:disc_ftb_vm_mode 0x0          disc_ftb_agnt2_miss 0x0
S:disc_ecb_de_pad_err 0x0          disc_ecb_de_tag_err 0x0
S:disc_ecb_de_seq_err 0x0          disc_ecb_err 0x0
S:disc_ftb_type4_match 0x0          disc_fcp_rsp_ftb_type4 0x0
S:disc_fcp_rsp_ftb_type4 0x0          0x0          disc_ftb_type5_match
          0x0
S:disc_ftb_type3_match 0x0          disc_els_ftb_type3 0x0
S:disc_ftb_type1_match 0x0          disc_els_rsp_ex_port 0x0
S:disc_inv_drp_dps 0x0          disc_did_lookup_miss 0x0
S:disc_ftb_type2_match 0x0          disc_trpd_plogi_pdisc 0x0
S:disc_type2_lookup_miss 0x0          0x0          disc_ftb_type6_match
          0x0
S:disc_els_rep_ex_port 0x0          0x0          disc_els_sid_lkup_bit1 0x0
S:disc_els_sid_lkup_bit0 0x0          0x0
disc_bls_frm_trap_bit1 0x0
S:disc_ftb_token_err 0x0          disc_asic_internal_err 0x0
S:disc_hard_zone_miss 0x0          disc_lun_zone_miss 0x0

```

```

S:disc_flt_frame_disc 0x0          disc_flt_parity_err 0x0
S:disc_frame_marked_du 0x0        disc_frame_marked_to 0x0
E:Connection type: FE
E:Port type: E_port
E:Trunk port: No
E:Configured Speed: AUTO_SPEED_NEGO
E:Max Capable Speed: 32G
E:Current SNSM Speed: UNDEFINED
E:Hardware TX Speed: 32G (0x00000004)
E:Hardware RX Speed: 32G (0x00000040)
E:
E:Interrupts: 0          Link_failure: 0
Loss_of_sync: 0        Loss_of_sig: 0
E:Lli: 0              Invalid_word: 0
E:trapped_frm: 0      fwd_status_ok: 0
E:fwd_timeout: 0      fwd_tx_unavail: 0
E:fwd_unroutable: 0    fwd_zone_out: 0
E:fwd_other_err: 0    frm_err_discard: 0
E:Fltr listA: 0       Fltr listB: 0
E:Zone trap fwd: 0    Zone trap disc: 0
E:shim_csum: 0        RTE_perr: 0
E:Invalid_crc: 0     Delim_err: 0
E:Protocol_err: 0
E:Lr_in: 0           Lr_out: 0
E:Ols_in: 0          Ols_out: 0

```

filterportshow 55

FILTER DATA

```

Shadow settings:
  Filter Enable: 0x00000000
  Redir RAM[0]: 0x00000000
  Redir RAM[1]: 0x00000000
  Redir RAM[2]: 0x00000000
  Redir RAM[3]: 0x00000000
  Redir RAM[4]: 0x00000000
  Redir RAM[5]: 0x00000000
  Redir RAM[6]: 0x00000000
  Redir RAM[7]: 0x00000000
  Redir RAM[8]: 0x00000000
  Redir RAM[9]: 0x00000000
  Redir RAM[10]: 0x00000000
  Redir RAM[11]: 0x00000000
  Redir RAM[12]: 0x00000000
  Redir RAM[13]: 0x00000000
  Redir RAM[14]: 0x00000000
  Redir RAM[15]: 0x00000000
  Redir RAM[16]: 0x00000000
  Redir RAM[17]: 0x00000000
  Redir RAM[18]: 0x00000000
  Redir RAM[19]: 0x00000000
  Redir RAM[20]: 0x00000000

```

Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass: 0x00000000

Real settings:

Enable RAM: 0x00000000, 0x00000000

Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass RAM: 0x00000000

Shadowed filters:

Filter 0: Not Installed (MIRROR1)(LISTA)

c4_fldenable[0] = 0x00000000 0x00000000 0x00000000
0x00000000

c4_fldnegate[0] = 0x00000000, c4_fltr_config[0] = 0x00000000

Filter 1: Not Installed (MIRROR2)(LISTA)
c4_fldenable[1] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[1] = 0x00000000,c4_fltr_config[1] = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
c4_fldenable[2] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[2] = 0x00000000,c4_fltr_config[2] = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
c4_fldenable[3] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[3] = 0x00000000,c4_fltr_config[3] = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
c4_fldenable[4] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[4] = 0x00000000,c4_fltr_config[4] = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
c4_fldenable[5] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[5] = 0x00000000,c4_fltr_config[5] = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
c4_fldenable[6] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[6] = 0x00000000,c4_fltr_config[6] = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
c4_fldenable[7] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[7] = 0x00000000,c4_fltr_config[7] = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
c4_fldenable[8] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[8] = 0x00000000,c4_fltr_config[8] = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
c4_fldenable[9] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[9] = 0x00000000,c4_fltr_config[9] = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
c4_fldenable[10] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[10] = 0x00000000,c4_fltr_config[10] =
0x00000000
Filter 11: Not Installed (SIM)(LISTA)
c4_fldenable[11] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[11] = 0x00000000,c4_fltr_config[11] =
0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
c4_fldenable[12] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[12] = 0x00000000,c4_fltr_config[12] =
0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
c4_fldenable[13] = 0x00000000 0x00000000 0x00000000
0x00000000

```
    c4_fldnegate[13] = 0x00000000,c4_fltr_config[13] =
0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
    c4_fldenable[14] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[14] = 0x00000000,c4_fltr_config[14] =
0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
    c4_fldenable[15] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[15] = 0x00000000,c4_fltr_config[15] =
0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
    c4_fldenable[16] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[16] = 0x00000000,c4_fltr_config[16] =
0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
    c4_fldenable[17] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[17] = 0x00000000,c4_fltr_config[17] =
0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
    c4_fldenable[18] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[18] = 0x00000000,c4_fltr_config[18] =
0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
    c4_fldenable[19] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[19] = 0x00000000,c4_fltr_config[19] =
0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
    c4_fldenable[20] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[20] = 0x00000000,c4_fltr_config[20] =
0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
    c4_fldenable[21] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[21] = 0x00000000,c4_fltr_config[21] =
0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
    c4_fldenable[22] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[22] = 0x00000000,c4_fltr_config[22] =
0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
    c4_fldenable[23] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[23] = 0x00000000,c4_fltr_config[23] =
0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
    c4_fldenable[24] = 0x00000000 0x00000000 0x00000000
```

```
0x00000000
    c4_fldnegate[24] = 0x00000000,c4_fltr_config[24] =
0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
    c4_fldenable[25] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[25] = 0x00000000,c4_fltr_config[25] =
0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
    c4_fldenable[26] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[26] = 0x00000000,c4_fltr_config[26] =
0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
    c4_fldenable[27] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[27] = 0x00000000,c4_fltr_config[27] =
0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
    c4_fldenable[28] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[28] = 0x00000000,c4_fltr_config[28] =
0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
    c4_fldenable[29] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[29] = 0x00000000,c4_fltr_config[29] =
0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    c4_fldenable[30] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[30] = 0x00000000,c4_fltr_config[30] =
0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    c4_fldenable[31] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[31] = 0x00000000,c4_fltr_config[31] =
0x00000000
```

Real filters:

```
Filter 0: Not Installed (MIRROR1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
```

Filter 3: Not Installed (MIRROR4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 5: Not Installed (ZONING TRAP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 7: Not Installed (TIN TRAP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 8: Not Installed (FICON CUP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 9: Not Installed (FICON CUP DST)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 11: Not Installed (SIM)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 12: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 13: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 14: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 15: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 16: Not Installed (PERF1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,

0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 30: Not Installed (IPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter dirty indicator: 0x00000000
Performance filters: 0
Port Mirror filters: 0 (0x0)

FIELD DATA

Shadowed fields:

fldoffset[0] = 0x00, fldmask[0] = 0x00, fldvalue_dyna[0]: 0x00 0x00
0x00 0x00
fldcontrol[0].inuse = 0x0 fldcontrol[0].refcnt = 0x00 0x00 0x00
0x00
fldoffset[1] = 0x00, fldmask[1] = 0x00, fldvalue_dyna[1]: 0x00 0x00
0x00 0x00
fldcontrol[1].inuse = 0x0 fldcontrol[1].refcnt = 0x00 0x00 0x00
0x00
fldoffset[2] = 0x00, fldmask[2] = 0x00, fldvalue_dyna[2]: 0x00 0x00
0x00 0x00
fldcontrol[2].inuse = 0x0 fldcontrol[2].refcnt = 0x00 0x00 0x00
0x00
fldoffset[3] = 0x00, fldmask[3] = 0x00, fldvalue_dyna[3]: 0x00 0x00
0x00 0x00
fldcontrol[3].inuse = 0x0 fldcontrol[3].refcnt = 0x00 0x00 0x00
0x00
fldoffset[4] = 0x00, fldmask[4] = 0x00, fldvalue_dyna[4]: 0x00 0x00
0x00 0x00
fldcontrol[4].inuse = 0x0 fldcontrol[4].refcnt = 0x00 0x00 0x00
0x00
fldoffset[5] = 0x00, fldmask[5] = 0x00, fldvalue_dyna[5]: 0x00 0x00
0x00 0x00
fldcontrol[5].inuse = 0x0 fldcontrol[5].refcnt = 0x00 0x00 0x00
0x00
fldoffset[6] = 0x00, fldmask[6] = 0x00, fldvalue_dyna[6]: 0x00 0x00
0x00 0x00
fldcontrol[6].inuse = 0x0 fldcontrol[6].refcnt = 0x00 0x00 0x00
0x00
fldoffset[7] = 0x00, fldmask[7] = 0x00, fldvalue_dyna[7]: 0x00 0x00
0x00 0x00
fldcontrol[7].inuse = 0x0 fldcontrol[7].refcnt = 0x00 0x00 0x00
0x00
fldoffset[8] = 0x00, fldmask[8] = 0x00, fldvalue_dyna[8]: 0x00 0x00
0x00 0x00
fldcontrol[8].inuse = 0x0 fldcontrol[8].refcnt = 0x00 0x00 0x00

```
0x00
fldoffset[9] = 0x00, fldmask[9] = 0x00, fldvalue_dyna[9]:0x00 0x00
0x00 0x00
fldcontrol[9].inuse = 0x0 fldcontrol[9].refcnt = 0x00 0x00 0x00
0x00
fldoffset[10] = 0x00, fldmask[10] = 0x00, fldvalue_dyna[10]:0x00 0x00
0x00 0x00
fldcontrol[10].inuse = 0x0 fldcontrol[10].refcnt = 0x00 0x00 0x00
0x00
fldoffset[11] = 0x00, fldmask[11] = 0x00, fldvalue_dyna[11]:0x00 0x00
0x00 0x00
fldcontrol[11].inuse = 0x0 fldcontrol[11].refcnt = 0x00 0x00 0x00
0x00
fldoffset[12] = 0x00, fldmask[12] = 0x00, fldvalue_dyna[12]:0x00 0x00
0x00 0x00
fldcontrol[12].inuse = 0x0 fldcontrol[12].refcnt = 0x00 0x00 0x00
0x00
fldoffset[13] = 0x00, fldmask[13] = 0x00, fldvalue_dyna[13]:0x00 0x00
0x00 0x00
fldcontrol[13].inuse = 0x0 fldcontrol[13].refcnt = 0x00 0x00 0x00
0x00
fldoffset[14] = 0x00, fldmask[14] = 0x00, fldvalue_dyna[14]:0x00 0x00
0x00 0x00
fldcontrol[14].inuse = 0x0 fldcontrol[14].refcnt = 0x00 0x00 0x00
0x00
fldoffset[15] = 0x00, fldmask[15] = 0x00, fldvalue_dyna[15]:0x00 0x00
0x00 0x00
fldcontrol[15].inuse = 0x0 fldcontrol[15].refcnt = 0x00 0x00 0x00
0x00
fldoffset[16] = 0x00, fldmask[16] = 0x00, fldvalue_dyna[16]:0x00 0x00
0x00 0x00
fldcontrol[16].inuse = 0x0 fldcontrol[16].refcnt = 0x00 0x00 0x00
0x00
fldoffset[17] = 0x00, fldmask[17] = 0x00, fldvalue_dyna[17]:0x00 0x00
0x00 0x00
fldcontrol[17].inuse = 0x0 fldcontrol[17].refcnt = 0x00 0x00 0x00
0x00
fldoffset[18] = 0x00, fldmask[18] = 0x00, fldvalue_dyna[18]:0x00 0x00
0x00 0x00
fldcontrol[18].inuse = 0x0 fldcontrol[18].refcnt = 0x00 0x00 0x00
0x00
fldoffset[19] = 0x00, fldmask[19] = 0x00, fldvalue_dyna[19]:0x00 0x00
0x00 0x00
fldcontrol[19].inuse = 0x0 fldcontrol[19].refcnt = 0x00 0x00 0x00
0x00
```

Real fields:

```
fldoffset RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000
fldmask RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000
fld value4 RAM:
0x00000000
```


Filter counter 11: 0 (SIM)
Filter counter 12: 0 (UNUSED)
Filter counter 13: 0 (UNUSED)
Filter counter 14: 0 (UNUSED)
Filter counter 15: 0 (UNUSED)
Filter counter 16: 0 (PERF1)
Filter counter 17: 0 (PERF2)
Filter counter 18: 0 (PERF3)
Filter counter 19: 0 (PERF4)
Filter counter 20: 0 (PERF5)
Filter counter 21: 0 (PERF6)
Filter counter 22: 0 (PERF7)
Filter counter 23: 0 (PERF8)
Filter counter 24: 0 (PERF9)
Filter counter 25: 0 (PERF10)
Filter counter 26: 0 (PERF11)
Filter counter 27: 0 (PERF12)
Filter counter 28: 0 (OPM1)
Filter counter 29: 0 (OPM2)
Filter counter 30: 0 (IPM1)
Filter counter 31: 0 (IPM2)

ACL DATA

Logical port 14: Hard Zoning disabled, Soft Zoning disabled
Zone type: WWN Zoning
Frames with hard zone miss: 0

*** Please use filterportshow on user port 56 to display ACL hash tables and Mirroring resources of thischip.
***We show this data only for the first physical port which is an external port.

portFcPortCmdShow --slot 0 56 3
doing portFcPortCmdShow: arg1 = 3, arg2 = -2

portshow 56
portDisableReason: None
portCFlags: 0x0
portFlags: 0x4021 PRESENT U_PORT DISABLED LED
LocalSwcFlags: 0x0
portType: 26.0
POD Port: Need license to enable the port
portState: 2 Offline
Protocol: FC
portPhys: 2 No_Module portScn: 2 Offline
port generation number: 0
state transition count: 0

portId: 013800
portIfId: 43020000
portWwn: 20:38:d8:1f:cc:2c:99:90
portWwn of device(s) connected:
16b Area list:

Distance: normal
portSpeed: N32Gbps

FEC: Inactive
Credit Recovery: Inactive
LE domain: 0
Peer beacon: Off
FC Fastwrite: OFF

| | | | | |
|-------------|---|---------------|---|-------|
| Interrupts: | 0 | Link_failure: | 0 | Frjt: |
| 0 | | | | |
| Unknown: | 0 | Loss_of_sync: | 0 | Fbsy: |
| 0 | | | | |
| Lli: | 0 | Loss_of_sig: | 0 | |
| Proc_rqrd: | 0 | Protocol_err: | 0 | |
| Timed_out: | 0 | Invalid_word: | 0 | |
| Tx_unavail: | 0 | Invalid_crc: | 0 | |
| Delim_err: | 0 | Address_err: | 0 | |
| Lr_in: | 0 | Ols_in: | 0 | |
| Lr_out: | 0 | Ols_out: | 0 | |

portloginshow 56

| Type | PID | World Wide Name | credit | df_sz | cos |
|-------|-----|-----------------|--------|-------|-----|
| ===== | | | | | |

portloginshow 56 -history

| Type | PID | World Wide Name | logout | time |
|-------|-----|-----------------|--------|------|
| ===== | | | | |

portregshow 56

LED registers

=====

| | | | |
|-------------|---------------|----------|-------------|
| 0x81c02000: | c4_led_status | 00000000 | 0x81c02004: |
| | c4_led_ctl | 00000000 | |

FPL registers

=====

| | | | |
|-------------|-------------------------|----------|-------------|
| 0x81c00200: | fpl_port_config | 23490000 | |
| 0x81c0020c: | fpl_port_id_ctl | 00000000 | 0x81c00210: |
| | fpl_port_id_addr | 00013800 | |
| 0x81c00214: | fpl_port_speed | 00000004 | 0x81c0021c: |
| | fpl_lli_ctl | 00000903 | |
| 0x81c00228: | fpl_lli_os_ctl | bc95b5b5 | 0x81c0022c: |
| | fpl_lli_send_word | bc95b5b5 | |
| 0x81c00230: | fpl_lli_mark_rx | 00000000 | 0x81c00234: |
| | fpl_lli_rnd_trip_time | 00000000 | |
| 0x81c00238: | fpl_lli_ns_status | 00070007 | 0x81c0023c: |
| | fpl_lli_intr_status | 80070007 | |
| 0x81c00244: | fpl_lli_def | 00000000 | 0x81c00254: |
| | fpl_lli_intr_enable_clr | 00100000 | |
| 0x81c00258: | fpl_err_intr_status | 00000000 | 0x81c00260: |

```

fpl_err_intr_enable_clr 00000000
0x81c00268: fpl_err_first_error 00000000 0x81c0026c:
fpl_speed_neg_ctl 00000000
0x81c00270: fpl_speed_neg_stat 00000000 0x81c00274:
fpl_softasn_ctl 0000000f
0x81c00278: fpl_link_init_ctl 00000000 0x81c0027c:
fpl_link_init_stat 00000000
0x81c00280: fpl_aec_ctl 00051060 0x81c00284:
fpl_aec_ctl2 04009f60
0x81c00288: fpl_pcs_ctl 00000160 0x81c0028c:
fpl_fec_ctl 00000441
0x81c00290: fpl_fec_cor 00000000 0x81c00294:
fpl_fec_uncor 00000000
0x81c00298: fpl_hss_link_ctl 0031f040 0x81c0029c:
fpl_afifo_link_ctl 00000a86
0x81c002a0: fpl_echo_lb_ctl 0000028c 0x81c002a4:
fpl_scratch 01000121
0x81c002a8: fpl_debug 00030005 0x81c002ac:
fpl_misc_debug 00001800
0x00000000: SW_shadow_reg 00000000 0x00000000:
SW_c4_phyp->cfgptr 00030000

```

per-fpg (per octet) registers

=====

```

0x8180382c: fpg_serdes_ctla0 81a37be7 0x81803830:
fpg_serdes_ctla1 81a37be7
0x81803834: fpg_serdes_ctlb0 81a1c3c3 0x81803838:
fpg_serdes_ctlb1 81a1c3c3
0x8180383c: fpg_serdes_xgmii_1ms 00067c28 0x81803840:
fpg_serdes_regtimctl 40e47946
0x81803844: fpg_serdes_asnrsttimctl 00000102

```

HSS PLL registers

=====

```

0x81801400: 00_hssplla_vco_coarse_cal0 00000000 0x81801404:
01_hssplla_vco_coarse_cal1 00000014
0x81801408: 02_hssplla_vco_coarse_cal2 00000000 0x8180140c:
03_hssplla_vco_coarse_cal3 00000000
0x81801410: 04_hssplla_vco_coarse_cal4 00000000 0x81801424:
09_hssplla_power_ctl 00000000
0x81801428: 0A_hssplla_charge_pump_ctl 00000004 0x81801438:
0E_hssplla_pll_misc_ctl 00000000
0x8180143c: 0F_hssplla_pclk_ctl 000000f8 0x81801440:
10_hssplla_eyem_intv_ctl 00000000
0x81801444: 11_hssplla_eyem_intv_lim1 00000000 0x81801448:
12_hssplla_eyem_intv_lim2 00000000
0x8180144c: 13_hssplla_eyem_intv_lim3 00000000 0x81801450:
14_hssplla_eyem_intv_lim4 00000000
0x818014f0: 3C_hssplla_macro_tst_ctl4 00000000 0x818014f4:
3D_hssplla_macro_tst_ctl3 00000000
0x818014f8: 3E_hssplla_macro_tst_ctl2 00000000 0x818014fc:
3F_hssplla_macro_tst_ctl1 00000000
0x81801500: 00_hssppll_vco_coarse_cal0 0000000a 0x81801504:
01_hssppll_vco_coarse_cal1 00000014

```

| | | |
|---|----------|-------------|
| 0x81801508: 02_hsspll_b_vco_coarse_cal2 | 00000000 | 0x8180150c: |
| 03_hsspll_b_vco_coarse_cal3 | 00000000 | |
| 0x81801510: 04_hsspll_b_vco_coarse_cal4 | 00000000 | 0x81801524: |
| 09_hsspll_b_power_ctl | 00000000 | |
| 0x81801528: 0A_hsspll_b_charge_pump_ctl | 00000004 | 0x81801538: |
| 0E_hsspll_b_pll_misc_ctl | 00000000 | |
| 0x8180153c: 0F_hsspll_b_pclk_ctl | 000000f8 | 0x81801540: |
| 10_hsspll_b_eyem_intv_ctl | 00000000 | |
| 0x81801544: 11_hsspll_b_eyem_intv_lim1 | 00000000 | 0x81801548: |
| 12_hsspll_b_eyem_intv_lim2 | 00000000 | |
| 0x8180154c: 13_hsspll_b_eyem_intv_lim3 | 00000000 | 0x81801550: |
| 14_hsspll_b_eyem_intv_lim4 | 00000000 | |
| 0x818015f0: 3C_hsspll_b_macro_tst_ctl4 | 00000000 | 0x818015f4: |
| 3D_hsspll_b_macro_tst_ctl3 | 00000000 | |
| 0x818015f8: 3E_hsspll_b_macro_tst_ctl2 | 00000000 | 0x818015fc: |
| 3F_hsspll_b_macro_tst_ctl1 | 00000000 | |

HSS TX registers

=====

| | | |
|--|----------|-------------|
| 0x81800000: 00_hsstx_cfg_mode_PHY | 00009f48 | 0x81800004: |
| 01_hsstx_test_ctl | 00000000 | |
| 0x81800008: 02_hsstx_coeff_ctl_INV | 00000000 | 0x8180000c: |
| 03_hsstx_drv_mode_ctl | 00000000 | |
| 0x81800010: 04_hsstx_drv_ovrd_ctl | 00000010 | 0x81800014: |
| 05_hsstx_dclk_align_ovrd | 00000080 | |
| 0x81800018: 06_hsstx_imp_cal_ovrd | 00000c0c | 0x8180001c: |
| 07_hsstx_dclk_drift_tol | 00000004 | |
| 0x81800020: 08_hsstx_tap0_coeff_TUNE | 00000000 | 0x81800024: |
| 09_hsstx_tap1_coeff_TUNE | 00000003 | |
| 0x81800028: 0A_hsstx_tap2_coeff_TUNE | 00000018 | 0x8180002c: |
| 0B_hsstx_tap3_coeff_TUNE | 0000000d | |
| 0x81800034: 0D_hsstx_pol_INV | 0000000a | 0x81800038: |
| 0E_hsstx_ae_cmd | 00000000 | |
| 0x8180003c: 0F_hsstx_ae_stat | 00000000 | 0x81800040: |
| 10_hsstx_ae_tap0_TUNE | 00000000 | |
| 0x81800044: 11_hsstx_ae_tap1_TUNE | 00000000 | 0x81800048: |
| 12_hsstx_ae_tap2_TUNE | 00000028 | |
| 0x8180004c: 13_hsstx_ae_tap3_TUNE | 00000000 | 0x81800054: |
| 15_hsstx_app_tune | 0000120e | |
| 0x81800058: 16_hsstx_analog_diag | 00000000 | 0x81800060: |
| 18_hsstx_4x_seg_app | 0000aafa | |
| 0x81800064: 19_hsstx_2x_seg_app | 00000000 | 0x81800068: |
| 1A_hsstx_1x_seg_app | 0000ff5d | |
| 0x8180006c: 1B_hsstx_seg_4x_term_app | 00000000 | 0x81800070: |
| 1C_hsstx_seg_2x1x_term_app | 00000f00 | |
| 0x81800074: 1D_hsstx_tap_sign_app | 0000000a | 0x81800078: |
| 1E_hsstx_ext_addr_data | 00000001 | |
| 0x8180007c: 1F_hsstx_ext_addr_addr | 00000000 | 0x81800080: |
| 20_hsstx_pat_buf_bytes_1_0 | 00000000 | |
| 0x81800084: 21_hsstx_pat_buf_bytes_3_2 | 00000000 | 0x81800088: |
| 22_hsstx_pat_buf_bytes_5_4 | 00000000 | |
| 0x8180008c: 23_hsstx_pat_buf_bytes_7_6 | 00000000 | 0x8180009c: |
| 27_hsstx_8023az_ctl | 00000000 | |
| 0x818000a0: 28_hsstx_dcc_ctl | 000060c0 | 0x818000a4: |

| | | | |
|---|----------|----------|-------------|
| 29_hsstx_dcc_ovrd | 00000000 | | |
| 0x818000a8: 2A_hsstx_dcc_app | | 00000083 | 0x818000ac: |
| 2B_hsstx_dcc_timeout | 0000ffff | | |
| 0x818000c0: 30_hsstx_tap_sign_ovrd | | 00000000 | 0x818000c8: |
| 32_hsstx_seg_4x_ovrd | 00000000 | | |
| 0x818000cc: 33_hsstx_seg_2x_ovrd | | 00000000 | 0x818000d0: |
| 34_hsstx_seg_1x_ovrd | 00000000 | | |
| 0x818000d8: 36_hsstx_tap_seg_4x_term_ovrd | | 00000000 | 0x818000dc: |
| 37_hsstx_tap_seg_2x_term_ovrd | 00000000 | | |
| 0x818000e0: 38_hsstx_tap_seg_1x_term_ovrd | | 00000000 | 0x818000ec: |
| 3B_hsstx_mac_test_ctl5 | 00000000 | | |
| 0x818000f0: 3C_hsstx_mac_test_ctl4 | | 00000000 | 0x818000f4: |
| 3D_hsstx_mac_test_ctl3 | 00000000 | | |
| 0x818000f8: 3E_hsstx_mac_test_ctl2 | | 00000000 | 0x818000fc: |
| 3F_hsstx_mac_test_ctl1 | 000000c6 | | |

HSS RX registers

=====

| | | | |
|---|----------|----------|-------------|
| 0x81800200: 00_hssrx_cfg_mode_PHY | | 00009e78 | 0x81800204: |
| 01_hssrx_test_ctl | 00000000 | | |
| 0x81800208: 02_hssrx_phs_rot_ctl | | 0000cb80 | 0x8180020c: |
| 03_hssrx_phs_rot_ofs_ctl | 00000610 | | |
| 0x81800210: 04_hssrx_phs_rot_posn1 | | 00000908 | 0x81800214: |
| 05_hssrx_phs_rot_posn2 | 00000039 | | |
| 0x81800218: 06_hssrx_phs_rot_sta_ofs1 | | 00000000 | 0x8180021c: |
| 07_hssrx_phs_rot_sta_ofs2 | 0000001f | | |
| 0x81800220: 08_hssrx_dfe_ctl_PHY | | 00002002 | 0x81800224: |
| 09_hssrx_dfe_smpl_snap1 | 00000000 | | |
| 0x81800228: 0A_hssrx_dfe_smpl_snap2 | | 00008000 | 0x8180022c: |
| 0B_hssrx_vga_ctl1 | 00004023 | | |
| 0x81800230: 0C_hssrx_vga_ctl2 | | 00007aa0 | 0x81800234: |
| 0D_hssrx_vga_ctl3 | 000009e4 | | |
| 0x81800238: 0E_hssrx_pwr_mgmt_ctl | | 0000001f | 0x8180023c: |
| 0F_hssrx_iqamp_ctl1 | 00000019 | | |
| 0x81800240: 10_hssrx_iqamp_ctl2 | | 00000004 | 0x81800244: |
| 11_hssrx_dacap_dacan_sel | 00000003 | | |
| 0x81800248: 12_hssrx_dacap_dacan | | 0000ffff | 0x8180024c: |
| 13_hssrx_daca_min | 00000000 | | |
| 0x81800250: 14_hssrx_adac_ctl | | 000000ff | 0x81800254: |
| 15_hssrx_ac_cp_ctl | 000031c3 | | |
| 0x81800258: 16_hssrx_ac_cp_val | | 00008049 | 0x8180025c: |
| 17_hssrx_dfe_h1h2h3_lcl_off_ch | 00000014 | | |
| 0x81800260: 18_hssrx_dfe_h1h2h3_lcl_off_val | | 00000000 | 0x81800264: |
| 19_hssrx_peaked_intg | 000000ff | | |
| 0x81800268: 1A_hssrx_cdr_analog_sw | | 0000ce00 | 0x8180026c: |
| 1B_hssrx_peaking_amp_init_c_PHY | 00000000 | | |
| 0x81800270: 1C_hssrx_dac_dpc | | 00000040 | 0x81800274: |
| 1D_hssrx_ddc | 00000000 | | |
| 0x81800278: 1E_hssrx_int_stat_PHY | | 00000c0f | 0x8180027c: |
| 1F_hssrx_dfe_func_ctl1_PHY | 0000ffff | | |
| 0x81800280: 20_hssrx_dfe_func_ctl2_INV | | 00007eff | 0x81800284: |
| 21_hssrx_ofs_ch_dcc_qcc_idx | 00002000 | | |
| 0x81800288: 22_hssrx_dfe_ofs_val | | 0000797f | 0x8180028c: |
| 23_hssrx_h_coeff_bist | 00000401 | | |

| | | |
|--|----------------|-------------|
| 0x81800290: 24_hssrx_ac_cap_bist | 000000d1 | 0x81800294: |
| 25_hssrx_max_gain_path_idx_res 00007800 | | |
| 0x81800298: 26_hssrx_loff_ctl | 00000054 | 0x8180029c: |
| 27_hssrx_sigdet_ctl 00002680 | | |
| 0x818002a0: 28_hssrx_ana_ctl_sw | 00000000 | 0x818002a4: |
| 29_hssrx_intg_dac_ofs 0000afe0 | | |
| 0x818002a8: 2A_hssrx_eye_ctl | 00000000 | 0x818002ac: |
| 2B_hssrx_eye_met 00000004 | | |
| 0x818002b0: 2C_hssrx_eye_met_err_cnt | 00000000 | 0x818002b4: |
| 2D_hssrx_eye_met_pdf_eyec 00000000 | | |
| 0x818002b8: 2E_hssrx_eye_met_pat_len | 0000007f | 0x818002bc: |
| 2F_hssrx_dfe_func_ctl3 0000dfff | | |
| 0x818002c0: 30_hssrx_dfe_tap_ctl_idx_ptr | 00000008 | 0x818002c4: |
| 31_hssrx_dfe_tap 00003030 | | |
| 0x818002c8: 32_hssrx_lte_ctl_TUNE | 00001601 | 0x818002e4: |
| 39_hssrx_int_stat2 000041ff | | |
| 0x818002e8: 3A_hssrx_ac_cpl_cur_src_adj | 00000040 | 0x818002ec: |
| 3B_hssrx_dcd_ctl 00007c4c | | |
| 0x818002f0: 3C_hssrx_dcc_ctl | 00000d00 | 0x818002f4: |
| 3D_hssrx_qcc_ctl 00006946 | | |
| 0x818002f8: 3E_hssrx_mac_test_ctl2 | 00000000 | 0x818002fc: |
| 3F_hssrx_mac_test_ctl1 00000000 | | |
| 0x81800248: 12_hssrx_dacap_dacan[02] | 00fd fffd | |
| 0x81800260: 18_hssrx_dfe_h1h2h3_lcl_off_va[00] | 0000 0000 0000 | |
| 0000 0000 0000 0000 0000 | | |
| 0x81800260: 18_hssrx_dfe_h1h2h3_lcl_off_va[08] | 0000 0000 0000 | |
| 0000 0000 0000 0000 0000 | | |
| 0x81800260: 18_hssrx_dfe_h1h2h3_lcl_off_va[16] | 0000 0000 0000 | |
| 0000 0000 | | |
| 0x81800288: 22_hssrx_dfe_ofs_val[00][00] | 797f 0100 0d7d | |
| 7f00 7a00 0000 | | |
| 0x81800288: 22_hssrx_dfe_ofs_val[03][00] | 7b08 0000 0106 | |
| 0000 7b7e 0000 | | |
| 0x81800288: 22_hssrx_dfe_ofs_val[06][00] | 7f05 0000 7b79 | |
| 0000 7f0b 007f | | |
| 0x81800288: 22_hssrx_dfe_ofs_val[09][00] | 7d7a 0000 0d04 | |
| 7f00 0501 7f00 | | |
| 0x81800288: 22_hssrx_dfe_ofs_val[12][00] | 7f7c 0000 0704 | |
| 7f00 0906 7f00 | | |
| 0x81800288: 22_hssrx_dfe_ofs_val[15][00] | 7d7b 0000 097e | |
| 7f00 047b 7f00 | | |
| 0x81800288: 22_hssrx_dfe_ofs_val[18][00] | 017d 0000 7b7d | |
| 0000 007b 0000 | | |
| 0x81800288: 22_hssrx_dfe_ofs_val[21][00] | 007b 0000 007b | |
| 0000 007b 0000 | | |
| 0x81800288: 22_hssrx_dfe_ofs_val[24][00] | 7c7f 0000 0200 | |
| 0000 7d01 0000 | | |
| 0x81800294: 25_hssrx_max_gain_path_idx_res[00] | 005c 084e 1101 | |
| 1896 2100 28b0 3096 3800 | | |
| 0x81800294: 25_hssrx_max_gain_path_idx_res[08] | 40d0 489a 5080 | |
| 5800 6040 6800 70f9 7800 | | |
| 0x818002c4: 31_hssrx_dfe_tap[00] | fffe 8080 0000 | |
| 0000 0030 0030 3030 3030 | | |
| 0x818002c4: 31_hssrx_dfe_tap[08] | 3030 3030 3030 | |

```

0000
0x818002e8: 3A_hssrx_ac_cpl_cur_src_adj[00]      0040 0040   0040
0040
0x818002ec: 3B_hssrx_dcd_ctl[00]                    7c4c 5c00   7c85
5c00   7c84
0x818002f0: 3C_hssrx_dcc_ctl[00]                    0d00 0d42   0d82
0d81
0x818002f4: 3D_hssrx_qcc_ctl[00]                    6986 6946

```

xfipcs, fec, aec, & aet registers

=====

```

0x81c00400: xfipcs_reg      [00] 00002040 00000080 00000000
00000000 00000001 00000008 00000000 00000000
0x81c00420: xfipcs_reg      [08] 00008c01 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c00440: xfipcs_reg      [16] 00000000 00000000 00000000
00000000 00000040 00000000 00000000 00000000
0x81c00460: xfipcs_reg      [24] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c00480: xfipcs_reg      [32] 00000004 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c00620: fec_32g_128g_reg [08] 00000000 00000000 00000000
00000000 00000000 00000000 00000000
0x81c00648: fec_32g_128g_reg [18] 00000000 00000000 00000000
00000000 00000000 00000000 00000000
0x81c00a00: aec_reg         [00] 00000000 00000000 00000000
00000000 00000000 00000000 00000000
0x81c00c00: aet_reg         [00] 00000000 00000000 00000000
00000000 00000000

```

bbc registers

=====

```

0x81c01800: bbc_trc      0 0 0 0 0 0 0
0
0x81c01840: bbc_trc      0 0 0 0 0 0 0
0
0x81c01880: bbc_trc      0 0 0 0 0 0 0
0
0x81c018c0: bbc_trc      0 0 0 0 0 0 0
0
0x81c01900: bbc_trc      0 0 0 0 0 0 0
0
0x81c01804: bbc_mbc      0 0 0 0 0 0 0
0
0x81c01844: bbc_mbc      0 0 0 0 0 0 0
0
0x81c01884: bbc_mbc      0 0 0 0 0 0 0
0
0x81c018c4: bbc_mbc      0 0 0 0 0 0 0
0
0x81c01904: bbc_mbc      0 0 0 0 0 0 0
0
0x81c01a00: bbc_rcc      0 0 0 0 0 0 0
0

```

| | | | | | | | |
|-------------------------------------|----------|---|---|---|---|----------------------|---|
| 0x81c01a20: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c01a40: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c01a60: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c01a80: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c01c00: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c01c20: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c01c40: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c01c60: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c01c80: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c01d00: bbc_fbpc | 00000000 | | | | | 0x81c01d04: bbc_csc | |
| 00000000 | | | | | | | |
| 0x81c01d08: bbc_rcc_inc | 00000000 | | | | | 0x81c01d0c: | |
| bbc_rqc_inc | 00000000 | | | | | | |
| 0x81c01d10: bbc_fbpc_inc | 00000000 | | | | | 0x81c01d14: | |
| bbc_tmc_inc | 00000000 | | | | | | |
| 0x81c01d18: bbc_threshold | 00080100 | | | | | 0x81c01d1c: | |
| bbc_counter_clr | 00000000 | | | | | | |
| 0x81c01d20: bbc_debug_en | 00000000 | | | | | 0x81c01d24: bbc_ctrl | |
| 00200020 | | | | | | | |
| 0x81c01d28: bbc_rqc_rcc_thresh | 00000055 | | | | | 0x81c01d34: | |
| bbc_bb_sc_n | 00000000 | | | | | | |
| 0x81c01d38: bbc_crd_reco_debug | 00000000 | | | | | 0x81c01d3c: | |
| bbc_crd_reco_debug_data | 00000000 | | | | | | |
| 0x81c01d40: bbc_multi_frm_loss_cnt | 00000000 | | | | | 0x81c01d44: | |
| bbc_multi_rdy_loss_cnt | 00000000 | | | | | | |
| 0x81c01d48: bbc_1frm_loss_recov_cnt | 00000000 | | | | | 0x81c01d4c: | |
| bbc_1rdy_loss_recov_cnt | 00000000 | | | | | | |
| 0x81c01d58: bbc_int_status | 00000000 | | | | | 0x81c01d5c: | |
| bbc_int_set | 00000000 | | | | | | |
| 0x81c01d60: bbc_int_first | 00000000 | | | | | 0x81c01d64: | |
| bbc_frm_rdy_rx_err_addr | 00000000 | | | | | | |
| 0x81c01d68: bbc_frm_rdy_tx_err_addr | 00000000 | | | | | 0x81c01d6c: | |
| bbc_trc_mbc_err_addr | 00000000 | | | | | | |
| 0x81c01d70: bbc_frm_rdy_rx_dbl_ecc | 00000000 | | | | | 0x81c01d74: | |
| bbc_frm_rdy_tx_dbl_ecc | 00000000 | | | | | | |
| 0x81c01d78: bbc_trc_mbc_dbl_ecc | 00000000 | | | | | | |
| 0x81c01d7c: bbc_fsm_status | 00001011 | | | | | 0x81c01d80: | |
| bbc_force_err | 00000000 | | | | | | |
| 0x81c01d84: bbc_crdt_avail0 | ffffffff | | | | | 0x81c01d88: | |
| bbc_crdt_avail1 | 000000ff | | | | | | |
| 0x81c01d8c: bbc_scratch | 00000000 | | | | | | |

FPS registers

=====

| | | | | | | | |
|---------------------------|----------|--|--|--|--|-------------|--|
| 0x81c00004: fps_er_enc_in | 00000000 | | | | | 0x81c00008: | |
|---------------------------|----------|--|--|--|--|-------------|--|

```

fps_er_crc          00000000
0x81c0000c: fps_er_trunc          00000000      0x81c00010:
fps_er_toolong     00000000
0x81c00014: fps_er_bad_eof        00000000      0x81c00018:
fps_er_enc_out     00000000
0x81c0001c: fps_er_bad_os         00000000      0x81c00020:
fps_er_flush       00000000
0x81c00024: fps_er_ifg            00000000      0x81c00038:
fps_er_crc_good_eof 00000000
0x81c0003c: fps_inv_arb            00000000      0x81c00040:
fps_slow_sts_status 00000000
0x81c00044: fps_tx_frm_cnt            00000000      0x81c00048:
fps_rx_frm_cnt     00000000
0x81c00050: fps_tx_word_cnt_hi          00000000      0x81c0004c:
fps_tx_word_cnt_lo 00000000
0x81c00058: fps_rx_word_cnt_hi          00000000      0x81c00054:
fps_rx_word_cnt_lo 00000000

```

BAL registers

=====

```

0x81c07000: bal_desired_buf          00000000      0x81c07004:
bal_alloc_buf      00000000
0x81c07008: bal_busy_buf              00000000      0x81c0700c:
bal_usable_buf     00000000
0x81c07010: bal_max_bor_buf          00000000
0x81c07014: bal_busy_buf_thresh      00000002

```

TXQ registers

=====

```

0x81c03004: txq_phys_port_ctl        00400000
0x81c03050: txq_link_skew            00000000
0x81c03068: txq_cr_lk_dttm_intr_sts [00] 00000000 00000000
0x81c03070: txq_cr_lk_dttm_intr_en [00] 00000000 00000000
0x81c03024: txq_disc_frm_trap_cnt    00000014

```

FDS registers

=====

```

0x81c04000: fds_rxf_ctl              00000002      0x81c04004:
fds_rxf_wait_thresh 00000909
0x81c04018: fds_rxf_first_error      00000000      0x81c0401c:
fds_rxf_first_error_info 00000000
0x81c04020: fds_rxf_inout_pkt_cnt    00000000
0x81c04008: fds_rxf_err_int_status   00000000      0x81c04024:
fds_rxf_fifo_status 00888888
0x81c05000: fds_txf_ctl              0000003a      0x81c05004:
fds_txf_wait_ifg_thresh 00a00106
0x81c05008: fds_txf_err_int_status   00000000      0x81c05024:
fds_txf_fifo_status 00088888
0x81c0502c: fds_txf_bbc_scs         00000000

```

Logical TXQ registers

=====

```

0x81c03000: txq_log_port_ctl        00000002      0x81c03008:
txq_port_status     00000000

```

```

0x81c0300c: txq_todo_flags [00] 00000000 00000000
0x81c03014: txq_spd_match_desc [00] 00000000 00000000 00000000
00000000
0x81c03024: txq_spd_match_desc [04] 00000014
0x81c03028: txq_vc_weight [00] 01010101 01010101 01010101
01010101
0x81c03038: txq_vc_weight [04] 01010101 01010101 01010101
01010101
0x81c03048: txq_vc_weight [08] 01010101 00010101
0x81c03054: txq_cong_dttn_ctrl 00000000
0x81c03058: txq_cong_dttn_intr_sts [00] 00000000 00000000
0x81c03060: txq_cong_dttn_intr_en [00] 00000000 00000000
0x81c03078: txq_bw_limit_en_reg [00] 00000000 00000000
0x81c03080: txq_bw_gua_en_reg [00] 00000000 00000000
0x81c03088: txq_vc_group [00] 03030300 03030303 03030303
03030303
0x81c03098: txq_vc_group [04] 03030303 03030303 03030303
03030303
0x81c030a8: txq_vc_group [08] 03030303 03030303 00000000
00000000
0x81c030b0: txq_bw_thresh_group [00] 00000000 00000000 00000000
00000000
0x81c030c0: txq_bw_thresh_group [04] 00000000 00000000 00000000
00000000
0x81c030d0: txq_bw_thresh_group [08] 00000000 00000000 00000000
00000000
0x81c030e0: txq_bw_thresh_group [12] 00000000 00000000 00000000
00000000
0x81c030f0: txq_bw_thresh_group [16] 00000000 00000000 00000000
00000000
0x81c03100: txq_bw_thresh_group [20] 00000000 00000000 00000000
00000000
0x81c03110: txq_bw_thresh_group [24] 00000000 00000000 00000000
00000000
0x81c03120: txq_bw_thresh_group [28] 00000000 00000000 00000000
00000000
0x81c03130: txq_bw_thresh_group [32] 00000000 00000000 00000000
00000000
0x81c03140: txq_bw_thresh_group [36] 00000000 00000000 00000000
00000000

```

txq Congestion detection Statistics RAM

```

=====
0x81090000: vc[0] 00000000 0x81090004: vc[1]
00000000
0x81090008: vc[2] 00000000 0x8109000c: vc[3]
00000000
0x81090010: vc[4] 00000000 0x81090014: vc[5]
00000000
0x81090018: vc[6] 00000000 0x8109001c: vc[7]
00000000
0x81090020: vc[8] 00000000 0x81090024: vc[9]
00000000
0x81090028: vc[10] 00000000 0x8109002c: vc[11]

```

```

00000000
0x81090030: vc[12]      00000000      0x81090034: vc[13]
00000000
0x81090038: vc[14]      00000000      0x8109003c: vc[15]
00000000
0x81090040: vc[16]      00000000      0x81090044: vc[17]
00000000
0x81090048: vc[18]      00000000      0x8109004c: vc[19]
00000000
0x81090050: vc[20]      00000000      0x81090054: vc[21]
00000000
0x81090058: vc[22]      00000000      0x8109005c: vc[23]
00000000
0x81090060: vc[24]      00000000      0x81090064: vc[25]
00000000
0x81090068: vc[26]      00000000      0x8109006c: vc[27]
00000000
0x81090070: vc[28]      00000000      0x81090074: vc[29]
00000000
0x81090078: vc[30]      00000000      0x8109007c: vc[31]
00000000
0x81090080: vc[32]      00000000      0x81090084: vc[33]
00000000
0x81090088: vc[34]      00000000      0x8109008c: vc[35]
00000000
0x81090090: vc[36]      00000000      0x81090094: vc[37]
00000000
0x81090098: vc[38]      00000000      0x8109009c: vc[39]
00000000

```

Logical STS registers

=====

```

0x81584084: sts_ftb_type1_miss      00000000
0x81584088: sts_ftb_type2_miss      00000000
0x8158408c: sts_ftb_type6_miss      00000000
0x81584090: sts_hard_zoning_miss    00000000
0x81584094: sts_lun_zoning_miss     00000000
0x8158409c: sts_unroutable          00000000
0x815810b4: sts_rte_cl2              00000000      0x815810b8:
sts_rte_cl3              00000000      0x815810bc: sts_rte_link_ctl
00000000      0x815840a8: sts_tx_timeout      00000000

```

Logical STS filter registers

=====

```

0x81584000: stsflt_trig      [00] 00000000 00000000 00000000
00000000
0x81584010: stsflt_trig      [04] 00000000 00000000 00000000
00000000
0x81584020: stsflt_trig      [08] 00000000 00000000 00000000
00000000
0x81584030: stsflt_trig      [12] 00000000 00000000 00000000
00000000
0x81584040: stsflt_trig      [16] 00000000 00000000 00000000

```

```

00000000
0x81584050: stsflt_trig [20] 00000000 00000000 00000000
00000000
0x81584060: stsflt_trig [24] 00000000 00000000 00000000
00000000
0x81584070: stsflt_trig [28] 00000000 00000000 00000000
00000000
0x81584080: stsflt_trig [32]

```

Logical STS discard registers

=====

```

0x81581000: disc_mcast_wka 00000000 0x81581004:
disc_inv_did 00000000
0x81581008: disc_cl1_cl4 00000000 0x8158100c:
disc_sid_chk_fail 00000000
0x81581010: disc_inv_dom_egid_txpt 00000000 0x81581014:
disc_vft_hop_cnt_1 00000000
0x81581018: disc_classf 00000000 0x8158101c:
disc_fcp_cdb_inv 00000000
0x81581020: disc_vfid_trap_enabled 00000000 0x81581024:
disc_vfid_hdr_chk_fail 00000000
0x81581028: disc_shim_cksum_fail 00000000 0x8158102c:
disc_fed_edit_cmd_err 00000000
0x81581030: disc_ftb_vm_mode 00000000 0x81581034:
disc_ftb_agnt2_miss 00000000
0x81581038: disc_ecb_reserved 00000000 0x8158103c:
disc_ecb_de_pad_err 00000000
0x81581040: disc_ecb_de_tag_err 00000000 0x81581044:
disc_ecb_de_seq_err 00000000
0x81581048: disc_ecb_err 00000000 0x8158104c:
disc_ftb_type4_match 00000000
0x81581050: disc_fcp_rsp_ftb_type4 00000000 0x81581054:
disc_ftb_type5_match 00000000
0x81581058: disc_ftb_type3_match 00000000 0x8158105c:
disc_els_ftb_type3 00000000
0x81581060: disc_ftb_type1_match 00000000 0x81581064:
disc_els_rsp_ex_port 00000000
0x81581068: disc_inv_drp_dps 00000000 0x8158106c:
disc_did_lookup_miss 00000000
0x81581070: disc_ftb_type2_match 00000000 0x81581074:
disc_trpd_plogi_pdisc 00000000
0x81581078: disc_type2_lookup_miss 00000000 0x8158107c:
disc_ftb_type6_match 00000000
0x81581080: disc_els_rep_ex_port 00000000 0x81581084:
disc_els_sid_lkup_bit1 00000000
0x81581088: disc_els_sid_lkup_bit0 00000000 0x8158108c:
disc_bls_frm_trap_bit1 00000000
0x81581090: disc_ftb_token_err 00000000 0x81581094:
disc_asic_internal_err 00000000
0x81581098: disc_hard_zone_miss 00000000 0x8158109c:
disc_lun_zone_miss 00000000
0x815810a0: discflt_frame_disc 00000000 0x815810a4:
discflt_parity_err 00000000
0x815810a8: disc_frame_marked_du 00000000 0x815810ac:

```

```
disc_frame_marked_to 00000000
0x815810b0: disc_lkup_rte_prty_err 00000000
```

```
portstatsshow 56
```

```

stat_wtx          0          4-byte words transmitted
stat_wrx          0          4-byte words received
stat_ftx          0          Frames transmitted
stat_frx          0          Frames received
stat_c2_frx       0          Class 2 frames received
stat_c3_frx       0          Class 3 frames received
stat_lc_rx        0          Link control frames
received
stat_mc_rx        0          Multicast frames
received
stat_mc_to        0          Multicast timeouts
stat_mc_tx        0          Multicast frames
transmitted
tim_txcrd_z       0          Time TX Credit Zero
(2.5Us ticks)
tim_txcrd_z_vc   0- 3: 0          0          0          0
tim_txcrd_z_vc   4- 7: 0          0          0          0
tim_txcrd_z_vc   8-11: 0         0          0          0
tim_txcrd_z_vc  12-15: 0         0          0          0
lat_tot_pkt_vc   0- 3: 1          1          1          1
lat_tot_pkt_vc   4- 7: 1          1          1          1
lat_tot_pkt_vc   8-11: 1          1          1          1
lat_tot_pkt_vc  12-15: 1          1          1          1
lat_hi_time_vc   0- 3: 0          0          0          0
lat_hi_time_vc   4- 7: 0          0          0          0
lat_hi_time_vc   8-11: 0          0          0          0
lat_hi_time_vc  12-15: 0          0          0          0
lat_lo_time_vc   0- 3: 1          1          1          1
lat_lo_time_vc   4- 7: 1          1          1          1
lat_lo_time_vc   8-11: 1          1          1          1
lat_lo_time_vc  12-15: 1          1          1          1
max_latency_vc   0- 3: 1          1          1          1
max_latency_vc   4- 7: 1          1          1          1
max_latency_vc   8-11: 1          1          1          1
max_latency_vc  12-15: 1          1          1          1
latency_dma_ts   09-09-2024 UTC Mon 08:47:26          TXQ
Latency DMA TimeStamp
fec_cor_detected 0          Count of blocks that
were corrected by FEC
fec_uncor_detected 0          Count of blocks that
were left uncorrected by FEC
er_enc_in        0          Encoding errors inside
of frames
er_crc           0          Frames with CRC errors
er_trunc         0          Frames shorter than
minimum
er_toolong       0          Frames longer than
maximum
er_bad_eof       0          Frames with bad end-of-
```



```

frame
er_enc_out          0          Encoding error outside
of frames
er_bad_os           0          Invalid ordered set
er_pcs_blk          0          PCS block errors
er_rx_c3_timeout    0          Class 3 receive frames
discarded due to timeout
er_tx_c3_timeout    0          Class 3 transmit frames
discarded due to timeout
er_unroutable       0          Frames that are
unroutable
er_unreachable      0          Frame with unreachable
destination
er_other_discard    0          Other discards
er_type1_miss       0          frames with FTB type 1
miss
er_type2_miss       0          frames with FTB type 2
miss
er_type6_miss       0          frames with FTB type 6
miss
er_zone_miss        0          frames with hard zoning
miss
er_lun_zone_miss    0          frames with LUN zoning
miss
er_crc_good_eof     0          Crc error with good eof
er_inv_arb          0          Invalid ARB
er_single_credit_loss 0          Single vcrdy/frame loss
on link
er_multi_credit_loss 0          Multiple vcrdy/frame
loss on link
other_credit_loss   0          Link timeout/complete
credit loss
phy_stats_clear_ts   09-06-2024 UTC Fri 08:30:19   Timestamp of
phy_port stats clear
lgc_stats_clear_ts   09-06-2024 UTC Fri 08:30:19   Timestamp of
lgc_port stats clear
fec_corrected_rate   0          FEC Corrected blocks per
second

```

portstats64show 56

```

stat64_wtx          0          top_int : 4-byte words transmitted
bottom_int : 4-byte words transmitted
stat64_wrx          0          top_int : 4-byte words received
bottom_int : 4-byte words received
stat64_ftx          0          top_int : Frames transmitted
bottom_int : Frames transmitted
stat64_frx          0          top_int : Frames received
bottom_int : Frames received
stat64_c2_frx       0          top_int : Class 2 frames received
bottom_int : Class 2 frames received
stat64_c3_frx       0          top_int : Class 3 frames received
bottom_int : Class 3 frames received
stat64_lc_rx        0          top_int : Link control frames received
bottom_int : Link control frames

```

| | | | |
|---|---|------------|--------------------------------|
| received | | | |
| stat64_mc_rx | 0 | top_int | : Multicast frames received |
| | 0 | bottom_int | : Multicast frames received |
| stat64_mc_to | 0 | top_int | : Multicast timeouts |
| | 0 | bottom_int | : Multicast timeouts |
| stat64_mc_tx | 0 | top_int | : Multicast frames transmitted |
| | 0 | bottom_int | : Multicast frames |
| transmitted | | | |
| tim64_rdy_pri | 0 | top_int | : Time R_RDY high priority |
| | 0 | bottom_int | : Time R_RDY high priority |
| tim64_txcrd_z | 0 | top_int | : Time BB_credit zero |
| | 0 | bottom_int | : Time BB_credit zero |
| er64_enc_in | 0 | top_int | : Encoding errors inside of |
| frames | 0 | bottom_int | : Encoding errors inside of |
| frames | | | |
| er64_crc | 0 | top_int | : Frames with CRC errors |
| | 0 | bottom_int | : Frames with CRC errors |
| er64_trunc | 0 | top_int | : Frames shorter than minimum |
| | 0 | bottom_int | : Frames shorter than minimum |
| er64_toolong | 0 | top_int | : Frames longer than maximum |
| | 0 | bottom_int | : Frames longer than maximum |
| er64_bad_eof | 0 | top_int | : Frames with bad end-of-frame |
| | 0 | bottom_int | : Frames with bad end-of- |
| frame | | | |
| er64_enc_out | 0 | top_int | : Encoding error outside of |
| frames | 0 | bottom_int | : Encoding error outside of |
| frames | | | |
| er64_disc_c3 | 0 | top_int | : Class 3 frames discarded |
| | 0 | bottom_int | : Class 3 frames discarded |
| er64_pcs_blk | 0 | top_int | : PCS block errors |
| | 0 | bottom_int | : PCS block errors |
| stat64_rateTxFrame | 0 | | Tx frame rate (fr/sec) |
| stat64_rateRxFrame | 0 | | Rx frame rate (fr/sec) |
| stat64_rateTxPeakFrame | 0 | | Tx peak frame rate (fr/sec) |
| stat64_rateRxPeakFrame | 0 | | Rx peak frame rate (fr/sec) |
| stat64_rateTxWord | 0 | | Tx Word rate (words/sec) |
| stat64_rateRxWord | 0 | | Rx Word rate (words/sec) |
| stat64_rateTxPeakWord | 0 | | Tx peak Word rate (words/sec) |
| stat64_rateRxPeakWord | 0 | | Rx peak Word rate (words/sec) |
| stat64_PRJTframes | 0 | top_int | : Number of PRJT frames |
| returned to this port | 0 | bottom_int | : Number of PRJT |
| frames returned to this port | | | |
| stat64_PBSYframes | 0 | top_int | : Number of PBSY frames |
| returned to this port | 0 | bottom_int | : Number of PBSY |
| frames returned to this port | | | |
| stat64_inputBuffersFull | 0 | top_int | : Number of occurrences |
| when all input buffers full | 0 | bottom_int | : Number of |
| occurrences when all input buffers full | | | |
| stat64_rxClass1Frames | 0 | top_int | : Number of class 1 |

```

frames received          0          bottom_int : Number of class 1
frames received
stat64_aveTxFrameSize  0          Average Tx Frame size
stat64_aveRxFrameSize  0          Average Rx Frame size
Lr_in                   0          top_int
                        0          bottom_int
Ols_in                  0          top_int
                        0          bottom_int
Lr_out                   0          top_int
                        0          bottom_int
Ols_out                  0          top_int
                        0          bottom_int
Link_failure            0          top_int
                        0          bottom_int
Invalid_CRC             0          top_int
                        0          bottom_int
Invalid_word            0          top_int
                        0          bottom_int
Protocol_err            0          top_int
                        0          bottom_int
Loss_of_sig              0          top_int
                        0          bottom_int
Loss_of_sync            0          top_int
                        0          bottom_int
er_bad_os                0          top_int : Invalid ordered set
                        0          bottom_int: Invalid ordered set

```

```

portrouteshow 56
port address ID: 0x013800
external unicast routing table:
  0: Embedded
 255: Embedded
internal unicast routing table:
  0: Embedded

```

portcamshow 56

```

-----
Port  SID used  DID used  SID entries  DID entries
56    0         0         000000     000000
-----

```

ptbufshow, ptcreditshow, ptdatashow, ptstatsshow 56

```

S:
S:VF Enable:          1
S:
S:C4 Global Variable:
S:-----
-----
S:trace_stop:        0
S:
S:C4 Phy Data Pointers: c4_phyp = 0xb6ab0000
S:-----

```

```

-----
S:tnodep                0xbb828c40      pt
    0x43028000
S:proto_phyph          0xb8804900      phy_cfg
0xb6ab1040
S:c4_chp                0x97e28000      c4_lgcp
0x97f48000
S:c4_phy_regp          0x81c00000      proc_dir
0xb8510c80
S:-----
-----
S:magic_id              0xc4345678      num_port_timer    12
S:prev_if_id            0x43020000      S:ftx              0
    tov              0
S:initialized           0                port_idx            0
S:ui_idx                56              slot_no
    0
S:blade_idx             0                sw_usr_ports        400
S:unused                0                intr_debounced
    0
S:aec_status            0x0              reason_code
    0
S:debug                 0x00000004      debug_trc_line     0
S:rxbuf_list_head       0xffffffff      rxbuf_list_tail
0xffffffff
S:isAePort              0                port_misc_data
    0
S:num_fault1_rx_disc    0                num_fault2_rx_disc 0
S:p_lli_cause0          0                p_sig_regained     0
S:p_sync_regained       0                enc_out
    0x0
S:cached_fps_status     0                cached_sts_status  0
S:cached_er_crc_good_eof 0
S:cached_er_bad_os      0                cached_er_too_long 0
S:cached_er_trunc       0
cached_tot_er_crc_good_eof 0
S:num_pt_excess_intr    0                num_no_fid          0
S:num_fault1_cnt        0                num_fault2_cnt
    0
S:num_fault_lip         0                num_fault_lli       0
S:num_fault_rx_fifo     0                num_fault_hss       0
S:num_fault_bwait       0                lli_intr_prim
    0
S:num_sw_link_to        0
be_link_err_mon_count   0
S:ecb_enc_enabled       0                ecb_comp_enabled
    0
S:ecb_rsv_enc           0                ecb_rsv_comp        0
S:ecb_enc_bm            0x0              ecb_key_index
0xffffffff
S:fab_idx               4
S:num_be_lto            0                lto_count_reset_intvl
    0
S:lr_count_reset_intvl 0                num_be_lr

```

```

      0
S:num_fault_qsfp          0          check_lto
      0
S:credit_loaded          0          num_credit_overrun
      0
S:fec_enabled            0x0          fec_los_to_flag          0x0
S:phy_stats_clear_ts      1725611419    pcs_err_online
      0
S:pcs_err_light_det      0          pcs_err_ignore
      0
S:pcs_blk_err            0          pcs_hiber          0
S:phy_port_status        0          ecb_enc_lr_count
      0
S:dport_mode              0          avoid_lto_det          0
S:sn_debounced           0x0          sn_started_kr_reqd      0
S:major_timer_started     0x0          ready_bm          0x0
S:parln_1_bm              0x0          parln_0_bm          0x0
S:be_los_of_sync_event_intvl 0
be_los_of_sync_event      0
S:errataPtenable_cntr    0          errataPoll_cntr
      0
S:jda_rx_sig_loss_det    0          jda_rx_sig_loss_cnt
      0
S:encrypt_blk_error      0
S:
S:      c4_trunk
S:=====
S:mark_ts                0x0          deskew          0x0
S:master_phyp            0x0
S:
S:adelay[00]: 0x00000000 0x00000000 0x00000000 0x00000000
S:adelay[04]: 0x00000000 0x00000000 0x00000000 0x00000000
S:
S:      c4_buf
S:=====
S:tx_csc                  0          rx_csc
      0
S:ld_vc_credits           0          tx_flag          0x0
S:alloc_buffers           0          req_buffers          0
S:est_buffers             20          ld_use_est          0
S:bb_sc_n                 0          rx_bb_sc_n
      0
S:data_cr                 5          nondata_cr
      6
S:cr_enable               0
S:ld_nondata_cr           6          tnodep
0xbb828d20
S:tx_credits[0] 0 0 0 0 0 0 0 0
S:tx_credits[8] 0 0 0 0 0 0 0 0
S:tx_credits[16] 0 0 0 0 0 0 0 0 0 0
S:tx_credits[24] 0 0 0 0 0 0 0 0 0 0
S:tx_credits[32] 0 0 0 0 0 0 0 0 0 0
S:rx_credits[0] 0 0 0 0 0 0 0 0
S:rx_credits[8] 0 0 0 0 0 0 0 0

```

```

S:rx_credits[16]      0    0    0    0    0    0    0    0    0
S:rx_credits[24]      0    0    0    0    0    0    0    0    0
S:rx_credits[32]      0    0    0    0    0    0    0    0    0
S:tx_mbc[0]           0    0    0    0    0    0    0    0    0
S:tx_mbc[8]           0    0    0    0    0    0    0    0    0
S:tx_mbc[16]          0    0    0    0    0    0    0    0    0
S:tx_mbc[24]          0    0    0    0    0    0    0    0    0
S:tx_mbc[32]          0    0    0    0    0    0    0    0    0
S:rx_mbc[0]           0    0    0    0    0    0    0    0    0
S:rx_mbc[8]           0    0    0    0    0    0    0    0    0
S:rx_mbc[16]          0    0    0    0    0    0    0    0    0
S:rx_mbc[24]          0    0    0    0    0    0    0    0    0
S:rx_mbc[32]          0    0    0    0    0    0    0    0    0

```

S:

S:C4 Chip Variables: c4_phyp->c4_chp = 0x97e28000

S:-----

S:version = 2.1

S:magic_id 0xc4234567 init_state 0x8

S:reset_reg_mem 0x1

S:ch_int0_en_bm 0x0 intr0_cause 0x0

S:ch_int1_en_bm 0x0 intr1_cause 0x0

S:ch_int2_en_bm 0x0 intr2_cause 0x0

S:ch 0x43010080 ch_cfg

0xb7013ba0

S:raslog_hdl.hndl 0x0 obj_halted 0x0

S:c4_chip_regp 0x80000000 c4_fpg_regp

0x81800000

S:num_chip_timer 0x5

S:hi_task_bm 0x0 lo_task_bm 0x0

S:c4_deferq.q_head 0x0 c4_deferq.q_tail 0x0

S:c4_tmrq.q_head 0x0 c4_tmrq.q_tail 0x0

slot_no 0

S:chip_inst 0 chip_idx 0

S:pll_initialized 1

pll_serdes_initialized 1

S:init_tries 0 init_ptEnableBM

0xba01b488

S:tick_polling 0xb980c9c0 sec_polling

0xb980c960

S:bb_fid 129

S:ecb_key_bm[0] 0x0 ecb_key_bm[1] 0x0

S:ecb_key_bm[2] 0x0 ecb_key_bm[3] 0x0

S:is_chip_enc_enabled 0

is_chip_comp_enabled 0x0

S:ftb_rsrcp->ftb_flags 0x0 act_rsrcp->act_flag 0x1

S:lue_rsrcp->lue_flags[0] 0x0 lue_rsrcp-

>lue_flags[1] 0x0

S:c4_phyp[00]: 0xb6ab0000 0xb6ab2080 0xb6ab4100 0xb6ab6180

S:c4_phyp[04]: 0xb6ab9040 0xb6abb0c0 0xb6abd140 0xb6ac0000

S:c4_phyp[08]: 0xb6ac2080 0xb6ac4100 0xb6ac6180 0xb6ac9040

S:c4_phyp[12]: 0xb6acb0c0 0xb6acd140 0xb6ad0000 0xb6ad2080

S:c4_phyp[16]: 0xb6ad4100 0xb6ad6180 0xb6ad9040 0xb6adb0c0

S:c4_phyp[20]: 0xb6add140 0xb6ae0000 0xb6ae2080 0xb6ae4100

```

S:c4_phyp[24]: 0xb6ae6180 0xb6ae9040 0xb6aeb0c0 0xb6aed140
S:c4_phyp[28]: 0xb6af0000 0xb6af2080 0xb6af4100 0xb6af6180
S:c4_phyp[32]: 0xb6af9040 0xb6afb0c0 0xb6afd140 0xb6b00000
S:c4_phyp[36]: 0xb6b02080 0xb6b04100 0xb6b06180 0xb6b09040
S:c4_phyp[40]: 0xb6b0b0c0 0xb6b0d140 0xb6b10000 0xb6b12080
S:c4_phyp[44]: 0xb6b14100 0xb6b16180 0xb6b19040 0xb6b1b0c0
S:c4_phyp[48]: 0xb6b1d140 0xb6b20000 0xb6b22080 0xb6b24100
S:c4_phyp[52]: 0xb6b26180 0xb6b29040 0xb6b2b0c0 0xb6b2d140
S:c4_phyp[56]: 0xb6b30000 0xb6b32080 0xb6b34100 0xb6b36180
S:c4_phyp[60]: 0xb6b39040 0xb6b3b0c0 0xb6b3d140 0xb6b40000
S:c4_lgcp[00]: 0x97f48000 0x97f4c000 0x97f50000 0x97f54000
S:c4_lgcp[04]: 0x97f58000 0x97f5c000 0x97f60000 0x97f64000
S:c4_lgcp[08]: 0x97f68000 0x97f6c000 0x97f70000 0x97f74000
S:c4_lgcp[12]: 0x97f78000 0x97f7c000 0x97f80000 0x97f84000
S:c4_lgcp[16]: 0x97f88000 0x97f8c000 0x97f90000 0x97f94000
S:c4_lgcp[20]: 0x97f98000 0x97f9c000 0x97fa0000 0x97fa4000
S:c4_lgcp[24]: 0x97fa8000 0x97fac000 0x97fb0000 0x97fb4000
S:c4_lgcp[28]: 0x97fb8000 0x97fbc000 0x97fc0000 0x97fc4000
S:c4_lgcp[32]: 0x97fc8000 0x97fcc000 0x97fd0000 0x97fd4000
S:c4_lgcp[36]: 0x97fd8000 0x97fdc000 0x97fe0000 0x97fe4000
S:c4_lgcp[40]: 0x97fe8000 0x97fec000 0x97ff0000 0x97ff4000
S:c4_lgcp[44]: 0x97ff8000 0x97ffc000 0x8e000000 0x8e004000
S:c4_lgcp[48]: 0x8e008000 0x8e00c000 0x8e010000 0x8e014000
S:c4_lgcp[52]: 0x8e018000 0x8e01c000 0x8e020000 0x8e024000
S:c4_lgcp[56]: 0x8e028000 0x8e02c000 0x8e030000 0x8e034000
S:c4_lgcp[60]: 0x8e038000 0x8e03c000 0x8e040000 0x8e044000
S:chip_timers[00]: 0xb980c720 0xb980c780 0xb980c7e0 0xb980c840
S:chip_timers[04]: 0xb980c8a0 0xb980c900
S:disc_trap_enable_required      0x0          rxlp_disc_log_stop
      0x0
S:curr_rxlp_frm_cnt      0x0          curr_rxlp_disc_frm_cnt  0x0
S:sw_disc_frm_cnt      0x0          last_disc_frm_cnt      0x0
S:txq_nopop_pr_cnt      0x0          pollErrataDfe_ptBM
0xba01b4b0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][0]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][1] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][2]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][0] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][1]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][2] 0x0
S:
S:C4 Logical Port Variables
S:-----
-----
S:c4_lgc_regp      0x81c00000
S:c4_phyp:
S:      0xb6ab0000      0x0          0x0          0x0

S:      0x0          0x0          0x0          0x0

S:master_phyp      0xb6ab0000      if_id
0x43020000
S:min_phyp      0x0          max_phyp      0x0
S:num_phy_ports      1          lgc_num      0

```

```

S:num_iu_to          0          sw_txq_bm
  0
S:port_fid          129          unused          0
S:port_group        0          lgc_stats_clear_ts
  1725611419
S:domain_tbl_sel    0          area_tbl_sel
  0
S:egid_tbl_sel      0
S:serv_lo_bm        0x0
S:
S:Proto Phy Variables:
S:-----
-----
S:magic_id          0xc4123456    asic_phyp
0xb6ab0000
S:port_id           0x43028000    phy_cfg
  0xb6ab1040
S:upsm_hdl          0xb800ddc0    physm_hdl
0xb800db40
S:ov_snsn_hdl       0xb800da00    sw_snsn_hdl
0xb800daa0
S:ov_lksm_hdl       0xb800dbe0    sw_lksm_hdl
0xb800dc80
S:trksm_hdl         0xb800dd20    lr_flag          0x0
S:lr_active         0x0          qsfp_txrx_rate_sel
  0x0
S:
S:UPSM             UP00: UPST_PORT_DISABLED    --> UP00: UPST_PORT_DISABLED
S:SNSM(OV)         SN00: OV_SNST_STOPPED        --> SN00: OV_SNST_STOPPED
S:SNSM(SW)         SW00: SW_SNST_STAGE_WS    --> SW00: SW_SNST_STAGE_WS
S:PHYSM            PP00: PHYST_STOPPED        --> PP00: PHYST_STOPPED
S:LKSM(OV)         LK00: OV_LKST_INACTIVE    --> LK00: OV_LKST_INACTIVE
S:LKSM(SW)         SW13: INACTIVE          --> SW13: INACTIVE
S:TRKSM           TRK0: TRKST_INIT          --> TRK0: TRKST_INIT
S:
S:physm variables:
S:-----
-----
S:proto_phyp        0xb8804900    physm_hdl
0xb800db40
S:force_offline     0          copper          0
S:fault_reason      0: UNKNOWN
S:phy_media_present 0
S:
S:snsn variables:
S:-----
-----
S:speed             0xff          proto_phyp
0xb8804900
S:hw_sn_tries_left  0x0          sw_sn_tries_left    0x0
S:curr_txsp_count   0x0
S:tx_max            0x0          curr_tx_indx
  0x0
S:curr_tx           0x0          curr_rxsp_count

```



```

    0x0
S:rx_max                0x0                curr_rx_indx
    0x0
S:curr_rx               0x0                rx_mem
    0x0
S:rxsp_rec_count       0x0
S:nc_start              0x0                tx_start                0x0
S:sync_start           0x0                sync_present            0x0
S:diag_auto            0x0                diag_speed              0xff
S:striped_wd_tov       3000                hw_wd_tov
    3000
S:step                  0x0                qsfp28_speed_mode
    0x0
S:qsfp_mode0_hw_sn_tries_left  0x0
S:qsfp_mode1_hw_sn_tries_left  0x0
S:
S:lksm variables:
S:-----
-----
S:proto_phyp           0xb8804900        ov_lksm_hdl
0xb800dbe0
sw_lksm_hdl            0xb800dc80
num_lf1                0
S:hw_link_tries_left   0                sw_link_tries_left     0
S:buf_ptype            0x0                stored_entry_state     0x6
S:handshake_owner      0x0                mark_unsent
    0x0
S:busybuf_stuck        0x0                lr_wait                0x0
S:
S:trksm variables:
S:-----
-----
S:Not a trunk port
S:
S:upsm variables:
S:-----
-----
S:proto_phyp           0xb8804900        upsm_hdl
0xb800ddc0
S:bb_credits           0                port_beacon            0
S:port_diag_flag       0                force_offline
    0
S:port_fault_rsn       0: PORT_NO_FAULT
S:retry_init_rsn       0: UNKNOWN
S:linit_reason         0                linit_result           0
S:ie_fctl_mode         0                fec_in_sync_tries_left 0
S:retry_sn_fail_init   0
retry_link_fail_init   0
S:excess_lr_count      0
S:
S:c4_ch_cfg
S:-----
-----
S:c4_desc_ring_size    256                292                256                256                292

```

```

292      2      292      292
S:thresh_def          0      16      1      0
S:intr_tries          500      cmem_pattern
0xdeadbeef
S:cmem_pattern_upwd   2      cmem_init_time      16
S:cmem_init_tries    5
S:ctrl_par_thresh    2      data_par_thresh
4
S:cam_par_thresh     4      buf_loss_thresh
12
S:crit_par_thresh    2      non_crit_par_thresh
6
S:pci_abort_thresh   10      pci_err_thresh      5
S:excess_chintr_thresh 8      sw_err_thresh      20
S:err_sample_period  300      intr_sleep
20000
S:frame_timeout      2500      proxy_dev      16384
S:vf_route           81920      qos      2048
S:stats 2048      f_redirect      2048
S:rsp_trap           2048      lun_zoning      20480
S:area_mode          0      ftb_max_loop[0]  0
S:ftb_max_loop[1]    6      ftb_max_loop[2]    9
S:ftb_max_loop[3]    10     ftb_max_loop[4]    10
S:ftb_max_loop[5]    5      ftb_max_loop[6]    6
S:ftb_seg_size[0]    0      ftb_seg_size[1]
16384
S:ftb_seg_size[2]    65536     ftb_seg_size[3]
16384
S:ftb_seg_size[4]    16384     ftb_seg_size[5]
65536
S:ftb_seg_size[6]    16384     ftb_seg_base[0]    0
S:ftb_seg_base[1]    0      ftb_seg_base[2]
65536
S:ftb_seg_base[3]    16384     ftb_seg_base[4]
32768
S:ftb_seg_base[5]    131072    ftb_seg_base[6]
49152
asic_err_monitor_period1 300
asic_err_monitor_period2 86400
zone_chk_to_poll_period 25
zone_chk_class2_reject_tov
S:
S:c4_phy_cfg

```

```

S:version = 2.1
S:pt      0x43028000      fab_ptr
0x9a800000
S:fabattr      0x9a8000d4      fab_iop
0x9a800050
S:cfgbm      0xbb828a84      port_ctrl
0xb6ab1058
S:pcap.pcap_bm 0x8d215547      pcap.pcap2_bm
0x2588289

```

```

S:pcap.pcap3_bm          0x1bebe0c
ui_idx                    56
    0
is_icl                    0
S:neg_speed              0 0 0 0 0
S:my_domain              0x1
S:hw_sn_maxtries        100
    0
S:hw_link_maxtries      10
S:rx_cyc_tov            28
S:bufrdy_tov            300
S:mark_tov              300
S:buf_dealloc_wait      4
S:hw_lk_train_tov       540
    150
S:syswait_tx_12_lips    1
S:al_time_tov           15
S:intr_tries_port       500
    250
S:intr_lsrflt_debounce  500
S:port_no_fid            3
S:port_fault1_thresh    100
S:port_fault1_disc_thresh 500
port_fault1_disc_spur_thresh 1000
S:port_fault2_thresh    5
S:port_sw_link_to       15
    1
frc_hw_sn_mode           0x1
S:enc_poll_thresh       0
S:fec_in_sync_to        50
    4
S:port_be_lto_threshold 100
    2
S:be_cr_in_sync_to      5
port_credit_overrun_thresh 10
S:jda_sfp_losig_tov     400
jda_sfp_losig_try_max   30
S:striped_wd_tov        3000
no_sync_debounce        1200
S:
S:    fab_iop
S:=====
S:fab_iop->interop_mode  0x0
S:fab_iop->fl_bbc        0x0
    0x0
S:fab_iop->fl_cls        0x4
    0x0
S:fab_iop->domain_id_offset 0x60
>mcdt_fabric_mode       0x0
S:fab_iop->mcdt_default_zone 0x0
>mcdt_safe_zone         0x0
S:
S:    port_ctrl
S:slot_no
S:sw_usr_ports          400
port_mode               0x0
    sw_sn_maxtries
sw_link_maxtries        5
rttov                   300
busybuf_tov             286
lksm_tov                3000
hw_wd_tov               3000
    hw_lk_test_tov
lip_rx_tov              55
lp_tov                  2000
    intr_mod_debounce
intr_efifo_debounce     100
excess_ptintr_thresh    8
port_fault1_spur_thresh 250
losync_tov              100
    en_8g_scramble
fec_enable
fec_in_sync_try_max
port_be_lr_threshold

```

```

S:=====
S:port_ctrl.port_type 1 port_ctrl.port_grp 0
S:port_ctrl.port_number 56 port_ctrl.vc_mode 1
S:
S: port_ctrl.lcap
S:=====
S:has_serdes 0 has_media 1
S:topology 1 skip_nego 0
S:skip_pnego 0 skip_init_event 0
S:en_shim 0 speed_neg
1
S:loop_back 0 num_speeds 5
S:fec_enable 0
S:
S: port_ctrl.speed_list array
S:=====
S:speed_list[0].auto_neg 1 speed_list[0].lnk_speed 0x0000000a
S:speed_list[1].auto_neg 1 speed_list[1].lnk_speed 0x00000008
S:speed_list[2].auto_neg 1 speed_list[2].lnk_speed 0x00000006
S:speed_list[3].auto_neg 1 speed_list[3].lnk_speed 0x00000005
S:speed_list[4].auto_neg 1 speed_list[4].lnk_speed 0x00000003
S:speed_list[5].auto_neg 0 speed_list[5].lnk_speed 0x00000000
S:
S: port_ctrl.cm
S:=====
S:port_ctrl.cm.num_vcs 8
S:port_ctrl.cm.min_bufs 8
S:port_ctrl.cm.cr_shar_bufs 0
S:port_ctrl.vc_alloc
S:port_ctrl.vc_alloc 2 0 1 1 1 1 1 1
S:port_ctrl.vc_alloc 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.norm_vc_alloc
S:port_ctrl.norm_vc_alloc 4 0 5 5 5 5 1 1
S:port_ctrl.norm_vc_alloc 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.cm.skip_bb_credit 0
S:port_ctrl.cm.use_shim_based_sublist 0
S:
S: port_ctrl.serdes_set
S:=====
S:serdes_type 0x8
S:serdes_data_t.ibm_hss_serdes.tx_drive_power 0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b_sign 0x1
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b 0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_a 0x0
S:serdes_data_t.ibm_hss_serdes.rxeq 0x0
S:
S: cfgbm
S:=====
S:old_distance 0x0 gport_lockdown 0x0
S:tport 0x1 speed 0x0
S:disable_eport 0x0 fcacc 0x0
S:lport_lockdown 0x0 priv_lport_lockdown

```

```

    0x0
S:vcxlt_linit          0x0          delay_flogi          0x0
S:isl_interop         0x0          distance             0x0
S:BufStarvFlag       0x0          credit_sharing       0x0
S:lport_halfduplex   0x0          lport_fairness       0x0
S:soft_neg            0x0          asn_frc_hwretry      0x0
S:cr_recov           0x0          fport_buffers        0x0
S:export              0x0          export_mode          0x0
    0x0
S:csctl_en            0x0          mirror_port          0x0
S:fault_delay         0x0          non_dfe              0x0
S:fec_configured*(0=ENAB) 0          fec_tts              0
    0

```

S:port_persistently_disabled (permanently) 0 (0)

S:

S: cfg property

S:=====

S:priv_pcfg_bm 0x00000000 lgcl_pcfg_bm

0xbb828ac4

S:fport_buffer 0x00000000

S:

S:

S:C4 Discard Cntrs: rxlp_stats = 0xb6ab03b0

S:-----

```

S:disc_mcast_wka      0x0          disc_inv_did         0x0
S:disc_cl1_cl4        0x0          disc_sid_chk_fail    0x0
S:disc_inv_dom_egid_txpt 0x0          disc_vft_hop_cnt_1
    0x0
S:disc_classf         0x0          disc_fcp_cdb_inv     0x0
S:disc_vfid_trap_enabled 0x0
disc_vfid_hdr_chk_fail 0x0
S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err 0x0
S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err 0x0
S:disc_ftb_vm_mode    0x0          disc_ftb_agnt2_miss  0x0
S:disc_ecb_de_pad_err 0x0          disc_ecb_de_tag_err  0x0
S:disc_ecb_de_seq_err 0x0          disc_ecb_err          0x0
S:disc_ftb_type4_match 0x0          disc_fcp_rsp_ftb_type4 0x0
S:disc_fcp_rsp_ftb_type4 0x0          disc_ftb_type5_match
    0x0
S:disc_ftb_type3_match 0x0          disc_els_ftb_type3   0x0
S:disc_ftb_type1_match 0x0          disc_els_rsp_ex_port 0x0
S:disc_inv_drp_dps    0x0          disc_did_lookup_miss 0x0
S:disc_ftb_type2_match 0x0          disc_trpd_plogi_pdisc 0x0
S:disc_type2_lookup_miss 0x0          disc_ftb_type6_match
    0x0
S:disc_els_rep_ex_port 0x0          disc_els_sid_lkup_bit1 0x0
S:disc_els_sid_lkup_bit0 0x0
disc_bls_frm_trap_bit1 0x0
S:disc_ftb_token_err  0x0          disc_asic_internal_err 0x0
S:disc_hard_zone_miss 0x0          disc_lun_zone_miss    0x0
S:discflt_frame_disc  0x0          discflt_parity_err    0x0
S:disc_frame_marked_du 0x0          disc_frame_marked_to  0x0

```

E:Connection type: FE

```

E:Port type: E_port
E:Trunk port: No
E:Configured Speed: AUTO_SPEED_NEGO
E:Max Capable Speed: 32G
E:Current SNSM Speed: UNDEFINED
E:Hardware TX Speed: 32G (0x00000004)
E:Hardware RX Speed: 32G (0x00000040)
E:
E:Interrupts:      0          Link_failure:      0
Loss_of_sync:     0          Loss_of_sig:       0
E:Lli:            0          Invalid_word:      0
E:trapped_frm:    0          fwd_status_ok:     0
E:fwd_timeout:    0          fwd_tx_unavail:    0
E:fwd_unroutable: 0          fwd_zone_out:      0
E:fwd_other_err:  0          frm_err_discard:   0
E:Fltr listA:     0          Fltr listB:        0
E:Zone trap fwd:  0          Zone trap disc:    0
E:shim_csum:      0          RTE_perr:          0
E:Invalid_crc:    0          Delim_err:         0
E:Protocol_err:   0
E:Lr_in:          0          Lr_out:            0
E:Ols_in:         0          Ols_out:           0

```

filterportshow 56

FILTER DATA

```

-----
Shadow settings:
  Filter Enable: 0x00000000
  Redir RAM[0]: 0x00000000
  Redir RAM[1]: 0x00000000
  Redir RAM[2]: 0x00000000
  Redir RAM[3]: 0x00000000
  Redir RAM[4]: 0x00000000
  Redir RAM[5]: 0x00000000
  Redir RAM[6]: 0x00000000
  Redir RAM[7]: 0x00000000
  Redir RAM[8]: 0x00000000
  Redir RAM[9]: 0x00000000
  Redir RAM[10]: 0x00000000
  Redir RAM[11]: 0x00000000
  Redir RAM[12]: 0x00000000
  Redir RAM[13]: 0x00000000
  Redir RAM[14]: 0x00000000
  Redir RAM[15]: 0x00000000
  Redir RAM[16]: 0x00000000
  Redir RAM[17]: 0x00000000
  Redir RAM[18]: 0x00000000
  Redir RAM[19]: 0x00000000
  Redir RAM[20]: 0x00000000
  Redir RAM[21]: 0x00000000
  Redir RAM[22]: 0x00000000
  Redir RAM[23]: 0x00000000

```

Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass: 0x00000000

Real settings:

Enable RAM: 0x00000000, 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass RAM: 0x00000000

Shadowed filters:

Filter 0: Not Installed (MIRROR1)(LISTA)

c4_fldenable[0] = 0x00000000 0x00000000 0x00000000
0x00000000

c4_fldnegate[0] = 0x00000000, c4_fltr_config[0] = 0x00000000

Filter 1: Not Installed (MIRROR2)(LISTA)

c4_fldenable[1] = 0x00000000 0x00000000 0x00000000
0x00000000

```
    c4_fldnegate[1] = 0x00000000,c4_fltr_config[1] = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
    c4_fldenable[2] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[2] = 0x00000000,c4_fltr_config[2] = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
    c4_fldenable[3] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[3] = 0x00000000,c4_fltr_config[3] = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
    c4_fldenable[4] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[4] = 0x00000000,c4_fltr_config[4] = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
    c4_fldenable[5] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[5] = 0x00000000,c4_fltr_config[5] = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
    c4_fldenable[6] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[6] = 0x00000000,c4_fltr_config[6] = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
    c4_fldenable[7] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[7] = 0x00000000,c4_fltr_config[7] = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
    c4_fldenable[8] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[8] = 0x00000000,c4_fltr_config[8] = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
    c4_fldenable[9] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[9] = 0x00000000,c4_fltr_config[9] = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
    c4_fldenable[10] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[10] = 0x00000000,c4_fltr_config[10] =
0x00000000
Filter 11: Not Installed (SIM)(LISTA)
    c4_fldenable[11] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[11] = 0x00000000,c4_fltr_config[11] =
0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
    c4_fldenable[12] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[12] = 0x00000000,c4_fltr_config[12] =
0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
    c4_fldenable[13] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[13] = 0x00000000,c4_fltr_config[13] =
0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
```



```
    c4_fldenable[14] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[14] = 0x00000000,c4_fltr_config[14] =
0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
    c4_fldenable[15] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[15] = 0x00000000,c4_fltr_config[15] =
0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
    c4_fldenable[16] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[16] = 0x00000000,c4_fltr_config[16] =
0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
    c4_fldenable[17] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[17] = 0x00000000,c4_fltr_config[17] =
0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
    c4_fldenable[18] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[18] = 0x00000000,c4_fltr_config[18] =
0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
    c4_fldenable[19] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[19] = 0x00000000,c4_fltr_config[19] =
0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
    c4_fldenable[20] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[20] = 0x00000000,c4_fltr_config[20] =
0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
    c4_fldenable[21] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[21] = 0x00000000,c4_fltr_config[21] =
0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
    c4_fldenable[22] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[22] = 0x00000000,c4_fltr_config[22] =
0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
    c4_fldenable[23] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[23] = 0x00000000,c4_fltr_config[23] =
0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
    c4_fldenable[24] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[24] = 0x00000000,c4_fltr_config[24] =
0x00000000
```

Filter 25: Not Installed (PERF10)(LISTA)
c4_fldenable[25] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[25] = 0x00000000,c4_fltr_config[25] =
0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
c4_fldenable[26] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[26] = 0x00000000,c4_fltr_config[26] =
0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
c4_fldenable[27] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[27] = 0x00000000,c4_fltr_config[27] =
0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
c4_fldenable[28] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[28] = 0x00000000,c4_fltr_config[28] =
0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
c4_fldenable[29] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[29] = 0x00000000,c4_fltr_config[29] =
0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
c4_fldenable[30] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[30] = 0x00000000,c4_fltr_config[30] =
0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
c4_fldenable[31] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[31] = 0x00000000,c4_fltr_config[31] =
0x00000000

Real filters:

Filter 0: Not Installed (MIRROR1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,

```
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 11: Not Installed (SIM)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
```

fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,

fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter dirty indicator: 0x00000000
Performance filters: 0
Port Mirror filters: 0 (0x0)

FIELD DATA

Shadowed fields:

fldoffset[0] = 0x00, fldmask[0] = 0x00, fldvalue_dyna[0]: 0x00 0x00
0x00 0x00
fldcontrol[0].inuse = 0x0 fldcontrol[0].refcnt = 0x00 0x00 0x00
0x00
fldoffset[1] = 0x00, fldmask[1] = 0x00, fldvalue_dyna[1]: 0x00 0x00
0x00 0x00
fldcontrol[1].inuse = 0x0 fldcontrol[1].refcnt = 0x00 0x00 0x00
0x00
fldoffset[2] = 0x00, fldmask[2] = 0x00, fldvalue_dyna[2]: 0x00 0x00
0x00 0x00
fldcontrol[2].inuse = 0x0 fldcontrol[2].refcnt = 0x00 0x00 0x00
0x00
fldoffset[3] = 0x00, fldmask[3] = 0x00, fldvalue_dyna[3]: 0x00 0x00
0x00 0x00
fldcontrol[3].inuse = 0x0 fldcontrol[3].refcnt = 0x00 0x00 0x00
0x00
fldoffset[4] = 0x00, fldmask[4] = 0x00, fldvalue_dyna[4]: 0x00 0x00
0x00 0x00
fldcontrol[4].inuse = 0x0 fldcontrol[4].refcnt = 0x00 0x00 0x00
0x00
fldoffset[5] = 0x00, fldmask[5] = 0x00, fldvalue_dyna[5]: 0x00 0x00
0x00 0x00
fldcontrol[5].inuse = 0x0 fldcontrol[5].refcnt = 0x00 0x00 0x00
0x00
fldoffset[6] = 0x00, fldmask[6] = 0x00, fldvalue_dyna[6]: 0x00 0x00
0x00 0x00
fldcontrol[6].inuse = 0x0 fldcontrol[6].refcnt = 0x00 0x00 0x00
0x00
fldoffset[7] = 0x00, fldmask[7] = 0x00, fldvalue_dyna[7]: 0x00 0x00
0x00 0x00
fldcontrol[7].inuse = 0x0 fldcontrol[7].refcnt = 0x00 0x00 0x00
0x00
fldoffset[8] = 0x00, fldmask[8] = 0x00, fldvalue_dyna[8]: 0x00 0x00
0x00 0x00
fldcontrol[8].inuse = 0x0 fldcontrol[8].refcnt = 0x00 0x00 0x00
0x00
fldoffset[9] = 0x00, fldmask[9] = 0x00, fldvalue_dyna[9]: 0x00 0x00
0x00 0x00

```
fldcontrol[9].inuse = 0x0 fldcontrol[9].refcnt = 0x00 0x00 0x00
0x00
fldoffset[10] = 0x00, fldmask[10] = 0x00, fldvalue_dyna[10]:0x00 0x00
0x00 0x00
fldcontrol[10].inuse = 0x0 fldcontrol[10].refcnt = 0x00 0x00 0x00
0x00
fldoffset[11] = 0x00, fldmask[11] = 0x00, fldvalue_dyna[11]:0x00 0x00
0x00 0x00
fldcontrol[11].inuse = 0x0 fldcontrol[11].refcnt = 0x00 0x00 0x00
0x00
fldoffset[12] = 0x00, fldmask[12] = 0x00, fldvalue_dyna[12]:0x00 0x00
0x00 0x00
fldcontrol[12].inuse = 0x0 fldcontrol[12].refcnt = 0x00 0x00 0x00
0x00
fldoffset[13] = 0x00, fldmask[13] = 0x00, fldvalue_dyna[13]:0x00 0x00
0x00 0x00
fldcontrol[13].inuse = 0x0 fldcontrol[13].refcnt = 0x00 0x00 0x00
0x00
fldoffset[14] = 0x00, fldmask[14] = 0x00, fldvalue_dyna[14]:0x00 0x00
0x00 0x00
fldcontrol[14].inuse = 0x0 fldcontrol[14].refcnt = 0x00 0x00 0x00
0x00
fldoffset[15] = 0x00, fldmask[15] = 0x00, fldvalue_dyna[15]:0x00 0x00
0x00 0x00
fldcontrol[15].inuse = 0x0 fldcontrol[15].refcnt = 0x00 0x00 0x00
0x00
fldoffset[16] = 0x00, fldmask[16] = 0x00, fldvalue_dyna[16]:0x00 0x00
0x00 0x00
fldcontrol[16].inuse = 0x0 fldcontrol[16].refcnt = 0x00 0x00 0x00
0x00
fldoffset[17] = 0x00, fldmask[17] = 0x00, fldvalue_dyna[17]:0x00 0x00
0x00 0x00
fldcontrol[17].inuse = 0x0 fldcontrol[17].refcnt = 0x00 0x00 0x00
0x00
fldoffset[18] = 0x00, fldmask[18] = 0x00, fldvalue_dyna[18]:0x00 0x00
0x00 0x00
fldcontrol[18].inuse = 0x0 fldcontrol[18].refcnt = 0x00 0x00 0x00
0x00
fldoffset[19] = 0x00, fldmask[19] = 0x00, fldvalue_dyna[19]:0x00 0x00
0x00 0x00
fldcontrol[19].inuse = 0x0 fldcontrol[19].refcnt = 0x00 0x00 0x00
0x00
```

Real fields:

```
fldoffset RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000
fldmask RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000
fld value4 RAM:
0x00000000
0x00000000
0x00000000
0x00000000
```

0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000

Field dirty indicator: 0x00000000

FDB reference count fdb: 0 [0 0 0 0]
FDB reference count fdb: 1 [0 0 0 0]
FDB reference count fdb: 2 [0 0 0 0]
FDB reference count fdb: 3 [0 0 0 0]
FDB reference count fdb: 4 [0 0 0 0]
FDB reference count fdb: 5 [0 0 0 0]
FDB reference count fdb: 6 [0 0 0 0]
FDB reference count fdb: 7 [0 0 0 0]
FDB reference count fdb: 8 [0 0 0 0]
FDB reference count fdb: 9 [0 0 0 0]
FDB reference count fdb: 10 [0 0 0 0]
FDB reference count fdb: 11 [0 0 0 0]
FDB reference count fdb: 12 [0 0 0 0]
FDB reference count fdb: 13 [0 0 0 0]
FDB reference count fdb: 14 [0 0 0 0]
FDB reference count fdb: 15 [0 0 0 0]
FDB reference count fdb: 16 [0 0 0 0]
FDB reference count fdb: 17 [0 0 0 0]
FDB reference count fdb: 18 [0 0 0 0]
FDB reference count fdb: 19 [0 0 0 0]

Filter counters:

Filter counter 0: 0 (MIRROR1)
Filter counter 1: 0 (MIRROR2)
Filter counter 2: 0 (MIRROR3)
Filter counter 3: 0 (MIRROR4)
Filter counter 4: 0 (AEPORT_NON_MIRR_DROP)
Filter counter 5: 0 (ZONING TRAP)
Filter counter 6: 0 (FCR_EXPORT_DC)
Filter counter 7: 0 (TIN TRAP)
Filter counter 8: 0 (FICON CUP)
Filter counter 9: 0 (FICON CUP DST)
Filter counter 10: 0 (WELL KNOWN ADDR)
Filter counter 11: 0 (SIM)
Filter counter 12: 0 (UNUSED)
Filter counter 13: 0 (UNUSED)

Filter counter 14: 0 (UNUSED)
Filter counter 15: 0 (UNUSED)
Filter counter 16: 0 (PERF1)
Filter counter 17: 0 (PERF2)
Filter counter 18: 0 (PERF3)
Filter counter 19: 0 (PERF4)
Filter counter 20: 0 (PERF5)
Filter counter 21: 0 (PERF6)
Filter counter 22: 0 (PERF7)
Filter counter 23: 0 (PERF8)
Filter counter 24: 0 (PERF9)
Filter counter 25: 0 (PERF10)
Filter counter 26: 0 (PERF11)
Filter counter 27: 0 (PERF12)
Filter counter 28: 0 (OPM1)
Filter counter 29: 0 (OPM2)
Filter counter 30: 0 (IPM1)
Filter counter 31: 0 (IPM2)

ACL DATA

Logical port 0: Hard Zoning disabled, Soft Zoning disabled
Zone type: WWN Zoning
Frames with hard zone miss: 0

ACL Hash table

Hash index :0x74
Flow index 0x30: SID :0x 10a00 DID :0x 40b00 VF_ID :0x 80
RX_PORT :0x32

Hash index :0x540
Flow index 0x97: SID :0x 10a00 DID :0x 40900 VF_ID :0x 80
RX_PORT :0x32

Hash index :0xa18
Flow index 0x2c: SID :0x 10a00 DID :0x 40f00 VF_ID :0x 80
RX_PORT :0x32

Hash index :0xf2c
Flow index 0x2e: SID :0x 10a00 DID :0x 40d00 VF_ID :0x 80
RX_PORT :0x32

Hash index :0x1700
Flow index 0x42: SID :0x 10600 DID :0x 10600 VF_ID :0x 80
RX_PORT :0x3b

Hash index :0x242c
Flow index 0x91: SID :0x 11500 DID :0x 10c00 VF_ID :0x 80
RX_PORT :0x2c

Hash index :0x2b74
Flow index 0x87: SID :0x 11500 DID :0x 10a00 VF_ID :0x 80
RX_PORT :0x2c

Hash index :0x49a0
Flow index 0x9b: SID :0x 11600 DID :0x 10b00 VF_ID :0x 80
RX_PORT :0x2b

Hash index :0x5188
Flow index 0x84: SID :0x 10b00 DID :0x 10a00 VF_ID :0x 80
RX_PORT :0x31

Hash index :0x5ed0

Flow index 0x35: SID :0x 10b00 DID :0x 10c00 VF_ID :0x 80
RX_PORT :0x31
Hash index :0x635c
Flow index 0xc: SID :0x 12600 DID :0x 40a00 VF_ID :0x 80
RX_PORT :0x1b
Hash index :0x6930
Flow index 0x8: SID :0x 12600 DID :0x 40e00 VF_ID :0x 80
RX_PORT :0x1b
Hash index :0x6944
Flow index 0xa6: SID :0x 10c00 DID :0x 11900 VF_ID :0x 80
RX_PORT :0x37
Hash index :0x6c04
Flow index 0xa: SID :0x 12600 DID :0x 40c00 VF_ID :0x 80
RX_PORT :0x1b
Hash index :0x6d6c
Flow index 0xb8: SID :0x 10c00 DID :0x 12500 VF_ID :0x 80
RX_PORT :0x37
Hash index :0x7070
Flow index 0x32: SID :0x 11100 DID :0x 12600 VF_ID :0x 80
RX_PORT :0x2d
Hash index :0x70e0
Flow index 0x41: SID :0x 10500 DID :0x 10500 VF_ID :0x 80
RX_PORT :0x3c
Hash index :0x72c4
Flow index 0x6d: SID :0x 10c00 DID :0x 11700 VF_ID :0x 80
RX_PORT :0x37
Hash index :0x77f0
Flow index 0x96: SID :0x 10c00 DID :0x 11500 VF_ID :0x 80
RX_PORT :0x37
Hash index :0x78a8
Flow index 0x24: SID :0x 10c00 DID :0x 11300 VF_ID :0x 80
RX_PORT :0x37
Hash index :0x7d9c
Flow index 0x69: SID :0x 10c00 DID :0x 11100 VF_ID :0x 80
RX_PORT :0x37
Hash index :0x8190
Flow index 0x13: SID :0x 11400 DID :0x 11400 VF_ID :0x 80
RX_PORT :0x2f
Hash index :0x82d8
Flow index 0xbb: SID :0x 12600 DID :0x 12500 VF_ID :0x 80
RX_PORT :0x1b
Hash index :0x83b0
Flow index 0x53: SID :0x 10c00 DID :0x 40c00 VF_ID :0x 80
RX_PORT :0x37
Hash index :0x8684
Flow index 0x55: SID :0x 10c00 DID :0x 40e00 VF_ID :0x 80
RX_PORT :0x37
Hash index :0x86f0
Flow index 0x34: SID :0x 12600 DID :0x 11900 VF_ID :0x 80
RX_PORT :0x1b
Hash index :0x870c
Flow index 0x5d: SID :0x 10900 DID :0x 11900 VF_ID :0x 80
RX_PORT :0x35
Hash index :0x8ce8

Flow index 0x51: SID :0x 10c00 DID :0x 40a00 VF_ID :0x 80
RX_PORT :0x37
Hash index :0x9228
Flow index 0x4c: SID :0x 12600 DID :0x 11100 VF_ID :0x 80
RX_PORT :0x1b
Hash index :0x93d4
Flow index 0x62: SID :0x 10900 DID :0x 11100 VF_ID :0x 80
RX_PORT :0x35
Hash index :0x96e0
Flow index 0x60: SID :0x 10900 DID :0x 11300 VF_ID :0x 80
RX_PORT :0x35
Hash index :0x971c
Flow index 0x9e: SID :0x 12600 DID :0x 11300 VF_ID :0x 80
RX_PORT :0x1b
Hash index :0x9844
Flow index 0x4e: SID :0x 12600 DID :0x 11500 VF_ID :0x 80
RX_PORT :0x1b
Hash index :0x99b8
Flow index 0x5e: SID :0x 10900 DID :0x 11500 VF_ID :0x 80
RX_PORT :0x35
Hash index :0x9c8c
Flow index 0x66: SID :0x 10900 DID :0x 11700 VF_ID :0x 80
RX_PORT :0x35
Hash index :0x9d70
Flow index 0x10: SID :0x 12600 DID :0x 11700 VF_ID :0x 80
RX_PORT :0x1b
Hash index :0x9e38
Flow index 0x7b: SID :0x 11400 DID :0x 12600 VF_ID :0x 80
RX_PORT :0x2f
Hash index :0xa0fc
Flow index 0x72: SID :0x 10b00 DID :0x 41100 VF_ID :0x 80
RX_PORT :0x31
Hash index :0xa5c8
Flow index 0x71: SID :0x 10b00 DID :0x 41300 VF_ID :0x 80
RX_PORT :0x31
Hash index :0xa7e8
Flow index 0x1b: SID :0x 11300 DID :0x 10b00 VF_ID :0x 80
RX_PORT :0x29
Hash index :0xaa90
Flow index 0x6f: SID :0x 10b00 DID :0x 41500 VF_ID :0x 80
RX_PORT :0x31
Hash index :0xaf4
Flow index 0xab: SID :0x 10b00 DID :0x 41700 VF_ID :0x 80
RX_PORT :0x31
Hash index :0xb5ac
Flow index 0x44: SID :0x 10e00 DID :0x 10e00 VF_ID :0x 80
RX_PORT :0x33
Hash index :0xc53c
Flow index 0x90: SID :0x 11000 DID :0x 10a00 VF_ID :0x 80
RX_PORT :0x2e
Hash index :0xc604
Flow index 0x33: SID :0x 11900 DID :0x 12600 VF_ID :0x 80
RX_PORT :0x25
Hash index :0xca64

Flow index 0x88: SID :0x 11000 DID :0x 10c00 VF_ID :0x 80
RX_PORT :0x2e
Hash index :0xd24c
Flow index 0x3b: SID :0x 10d00 DID :0x 10d00 VF_ID :0x 80
RX_PORT :0x34
Hash index :0xe4c4
Flow index 0x7a: SID :0x 10a00 DID :0x 12600 VF_ID :0x 80
RX_PORT :0x32
Hash index :0xe538
Flow index 0x7c: SID :0x 12500 DID :0x 12600 VF_ID :0x 80
RX_PORT :0x1c
Hash index :0xe670
Flow index 0x3c: SID :0x 11700 DID :0x 11700 VF_ID :0x 80
RX_PORT :0x28
Hash index :0xf100
Flow index 0x8c: SID :0x 10a00 DID :0x 11000 VF_ID :0x 80
RX_PORT :0x32
Hash index :0xf434
Flow index 0x19: SID :0x 10a00 DID :0x 11200 VF_ID :0x 80
RX_PORT :0x32
Hash index :0xfb6c
Flow index 0x15: SID :0x 10a00 DID :0x 11400 VF_ID :0x 80
RX_PORT :0x32
Hash index :0x10c6c
Flow index 0xae: SID :0x 10a00 DID :0x 41800 VF_ID :0x 80
RX_PORT :0x32
Hash index :0x110f8
Flow index 0x37: SID :0x 11200 DID :0x 10c00 VF_ID :0x 80
RX_PORT :0x2a
Hash index :0x112d8
Flow index 0x28: SID :0x 10a00 DID :0x 41400 VF_ID :0x 80
RX_PORT :0x32
Hash index :0x11340
Flow index 0xb2: SID :0x 11f00 DID :0x 11f00 VF_ID :0x 80
RX_PORT :0x21
Hash index :0x117ec
Flow index 0x26: SID :0x 10a00 DID :0x 41600 VF_ID :0x 80
RX_PORT :0x32
Hash index :0x118b4
Flow index 0x2b: SID :0x 10a00 DID :0x 41000 VF_ID :0x 80
RX_PORT :0x32
Hash index :0x11fa0
Flow index 0x82: SID :0x 11200 DID :0x 10a00 VF_ID :0x 80
RX_PORT :0x2a
Hash index :0x139d8
Flow index 0x8e: SID :0x 11500 DID :0x 11500 VF_ID :0x 80
RX_PORT :0x2c
Hash index :0x14324
Flow index 0x95: SID :0x 10b00 DID :0x 11500 VF_ID :0x 80
RX_PORT :0x31
Hash index :0x144a4
Flow index 0xf: SID :0x 11600 DID :0x 12600 VF_ID :0x 80
RX_PORT :0x2b
Hash index :0x14610

Flow index 0x40: SID :0x 10b00 DID :0x 11700 VF_ID :0x 80
RX_PORT :0x31
Hash index :0x14948
Flow index 0x22: SID :0x 10b00 DID :0x 11100 VF_ID :0x 80
RX_PORT :0x31
Hash index :0x14c7c
Flow index 0x1c: SID :0x 10b00 DID :0x 11300 VF_ID :0x 80
RX_PORT :0x31
Hash index :0x159b8
Flow index 0xba: SID :0x 10b00 DID :0x 12500 VF_ID :0x 80
RX_PORT :0x31
Hash index :0x15d90
Flow index 0xa8: SID :0x 10b00 DID :0x 11900 VF_ID :0x 80
RX_PORT :0x31
Hash index :0x1655c
Flow index 0x99: SID :0x 10c00 DID :0x 10a00 VF_ID :0x 80
RX_PORT :0x37
Hash index :0x16a04
Flow index 0x20: SID :0x 10c00 DID :0x 10c00 VF_ID :0x 80
RX_PORT :0x37
Hash index :0x171f0
Flow index 0x2: SID :0x 12600 DID :0x 41500 VF_ID :0x 80
RX_PORT :0x1b
Hash index :0x174a0
Flow index 0x47: SID :0x 11c00 DID :0x 11c00 VF_ID :0x 80
RX_PORT :0x26
Hash index :0x174c4
Flow index 0xad: SID :0x 12600 DID :0x 41700 VF_ID :0x 80
RX_PORT :0x1b
Hash index :0x17b9c
Flow index 0x5: SID :0x 12600 DID :0x 41100 VF_ID :0x 80
RX_PORT :0x1b
Hash index :0x17d74
Flow index 0x1e: SID :0x 11100 DID :0x 10b00 VF_ID :0x 80
RX_PORT :0x2d
Hash index :0x17ea8
Flow index 0x4: SID :0x 12600 DID :0x 41300 VF_ID :0x 80
RX_PORT :0x1b
Hash index :0x1844c
Flow index 0x98: SID :0x 10900 DID :0x 10c00 VF_ID :0x 80
RX_PORT :0x35
Hash index :0x185b0
Flow index 0x8a: SID :0x 12600 DID :0x 10c00 VF_ID :0x 80
RX_PORT :0x1b
Hash index :0x18ae8
Flow index 0x49: SID :0x 12600 DID :0x 10a00 VF_ID :0x 80
RX_PORT :0x1b
Hash index :0x18b14
Flow index 0x64: SID :0x 10900 DID :0x 10a00 VF_ID :0x 80
RX_PORT :0x35
Hash index :0x1911c
Flow index 0x59: SID :0x 10c00 DID :0x 41300 VF_ID :0x 80
RX_PORT :0x37
Hash index :0x1933c

Flow index 0x14: SID :0x 11400 DID :0x 10b00 VF_ID :0x 80
RX_PORT :0x2f
Hash index :0x19428
Flow index 0x58: SID :0x 10c00 DID :0x 41100 VF_ID :0x 80
RX_PORT :0x37
Hash index :0x19b70
Flow index 0xac: SID :0x 10c00 DID :0x 41700 VF_ID :0x 80
RX_PORT :0x37
Hash index :0x19b74
Flow index 0x7d: SID :0x 11d00 DID :0x 11d00 VF_ID :0x 80
RX_PORT :0x24
Hash index :0x19e44
Flow index 0x5b: SID :0x 10c00 DID :0x 41500 VF_ID :0x 80
RX_PORT :0x37
Hash index :0x1aaec
Flow index 0x4f: SID :0x 11300 DID :0x 12600 VF_ID :0x 80
RX_PORT :0x29
Hash index :0x1af48
Flow index 0x43: SID :0x 10700 DID :0x 10700 VF_ID :0x 80
RX_PORT :0x38
Hash index :0x1b250
Flow index 0x75: SID :0x 10b00 DID :0x 40e00 VF_ID :0x 80
RX_PORT :0x31
Hash index :0x1b764
Flow index 0x77: SID :0x 10b00 DID :0x 40c00 VF_ID :0x 80
RX_PORT :0x31
Hash index :0x1b83c
Flow index 0x79: SID :0x 10b00 DID :0x 40a00 VF_ID :0x 80
RX_PORT :0x31
Hash index :0x1c8a8
Flow index 0x16: SID :0x 10400 DID :0x 10400 VF_ID :0x 80
RX_PORT :0x3f
Hash index :0x1cb00
Flow index 0xb7: SID :0x 11900 DID :0x 10b00 VF_ID :0x 80
RX_PORT :0x25
Hash index :0x1e83c
Flow index 0x3e: SID :0x 12500 DID :0x 10b00 VF_ID :0x 80
RX_PORT :0x1c
Hash index :0x1e9c0
Flow index 0x1: SID :0x 10a00 DID :0x 10b00 VF_ID :0x 80
RX_PORT :0x32
Hash index :0x1f1e8
Flow index 0x7f: SID :0x 11700 DID :0x 10a00 VF_ID :0x 80
RX_PORT :0x28
Hash index :0x1feb0
Flow index 0x3d: SID :0x 11700 DID :0x 10c00 VF_ID :0x 80
RX_PORT :0x28
Hash index :0x200cc
Flow index 0x17: SID :0x 11200 DID :0x 11200 VF_ID :0x 80
RX_PORT :0x2a
Hash index :0x202ec
Flow index 0xa1: SID :0x 10a00 DID :0x 40a00 VF_ID :0x 80
RX_PORT :0x32
Hash index :0x20880

Flow index 0x2d: SID :0x 10a00 DID :0x 40e00 VF_ID :0x 80
RX_PORT :0x32
Hash index :0x20db4
Flow index 0x2f: SID :0x 10a00 DID :0x 40c00 VF_ID :0x 80
RX_PORT :0x32
Hash index :0x2103c
Flow index 0xe: SID :0x 11200 DID :0x 12600 VF_ID :0x 80
RX_PORT :0x2a
Hash index :0x229ec
Flow index 0x92: SID :0x 11500 DID :0x 10b00 VF_ID :0x 80
RX_PORT :0x2c
Hash index :0x22a54
Flow index 0x45: SID :0x 11800 DID :0x 11800 VF_ID :0x 80
RX_PORT :0x27
Hash index :0x234f0
Flow index 0x46: SID :0x 10800 DID :0x 10800 VF_ID :0x 80
RX_PORT :0x36
Hash index :0x24460
Flow index 0x9a: SID :0x 11600 DID :0x 10c00 VF_ID :0x 80
RX_PORT :0x2b
Hash index :0x24b38
Flow index 0x7e: SID :0x 11600 DID :0x 10a00 VF_ID :0x 80
RX_PORT :0x2b
Hash index :0x25310
Flow index 0x21: SID :0x 10b00 DID :0x 10b00 VF_ID :0x 80
RX_PORT :0x31
Hash index :0x261c4
Flow index 0xb: SID :0x 12600 DID :0x 40b00 VF_ID :0x 80
RX_PORT :0x1b
Hash index :0x264f0
Flow index 0x9c: SID :0x 12600 DID :0x 40900 VF_ID :0x 80
RX_PORT :0x1b
Hash index :0x2672c
Flow index 0x1d: SID :0x 11100 DID :0x 11100 VF_ID :0x 80
RX_PORT :0x2d
Hash index :0x26ac0
Flow index 0xb5: SID :0x 10c00 DID :0x 12600 VF_ID :0x 80
RX_PORT :0x37
Hash index :0x26ba8
Flow index 0x7: SID :0x 12600 DID :0x 40f00 VF_ID :0x 80
RX_PORT :0x1b
Hash index :0x26e9c
Flow index 0x9: SID :0x 12600 DID :0x 40d00 VF_ID :0x 80
RX_PORT :0x1b
Hash index :0x27568
Flow index 0x6c: SID :0x 10c00 DID :0x 11400 VF_ID :0x 80
RX_PORT :0x37
Hash index :0x27a30
Flow index 0x6a: SID :0x 10c00 DID :0x 11200 VF_ID :0x 80
RX_PORT :0x37
Hash index :0x27f04
Flow index 0x8b: SID :0x 10c00 DID :0x 11000 VF_ID :0x 80
RX_PORT :0x37
Hash index :0x28128

Flow index 0x54: SID :0x 10c00 DID :0x 40d00 VF_ID :0x 80
RX_PORT :0x37
Hash index :0x2841c
Flow index 0x56: SID :0x 10c00 DID :0x 40f00 VF_ID :0x 80
RX_PORT :0x37
Hash index :0x28574
Flow index 0xd: SID :0x 12600 DID :0x 12600 VF_ID :0x 80
RX_PORT :0x1b
Hash index :0x28b44
Flow index 0x5f: SID :0x 10c00 DID :0x 40900 VF_ID :0x 80
RX_PORT :0x37
Hash index :0x28e70
Flow index 0x52: SID :0x 10c00 DID :0x 40b00 VF_ID :0x 80
RX_PORT :0x37
Hash index :0x290b0
Flow index 0x4b: SID :0x 12600 DID :0x 11000 VF_ID :0x 80
RX_PORT :0x1b
Hash index :0x2914c
Flow index 0x63: SID :0x 10900 DID :0x 11000 VF_ID :0x 80
RX_PORT :0x35
Hash index :0x29478
Flow index 0x61: SID :0x 10900 DID :0x 11200 VF_ID :0x 80
RX_PORT :0x35
Hash index :0x29584
Flow index 0x4d: SID :0x 12600 DID :0x 11200 VF_ID :0x 80
RX_PORT :0x1b
Hash index :0x29adc
Flow index 0x93: SID :0x 12600 DID :0x 11400 VF_ID :0x 80
RX_PORT :0x1b
Hash index :0x29b20
Flow index 0x86: SID :0x 10900 DID :0x 11400 VF_ID :0x 80
RX_PORT :0x35
Hash index :0x29e14
Flow index 0x9d: SID :0x 10900 DID :0x 11600 VF_ID :0x 80
RX_PORT :0x35
Hash index :0x2a264
Flow index 0x73: SID :0x 10b00 DID :0x 41000 VF_ID :0x 80
RX_PORT :0x31
Hash index :0x2a570
Flow index 0x81: SID :0x 11300 DID :0x 10a00 VF_ID :0x 80
RX_PORT :0x29
Hash index :0x2a808
Flow index 0x70: SID :0x 10b00 DID :0x 41400 VF_ID :0x 80
RX_PORT :0x31
Hash index :0x2aa28
Flow index 0x38: SID :0x 11300 DID :0x 10c00 VF_ID :0x 80
RX_PORT :0x29
Hash index :0x2ad3c
Flow index 0x6e: SID :0x 10b00 DID :0x 41600 VF_ID :0x 80
RX_PORT :0x31
Hash index :0x2b6bc
Flow index 0xaf: SID :0x 10b00 DID :0x 41800 VF_ID :0x 80
RX_PORT :0x31
Hash index :0x2c580

Flow index 0xa0: SID :0x 11900 DID :0x 11900 VF_ID :0x 80
RX_PORT :0x25
Hash index :0x2c7a4
Flow index 0x89: SID :0x 11000 DID :0x 10b00 VF_ID :0x 80
RX_PORT :0x2e
Hash index :0x2e294
Flow index 0xb4: SID :0x 12500 DID :0x 12500 VF_ID :0x 80
RX_PORT :0x1c
Hash index :0x2e368
Flow index 0xb9: SID :0x 10a00 DID :0x 12500 VF_ID :0x 80
RX_PORT :0x32
Hash index :0x2e740
Flow index 0xa7: SID :0x 10a00 DID :0x 11900 VF_ID :0x 80
RX_PORT :0x32
Hash index :0x2f1bc
Flow index 0x3a: SID :0x 10300 DID :0x 10300 VF_ID :0x 80
RX_PORT :0x39
Hash index :0x2f398
Flow index 0x1f: SID :0x 10a00 DID :0x 11100 VF_ID :0x 80
RX_PORT :0x32
Hash index :0x2f6ac
Flow index 0x6b: SID :0x 10a00 DID :0x 11300 VF_ID :0x 80
RX_PORT :0x32
Hash index :0x2f9f4
Flow index 0x94: SID :0x 10a00 DID :0x 11500 VF_ID :0x 80
RX_PORT :0x32
Hash index :0x2fcc0
Flow index 0x3f: SID :0x 10a00 DID :0x 11700 VF_ID :0x 80
RX_PORT :0x32
Hash index :0x2fe74
Flow index 0xa5: SID :0x 11700 DID :0x 12600 VF_ID :0x 80
RX_PORT :0x28
Hash index :0x31040
Flow index 0x27: SID :0x 10a00 DID :0x 41500 VF_ID :0x 80
RX_PORT :0x32
Hash index :0x31574
Flow index 0xaa: SID :0x 10a00 DID :0x 41700 VF_ID :0x 80
RX_PORT :0x32
Hash index :0x31a2c
Flow index 0x2a: SID :0x 10a00 DID :0x 41100 VF_ID :0x 80
RX_PORT :0x32
Hash index :0x31d38
Flow index 0x18: SID :0x 11200 DID :0x 10b00 VF_ID :0x 80
RX_PORT :0x2a
Hash index :0x31f18
Flow index 0x29: SID :0x 10a00 DID :0x 41300 VF_ID :0x 80
RX_PORT :0x32
Hash index :0x324e8
Flow index 0x48: SID :0x 11500 DID :0x 12600 VF_ID :0x 80
RX_PORT :0x2c
Hash index :0x32e14
Flow index 0x11: SID :0x 10100 DID :0x 10100 VF_ID :0x 80
RX_PORT :0x3d
Hash index :0x341bc

Flow index 0x25: SID :0x 10b00 DID :0x 11400 VF_ID :0x 80
RX_PORT :0x31
Hash index :0x349f4
Flow index 0x12: SID :0x 10200 DID :0x 10200 VF_ID :0x 80
RX_PORT :0x3a
Hash index :0x34bd0
Flow index 0x8d: SID :0x 10b00 DID :0x 11000 VF_ID :0x 80
RX_PORT :0x31
Hash index :0x34ee4
Flow index 0x23: SID :0x 10b00 DID :0x 11200 VF_ID :0x 80
RX_PORT :0x31
Hash index :0x35e14
Flow index 0x31: SID :0x 10b00 DID :0x 12600 VF_ID :0x 80
RX_PORT :0x31
Hash index :0x367c4
Flow index 0x68: SID :0x 10c00 DID :0x 10b00 VF_ID :0x 80
RX_PORT :0x37
Hash index :0x36ddc
Flow index 0xb1: SID :0x 12600 DID :0x 41800 VF_ID :0x 80
RX_PORT :0x1b
Hash index :0x370b4
Flow index 0x36: SID :0x 11100 DID :0x 10c00 VF_ID :0x 80
RX_PORT :0x2d
Hash index :0x37368
Flow index 0x3: SID :0x 12600 DID :0x 41400 VF_ID :0x 80
RX_PORT :0x1b
Hash index :0x3765c
Flow index 0xa9: SID :0x 12600 DID :0x 41600 VF_ID :0x 80
RX_PORT :0x1b
Hash index :0x37904
Flow index 0x6: SID :0x 12600 DID :0x 41000 VF_ID :0x 80
RX_PORT :0x1b
Hash index :0x37fec
Flow index 0x83: SID :0x 11100 DID :0x 10a00 VF_ID :0x 80
RX_PORT :0x2d
Hash index :0x38268
Flow index 0xb0: SID :0x 10c00 DID :0x 41800 VF_ID :0x 80
RX_PORT :0x37
Hash index :0x38870
Flow index 0x4a: SID :0x 12600 DID :0x 10b00 VF_ID :0x 80
RX_PORT :0x1b
Hash index :0x3898c
Flow index 0x8f: SID :0x 10900 DID :0x 10b00 VF_ID :0x 80
RX_PORT :0x35
Hash index :0x391a4
Flow index 0x80: SID :0x 11400 DID :0x 10a00 VF_ID :0x 80
RX_PORT :0x2f
Hash index :0x396b0
Flow index 0x57: SID :0x 10c00 DID :0x 41000 VF_ID :0x 80
RX_PORT :0x37
Hash index :0x399e8
Flow index 0x5c: SID :0x 10c00 DID :0x 41600 VF_ID :0x 80
RX_PORT :0x37
Hash index :0x39cdc

Flow index 0x5a: SID :0x 10c00 DID :0x 41400 VF_ID :0x 80
RX_PORT :0x37
Hash index :0x39efc
Flow index 0x39: SID :0x 11400 DID :0x 10c00 VF_ID :0x 80
RX_PORT :0x2f
Hash index :0x3b0c8
Flow index 0x74: SID :0x 10b00 DID :0x 40f00 VF_ID :0x 80
RX_PORT :0x31
Hash index :0x3b5fc
Flow index 0x76: SID :0x 10b00 DID :0x 40d00 VF_ID :0x 80
RX_PORT :0x31
Hash index :0x3b884
Flow index 0x1a: SID :0x 11300 DID :0x 11300 VF_ID :0x 80
RX_PORT :0x29
Hash index :0x3baa4
Flow index 0x78: SID :0x 10b00 DID :0x 40b00 VF_ID :0x 80
RX_PORT :0x31
Hash index :0x3bf90
Flow index 0x9f: SID :0x 10b00 DID :0x 40900 VF_ID :0x 80
RX_PORT :0x31
Hash index :0x3c6c0
Flow index 0xa3: SID :0x 11900 DID :0x 10c00 VF_ID :0x 80
RX_PORT :0x25
Hash index :0x3c998
Flow index 0x65: SID :0x 11900 DID :0x 10a00 VF_ID :0x 80
RX_PORT :0x25
Hash index :0x3caa0
Flow index 0x50: SID :0x 11000 DID :0x 12600 VF_ID :0x 80
RX_PORT :0x2e
Hash index :0x3df64
Flow index 0x85: SID :0x 11000 DID :0x 11000 VF_ID :0x 80
RX_PORT :0x2e
Hash index :0x3e400
Flow index 0x67: SID :0x 10a00 DID :0x 10c00 VF_ID :0x 80
RX_PORT :0x32
Hash index :0x3e5fc
Flow index 0xb6: SID :0x 12500 DID :0x 10c00 VF_ID :0x 80
RX_PORT :0x1c
Hash index :0x3eaa4
Flow index 0xb3: SID :0x 12500 DID :0x 10a00 VF_ID :0x 80
RX_PORT :0x1c
Hash index :0x3eb58
Flow index 0xa2: SID :0x 10a00 DID :0x 10a00 VF_ID :0x 80
RX_PORT :0x32
Hash index :0x3f370
Flow index 0xa4: SID :0x 11700 DID :0x 10b00 VF_ID :0x 80
RX_PORT :0x28

Usage count 187

Dynamic traps installed:

IUs pending queue for dynamic trap:

IUs pending queue for zone check:

*****Mirror resources
Information*****

| | | | | | | | |
|---------|---|---|---|---|---|---|---|
| MPHDR0: | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | | | | | | |
| MPHDR1: | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | | | | | | |
| MPHDR2: | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | | | | | | |
| MPHDR3: | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | | | | | | |

| | | | | | | | | |
|----------|---|---|---|---|---|---|---|---|
| MPTXPT0: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| MPTXPT1: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| MPTXPT2: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| MPTXPT3: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

mp_egid = 0
mp_egid = 0
mp_egid = 0
mp_egid = 0

| | | | | | | |
|-------------------|---|---|---|---|---|---|
| RFM blk_usage = | 0 | 0 | 0 | 0 | 0 | 0 |
| mphdr_in_use[0] = | 0 | | | | | |
| mphdr_in_use[1] = | 0 | | | | | |
| mphdr_in_use[2] = | 0 | | | | | |
| mphdr_in_use[3] = | 0 | | | | | |

ipm_port = 0x0 opm_port = 0x0 opm_port_valid = 0x0

frame_cap_en = 0 frame_cap_count = 0
num_np_mr_flows = 0

portFcPortCmdShow --slot 0 57 3
doing portFcPortCmdShow: arg1 = 3, arg2 = -2

portshow 57
portDisableReason: None
portCFlags: 0x0
portFlags: 0x4021 PRESENT U_PORT DISABLED LED
LocalSwcFlags: 0x0
portType: 26.0
POD Port: Need license to enable the port
portState: 2 Offline
Protocol: FC
portPhys: 2 No_Module portScn: 2 Offline
port generation number: 0
state transition count: 0

```

portId:      013900
portIfId:    43020002
portWwn:     20:39:d8:1f:cc:2c:99:90
portWwn of device(s) connected:
16b Area list:
Distance:    normal
portSpeed:   N32Gbps

```

```

FEC: Inactive
Credit Recovery: Inactive
LE domain: 0
Peer beacon: Off
FC Fastwrite: OFF

```

```

Interrupts:      0          Link_failure: 0          Frjt:
0
Unknown:         0          Loss_of_sync: 0         Fbsy:
0
Lli:             0          Loss_of_sig: 0
Proc_rqrd:       0          Protocol_err: 0
Timed_out:       0          Invalid_word: 0
Tx_unavail:      0          Invalid_crc: 0
Delim_err:       0          Address_err: 0
Lr_in:           0          Ols_in: 0
Lr_out:          0          Ols_out: 0

```

```
portloginshow 57
```

```

Type  PID      World Wide Name          credit df_sz cos
=====

```

```
portloginshow 57 -history
```

```

Type  PID      World Wide Name          logout time
=====

```

```
portregshow 57
```

```
LED registers
```

```

=====
0x81c12000: c4_led_status          00000000    0x81c12004:
c4_led_ctl          00000000

```

```
FPL registers
```

```

=====
0x81c10200: fpl_port_config          23490000
0x81c1020c: fpl_port_id_ctl          00000000    0x81c10210:
fpl_port_id_addr    00013900
0x81c10214: fpl_port_speed          00000004    0x81c1021c:
fpl_lli_ctl         00000903
0x81c10228: fpl_lli_os_ctl          bc95b5b5    0x81c1022c:
fpl_lli_send_word   bc95b5b5
0x81c10230: fpl_lli_mark_rx          00000000    0x81c10234:

```

```

fpl_lli_rnd_trip_time 00000000
0x81c10238: fpl_lli_ns_status 80070007 0x81c1023c:
fpl_lli_intr_status 80070007
0x81c10244: fpl_lli_def 00000000 0x81c10254:
fpl_lli_intr_enable_clr 00100000
0x81c10258: fpl_err_intr_status 00000000 0x81c10260:
fpl_err_intr_enable_clr 00000000
0x81c10268: fpl_err_first_error 00000000 0x81c1026c:
fpl_speed_neg_ctl 00000000
0x81c10270: fpl_speed_neg_stat 00000000 0x81c10274:
fpl_softasn_ctl 0000000f
0x81c10278: fpl_link_init_ctl 00000000 0x81c1027c:
fpl_link_init_stat 00000000
0x81c10280: fpl_aec_ctl 00051060 0x81c10284:
fpl_aec_ctl2 04009f60
0x81c10288: fpl_pcs_ctl 00000160 0x81c1028c:
fpl_fec_ctl 00000441
0x81c10290: fpl_fec_cor 00000000 0x81c10294:
fpl_fec_uncor 00000000
0x81c10298: fpl_hss_link_ctl 0031f040 0x81c1029c:
fpl_afifo_link_ctl 00000a86
0x81c102a0: fpl_echo_lb_ctl 0000028c 0x81c102a4:
fpl_scratch 00000121
0x81c102a8: fpl_debug 00030005 0x81c102ac:
fpl_misc_debug 00001800
0x00000000: SW_shadow_reg 00000000 0x00000000:
SW_c4_phy->cfgptr 00030000

```

per-fpg (per octet) registers

```

=====
0x8180382c: fpg_serdes_ctla0 81a37be7 0x81803830:
fpg_serdes_ctla1 81a37be7
0x81803834: fpg_serdes_ctlb0 81a1c3c3 0x81803838:
fpg_serdes_ctlb1 81a1c3c3
0x8180383c: fpg_serdes_xgmii_1ms 00067c28 0x81803840:
fpg_serdes_regtimctl 40e47946
0x81803844: fpg_serdes_asnrsttimctl 00000102

```

HSS PLL registers

```

=====
0x81801400: 00_hssplla_vco_coarse_cal0 00000000 0x81801404:
01_hssplla_vco_coarse_cal1 00000014
0x81801408: 02_hssplla_vco_coarse_cal2 00000000 0x8180140c:
03_hssplla_vco_coarse_cal3 00000000
0x81801410: 04_hssplla_vco_coarse_cal4 00000000 0x81801424:
09_hssplla_power_ctl 00000000
0x81801428: 0A_hssplla_charge_pump_ctl 00000004 0x81801438:
0E_hssplla_pll_misc_ctl 00000000
0x8180143c: 0F_hssplla_pclk_ctl 000000f8 0x81801440:
10_hssplla_eyem_intv_ctl 00000000
0x81801444: 11_hssplla_eyem_intv_lim1 00000000 0x81801448:
12_hssplla_eyem_intv_lim2 00000000
0x8180144c: 13_hssplla_eyem_intv_lim3 00000000 0x81801450:
14_hssplla_eyem_intv_lim4 00000000

```

| | | | |
|-------------|----------------------------|----------|-------------|
| 0x818014f0: | 3C_hssplla_macro_tst_ctl4 | 00000000 | 0x818014f4: |
| | 3D_hssplla_macro_tst_ctl3 | 00000000 | |
| 0x818014f8: | 3E_hssplla_macro_tst_ctl2 | 00000000 | 0x818014fc: |
| | 3F_hssplla_macro_tst_ctl1 | 00000000 | |
| 0x81801500: | 00_hsspllb_vco_coarse_cal0 | 0000000a | 0x81801504: |
| | 01_hsspllb_vco_coarse_cal1 | 00000014 | |
| 0x81801508: | 02_hsspllb_vco_coarse_cal2 | 00000000 | 0x8180150c: |
| | 03_hsspllb_vco_coarse_cal3 | 00000000 | |
| 0x81801510: | 04_hsspllb_vco_coarse_cal4 | 00000000 | 0x81801524: |
| | 09_hsspllb_power_ctl | 00000000 | |
| 0x81801528: | 0A_hsspllb_charge_pump_ctl | 00000004 | 0x81801538: |
| | 0E_hsspllb_pll_misc_ctl | 00000000 | |
| 0x8180153c: | 0F_hsspllb_pclk_ctl | 000000f8 | 0x81801540: |
| | 10_hsspllb_eyem_intv_ctl | 00000000 | |
| 0x81801544: | 11_hsspllb_eyem_intv_lim1 | 00000000 | 0x81801548: |
| | 12_hsspllb_eyem_intv_lim2 | 00000000 | |
| 0x8180154c: | 13_hsspllb_eyem_intv_lim3 | 00000000 | 0x81801550: |
| | 14_hsspllb_eyem_intv_lim4 | 00000000 | |
| 0x818015f0: | 3C_hsspllb_macro_tst_ctl4 | 00000000 | 0x818015f4: |
| | 3D_hsspllb_macro_tst_ctl3 | 00000000 | |
| 0x818015f8: | 3E_hsspllb_macro_tst_ctl2 | 00000000 | 0x818015fc: |
| | 3F_hsspllb_macro_tst_ctl1 | 00000000 | |

HSS TX registers

=====

| | | | |
|-------------|----------------------------|----------|-------------|
| 0x81800400: | 00_hsstx_cfg_mode_PHY | 00009f48 | 0x81800404: |
| | 01_hsstx_test_ctl | 00000000 | |
| 0x81800408: | 02_hsstx_coeff_ctl_INV | 00000000 | 0x8180040c: |
| | 03_hsstx_drv_mode_ctl | 00000000 | |
| 0x81800410: | 04_hsstx_drv_ovrd_ctl | 00000010 | 0x81800414: |
| | 05_hsstx_dclk_align_ovrd | 00000080 | |
| 0x81800418: | 06_hsstx_imp_cal_ovrd | 00000c0c | 0x8180041c: |
| | 07_hsstx_dclk_drift_tol | 00000004 | |
| 0x81800420: | 08_hsstx_tap0_coeff_TUNE | 00000000 | 0x81800424: |
| | 09_hsstx_tap1_coeff_TUNE | 00000003 | |
| 0x81800428: | 0A_hsstx_tap2_coeff_TUNE | 00000018 | 0x8180042c: |
| | 0B_hsstx_tap3_coeff_TUNE | 0000000d | |
| 0x81800434: | 0D_hsstx_pol_INV | 0000000a | 0x81800438: |
| | 0E_hsstx_ae_cmd | 00000000 | |
| 0x8180043c: | 0F_hsstx_ae_stat | 00000000 | 0x81800440: |
| | 10_hsstx_ae_tap0_TUNE | 00000000 | |
| 0x81800444: | 11_hsstx_ae_tap1_TUNE | 00000000 | 0x81800448: |
| | 12_hsstx_ae_tap2_TUNE | 00000028 | |
| 0x8180044c: | 13_hsstx_ae_tap3_TUNE | 00000000 | 0x81800454: |
| | 15_hsstx_app_tune | 0000120e | |
| 0x81800458: | 16_hsstx_analog_diag | 00000000 | 0x81800460: |
| | 18_hsstx_4x_seg_app | 0000aafa | |
| 0x81800464: | 19_hsstx_2x_seg_app | 00000000 | 0x81800468: |
| | 1A_hsstx_1x_seg_app | 0000ff5d | |
| 0x8180046c: | 1B_hsstx_seg_4x_term_app | 00000000 | 0x81800470: |
| | 1C_hsstx_seg_2x1x_term_app | 00000f00 | |
| 0x81800474: | 1D_hsstx_tap_sign_app | 0000000a | 0x81800478: |
| | 1E_hsstx_ext_addr_data | 00000001 | |
| 0x8180047c: | 1F_hsstx_ext_addr_addr | 00000000 | 0x81800480: |

| | | | |
|---|----------|----------|-------------|
| 20_hsstx_pat_buf_bytes_1_0 | 00000000 | | |
| 0x81800484: 21_hsstx_pat_buf_bytes_3_2 | 00000000 | 00000000 | 0x81800488: |
| 22_hsstx_pat_buf_bytes_5_4 | 00000000 | | |
| 0x8180048c: 23_hsstx_pat_buf_bytes_7_6 | 00000000 | 00000000 | 0x8180049c: |
| 27_hsstx_8023az_ctl | 00000000 | | |
| 0x818004a0: 28_hsstx_dcc_ctl | | 000060c0 | 0x818004a4: |
| 29_hsstx_dcc_ovrd | 00000000 | | |
| 0x818004a8: 2A_hsstx_dcc_app | | 00000101 | 0x818004ac: |
| 2B_hsstx_dcc_timeout | 0000ffff | | |
| 0x818004c0: 30_hsstx_tap_sign_ovrd | 00000000 | 00000000 | 0x818004c8: |
| 32_hsstx_seg_4x_ovrd | 00000000 | | |
| 0x818004cc: 33_hsstx_seg_2x_ovrd | | 00000000 | 0x818004d0: |
| 34_hsstx_seg_1x_ovrd | 00000000 | | |
| 0x818004d8: 36_hsstx_tap_seg_4x_term_ovrd | 00000000 | 00000000 | 0x818004dc: |
| 37_hsstx_tap_seg_2x_term_ovrd | 00000000 | | |
| 0x818004e0: 38_hsstx_tap_seg_1x_term_ovrd | 00000000 | 00000000 | 0x818004ec: |
| 3B_hsstx_mac_test_ctl5 | 00000000 | | |
| 0x818004f0: 3C_hsstx_mac_test_ctl4 | | 00000000 | 0x818004f4: |
| 3D_hsstx_mac_test_ctl3 | 00000000 | | |
| 0x818004f8: 3E_hsstx_mac_test_ctl2 | | 00000000 | 0x818004fc: |
| 3F_hsstx_mac_test_ctl1 | 000000c6 | | |

HSS RX registers

=====

| | | | |
|---|----------|----------|-------------|
| 0x81800600: 00_hssrx_cfg_mode_PHY | 00009e78 | | 0x81800604: |
| 01_hssrx_test_ctl | 00000000 | | |
| 0x81800608: 02_hssrx_phs_rot_ctl | | 0000cb80 | 0x8180060c: |
| 03_hssrx_phs_rot_ofs_ctl | 00000610 | | |
| 0x81800610: 04_hssrx_phs_rot_posn1 | | 00002d2c | 0x81800614: |
| 05_hssrx_phs_rot_posn2 | 0000001c | | |
| 0x81800618: 06_hssrx_phs_rot_sta_ofs1 | | 00000001 | 0x8180061c: |
| 07_hssrx_phs_rot_sta_ofs2 | 00000000 | | |
| 0x81800620: 08_hssrx_dfe_ctl_PHY | | 00002002 | 0x81800624: |
| 09_hssrx_dfe_smpl_snap1 | 00000000 | | |
| 0x81800628: 0A_hssrx_dfe_smpl_snap2 | | 00008000 | 0x8180062c: |
| 0B_hssrx_vga_ctl1 | 00004018 | | |
| 0x81800630: 0C_hssrx_vga_ctl2 | | 00007aa0 | 0x81800634: |
| 0D_hssrx_vga_ctl3 | 000009e4 | | |
| 0x81800638: 0E_hssrx_pwr_mgmt_ctl | | 0000001f | 0x8180063c: |
| 0F_hssrx_iqamp_ctl1 | 00000019 | | |
| 0x81800640: 10_hssrx_iqamp_ctl2 | | 00000005 | 0x81800644: |
| 11_hssrx_dacap_dacan_sel | 00000003 | | |
| 0x81800648: 12_hssrx_dacap_dacan | | 0000fffe | 0x8180064c: |
| 13_hssrx_daca_min | 00000000 | | |
| 0x81800650: 14_hssrx_adac_ctl | | 000000ff | 0x81800654: |
| 15_hssrx_ac_cp_ctl | 000031c3 | | |
| 0x81800658: 16_hssrx_ac_cp_val | | 0000804d | 0x8180065c: |
| 17_hssrx_dfe_h1h2h3_lcl_off_ch | 00000014 | | |
| 0x81800660: 18_hssrx_dfe_h1h2h3_lcl_off_val | 00000000 | 00000000 | 0x81800664: |
| 19_hssrx_peaked_intg | 000000ff | | |
| 0x81800668: 1A_hssrx_cdr_analog_sw | | 0000ce00 | 0x8180066c: |
| 1B_hssrx_peaking_amp_init_c_PHY | 00000000 | | |
| 0x81800670: 1C_hssrx_dac_dpc | | 00000040 | 0x81800674: |
| 1D_hssrx_ddc | 00000000 | | |

| | | | |
|--|-----------|-------------|--|
| 0x81800678: 1E_hssrx_int_stat_PHY | 0000c0f | 0x8180067c: | |
| 1F_hssrx_dfe_func_ctl1_PHY | 0000ffff | | |
| 0x81800680: 20_hssrx_dfe_func_ctl2_INV | 00007ebf | 0x81800684: | |
| 21_hssrx_ofs_ch_dcc_qcc_idx | 00002000 | | |
| 0x81800688: 22_hssrx_dfe_ofs_val | 00007d08 | 0x8180068c: | |
| 23_hssrx_h_coeff_bist | 00000401 | | |
| 0x81800690: 24_hssrx_ac_cap_bist | 00000000 | 0x81800694: | |
| 25_hssrx_max_gain_path_idx_res | 00007800 | | |
| 0x81800698: 26_hssrx_loff_ctl | 00000054 | 0x8180069c: | |
| 27_hssrx_sigdet_ctl | 00002180 | | |
| 0x818006a0: 28_hssrx_ana_ctl_sw | 00000000 | 0x818006a4: | |
| 29_hssrx_intg_dac_ofs | 0000dedf | | |
| 0x818006a8: 2A_hssrx_eye_ctl | 00000000 | 0x818006ac: | |
| 2B_hssrx_eye_met | 00000004 | | |
| 0x818006b0: 2C_hssrx_eye_met_err_cnt | 00000000 | 0x818006b4: | |
| 2D_hssrx_eye_met_pdf_eyec | 00000000 | | |
| 0x818006b8: 2E_hssrx_eye_met_pat_len | 0000007f | 0x818006bc: | |
| 2F_hssrx_dfe_func_ctl3 | 0000dfff | | |
| 0x818006c0: 30_hssrx_dfe_tap_ctl_idx_ptr | 00000008 | 0x818006c4: | |
| 31_hssrx_dfe_tap | 00003030 | | |
| 0x818006c8: 32_hssrx_lte_ctl_TUNE | 00001601 | 0x818006e4: | |
| 39_hssrx_int_stat2 | 000041ff | | |
| 0x818006e8: 3A_hssrx_ac_cpl_cur_src_adj | 00000040 | 0x818006ec: | |
| 3B_hssrx_dcd_ctl | 00007c41 | | |
| 0x818006f0: 3C_hssrx_dcc_ctl | 00000d81 | 0x818006f4: | |
| 3D_hssrx_qcc_ctl | 00006989 | | |
| 0x818006f8: 3E_hssrx_mac_test_ctl2 | 00000000 | 0x818006fc: | |
| 3F_hssrx_mac_test_ctl1 | 00000000 | | |
| 0x81800648: 12_hssrx_dacap_dacan[02] | 00fe fffe | | |
| 0x81800660: 18_hssrx_dfe_h1h2h3_lcl_off_va[00] | 0000 0000 | 0000 | |
| 0000 0000 0000 0000 0000 | | | |
| 0x81800660: 18_hssrx_dfe_h1h2h3_lcl_off_va[08] | 0000 0000 | 0000 | |
| 0000 0000 0000 0000 0000 | | | |
| 0x81800660: 18_hssrx_dfe_h1h2h3_lcl_off_va[16] | 0000 0000 | 0000 | |
| 0000 0000 | | | |
| 0x81800688: 22_hssrx_dfe_ofs_val[00][00] | 7d08 007f | 017e | |
| 7f00 7d01 0000 | | | |
| 0x81800688: 22_hssrx_dfe_ofs_val[03][00] | 7b03 007f | 077f | |
| 7f00 7e7c 0000 | | | |
| 0x81800688: 22_hssrx_dfe_ofs_val[06][00] | 7f02 7f7f | 000b | |
| 007f 797b 0000 | | | |
| 0x81800688: 22_hssrx_dfe_ofs_val[09][00] | 077d 7f00 | 7d7c | |
| 0000 0001 0000 | | | |
| 0x81800688: 22_hssrx_dfe_ofs_val[12][00] | 077b 7f00 | 7d06 | |
| 007f 0505 7f7f | | | |
| 0x81800688: 22_hssrx_dfe_ofs_val[15][00] | 7f7b 0000 | 7e7d | |
| 0000 0100 0000 | | | |
| 0x81800688: 22_hssrx_dfe_ofs_val[18][00] | 057d 7f00 | 0702 | |
| 0000 0007 007f | | | |
| 0x81800688: 22_hssrx_dfe_ofs_val[21][00] | 0007 007f | 0007 | |
| 007f 0007 007f | | | |
| 0x81800688: 22_hssrx_dfe_ofs_val[24][00] | 0101 0000 | 7a78 | |
| 0101 027d 0000 | | | |
| 0x81800694: 25_hssrx_max_gain_path_idx_res[00] | 0057 0843 | 100d | |


```

18a6 20cf 289a 3082 3800
0x81800694: 25_hssrx_max_gain_path_idx_res[08]      409f 4875 506b
5800 6040 6800 70fd 7800
0x818006c4: 31_hssrx_dfe_tap[00]                        fffe 8080 0000
0000 0030 0030 3030 3030
0x818006c4: 31_hssrx_dfe_tap[08]                        3030 3030 3030
0000
0x818006e8: 3A_hssrx_ac_cpl_cur_src_adj[00]                0040 0040 0040
0040
0x818006ec: 3B_hssrx_dcd_ctl[00]                            7c41 5c00 7c81
5c00 7c81
0x818006f0: 3C_hssrx_dcc_ctl[00]                            0d81 0d83 0d82
0d83
0x818006f4: 3D_hssrx_qcc_ctl[00]                        6984 6989

```

xfipcs, fec, aec, & aet registers

=====

```

0x81c10400: xfipcs_reg [00] 00002040 00000080 00000000
00000000 00000001 00000008 00000000 00000000
0x81c10420: xfipcs_reg [08] 00008c01 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c10440: xfipcs_reg [16] 00000000 00000000 00000000
00000000 00000040 00000000 00000000 00000000
0x81c10460: xfipcs_reg [24] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c10480: xfipcs_reg [32] 00000004 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c10620: fec_32g_128g_reg [08] 00000000 00000000 00000000
00000000 00000000 00000000 00000000
0x81c10648: fec_32g_128g_reg [18] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c10a00: aec_reg [00] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c10c00: aet_reg [00] 00000000 00000000 00000000
00000000 00000000

```

bbc registers

=====

```

0x81c11800: bbc_trc 0 0 0 0 0 0 0
0
0x81c11840: bbc_trc 0 0 0 0 0 0 0
0
0x81c11880: bbc_trc 0 0 0 0 0 0 0
0
0x81c118c0: bbc_trc 0 0 0 0 0 0 0
0
0x81c11900: bbc_trc 0 0 0 0 0 0 0
0
0x81c11804: bbc_mbc 0 0 0 0 0 0 0
0
0x81c11844: bbc_mbc 0 0 0 0 0 0 0
0
0x81c11884: bbc_mbc 0 0 0 0 0 0 0
0

```

| | | | | | | | |
|-------------------------------------|----------|---|---|---|---|---|----------------------|
| 0x81c118c4: bbc_mbc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c11904: bbc_mbc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c11a00: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c11a20: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c11a40: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c11a60: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c11a80: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c11c00: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c11c20: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c11c40: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c11c60: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c11c80: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c11d00: bbc_fbpc | 00000000 | | | | | | |
| 00000000 | | | | | | | 0x81c11d04: bbc_csc |
| 0x81c11d08: bbc_rcc_inc | 00000000 | | | | | | 0x81c11d0c: |
| bbc_rqc_inc | 00000000 | | | | | | |
| 0x81c11d10: bbc_fbpc_inc | 00000000 | | | | | | 0x81c11d14: |
| bbc_tmc_inc | 00000000 | | | | | | |
| 0x81c11d18: bbc_threshold | 00080100 | | | | | | 0x81c11d1c: |
| bbc_counter_clr | 00000000 | | | | | | |
| 0x81c11d20: bbc_debug_en | 00000000 | | | | | | 0x81c11d24: bbc_ctrl |
| 00200020 | | | | | | | |
| 0x81c11d28: bbc_rqc_rcc_thresh | 00000055 | | | | | | 0x81c11d34: |
| bbc_bb_sc_n | 00000000 | | | | | | |
| 0x81c11d38: bbc_crd_reco_debug | 00000000 | | | | | | 0x81c11d3c: |
| bbc_crd_reco_debug_data | 00000000 | | | | | | |
| 0x81c11d40: bbc_multi_frm_loss_cnt | 00000000 | | | | | | 0x81c11d44: |
| bbc_multi_rdy_loss_cnt | 00000000 | | | | | | |
| 0x81c11d48: bbc_1frm_loss_recov_cnt | 00000000 | | | | | | 0x81c11d4c: |
| bbc_1rdy_loss_recov_cnt | 00000000 | | | | | | |
| 0x81c11d58: bbc_int_status | 00000000 | | | | | | 0x81c11d5c: |
| bbc_int_set | 00000000 | | | | | | |
| 0x81c11d60: bbc_int_first | 00000000 | | | | | | 0x81c11d64: |
| bbc_frm_rdy_rx_err_addr | 00000000 | | | | | | |
| 0x81c11d68: bbc_frm_rdy_tx_err_addr | 00000000 | | | | | | 0x81c11d6c: |
| bbc_trc_mbc_err_addr | 00000000 | | | | | | |
| 0x81c11d70: bbc_frm_rdy_rx_dbl_ecc | 00000000 | | | | | | 0x81c11d74: |
| bbc_frm_rdy_tx_dbl_ecc | 00000000 | | | | | | |
| 0x81c11d78: bbc_trc_mbc_dbl_ecc | 00000000 | | | | | | |
| 0x81c11d7c: bbc_fsm_status | 00001011 | | | | | | 0x81c11d80: |
| bbc_force_err | 00000000 | | | | | | |
| 0x81c11d84: bbc_crtd_avail0 | ffffffff | | | | | | 0x81c11d88: |

bbc_crdt_avail1 000000ff
0x81c11d8c: bbc_scratch 00000000

FPS registers

=====

0x81c10004: fps_er_enc_in 00000000 0x81c10008:
fps_er_crc 00000000
0x81c1000c: fps_er_trunc 00000000 0x81c10010:
fps_er_toolong 00000000
0x81c10014: fps_er_bad_eof 00000000 0x81c10018:
fps_er_enc_out 00000000
0x81c1001c: fps_er_bad_os 00000000 0x81c10020:
fps_er_flush 00000000
0x81c10024: fps_er_ifg 00000000 0x81c10038:
fps_er_crc_good_eof 00000000
0x81c1003c: fps_inv_arb 00000000 0x81c10040:
fps_slow_sts_status 00000000
0x81c10044: fps_tx_frm_cnt 00000000 0x81c10048:
fps_rx_frm_cnt 00000000
0x81c10050: fps_tx_word_cnt_hi 00000000 0x81c1004c:
fps_tx_word_cnt_lo 00000000
0x81c10058: fps_rx_word_cnt_hi 00000000 0x81c10054:
fps_rx_word_cnt_lo 00000000

BAL registers

=====

0x81c17000: bal_desired_buf 00000000 0x81c17004:
bal_alloc_buf 00000000
0x81c17008: bal_busy_buf 00000000 0x81c1700c:
bal_usable_buf 00000000
0x81c17010: bal_max_bor_buf 00000000
0x81c17014: bal_busy_buf_thresh 00000002

TXQ registers

=====

0x81c13004: txq_phys_port_ctl 00420000
0x81c13050: txq_link_skew 00000000
0x81c13068: txq_cr_lk_dttm_intr_sts [00] 00000000 00000000
0x81c13070: txq_cr_lk_dttm_intr_en [00] 00000000 00000000
0x81c13024: txq_disc_frm_trap_cnt 00000014

FDS registers

=====

0x81c14000: fds_rxf_ctl 00000002 0x81c14004:
fds_rxf_wait_thresh 00000909
0x81c14018: fds_rxf_first_error 00000000 0x81c1401c:
fds_rxf_first_error_info 00000000
0x81c14020: fds_rxf_inout_pkt_cnt 00000000
0x81c14008: fds_rxf_err_int_status 00000000 0x81c14024:
fds_rxf_fifo_status 00888888
0x81c15000: fds_txf_ctl 0000003a 0x81c15004:
fds_txf_wait_ifg_thresh 00a00106
0x81c15008: fds_txf_err_int_status 00000000 0x81c15024:
fds_txf_fifo_status 00088888

0x81c1502c: fds_txf_bbc_scs 00000000

Logical TXQ registers

=====

| | | |
|------------------------------------|---------------------------------|-------------|
| 0x81c13000: txq_log_port_ctl | 00000002 | 0x81c13008: |
| txq_port_status | 00000000 | |
| 0x81c1300c: txq_todo_flags | [00] 00000000 00000000 | |
| 0x81c13014: txq_spd_match_desc | [00] 00000000 00000000 00000000 | |
| 00000000 | | |
| 0x81c13024: txq_spd_match_desc | [04] 00000014 | |
| 0x81c13028: txq_vc_weight | [00] 01010101 01010101 01010101 | |
| 01010101 | | |
| 0x81c13038: txq_vc_weight | [04] 01010101 01010101 01010101 | |
| 01010101 | | |
| 0x81c13048: txq_vc_weight | [08] 01010101 00010101 | |
| 0x81c13054: txq_cong_dttm_ctrl | 00000000 | |
| 0x81c13058: txq_cong_dttm_intr_sts | [00] 00000000 00000000 | |
| 0x81c13060: txq_cong_dttm_intr_en | [00] 00000000 00000000 | |
| 0x81c13078: txq_bw_limit_en_reg | [00] 00000000 00000000 | |
| 0x81c13080: txq_bw_gua_en_reg | [00] 00000000 00000000 | |
| 0x81c13088: txq_vc_group | [00] 03030300 03030303 03030303 | |
| 03030303 | | |
| 0x81c13098: txq_vc_group | [04] 03030303 03030303 03030303 | |
| 03030303 | | |
| 0x81c130a8: txq_vc_group | [08] 03030303 03030303 00000000 | |
| 00000000 | | |
| 0x81c130b0: txq_bw_thresh_group | [00] 00000000 00000000 00000000 | |
| 00000000 | | |
| 0x81c130c0: txq_bw_thresh_group | [04] 00000000 00000000 00000000 | |
| 00000000 | | |
| 0x81c130d0: txq_bw_thresh_group | [08] 00000000 00000000 00000000 | |
| 00000000 | | |
| 0x81c130e0: txq_bw_thresh_group | [12] 00000000 00000000 00000000 | |
| 00000000 | | |
| 0x81c130f0: txq_bw_thresh_group | [16] 00000000 00000000 00000000 | |
| 00000000 | | |
| 0x81c13100: txq_bw_thresh_group | [20] 00000000 00000000 00000000 | |
| 00000000 | | |
| 0x81c13110: txq_bw_thresh_group | [24] 00000000 00000000 00000000 | |
| 00000000 | | |
| 0x81c13120: txq_bw_thresh_group | [28] 00000000 00000000 00000000 | |
| 00000000 | | |
| 0x81c13130: txq_bw_thresh_group | [32] 00000000 00000000 00000000 | |
| 00000000 | | |
| 0x81c13140: txq_bw_thresh_group | [36] 00000000 00000000 00000000 | |
| 00000000 | | |

txq Congestion detection Statistics RAM

=====

| | | |
|-------------------|----------|-------------------|
| 0x81090140: vc[0] | 00000000 | 0x81090144: vc[1] |
| 00000000 | | |
| 0x81090148: vc[2] | 00000000 | 0x8109014c: vc[3] |
| 00000000 | | |
| 0x81090150: vc[4] | 00000000 | 0x81090154: vc[5] |

```

00000000
0x81090158: vc[6]      00000000      0x8109015c: vc[7]
00000000
0x81090160: vc[8]      00000000      0x81090164: vc[9]
00000000
0x81090168: vc[10]     00000000      0x8109016c: vc[11]
00000000
0x81090170: vc[12]     00000000      0x81090174: vc[13]
00000000
0x81090178: vc[14]     00000000      0x8109017c: vc[15]
00000000
0x81090180: vc[16]     00000000      0x81090184: vc[17]
00000000
0x81090188: vc[18]     00000000      0x8109018c: vc[19]
00000000
0x81090190: vc[20]     00000000      0x81090194: vc[21]
00000000
0x81090198: vc[22]     00000000      0x8109019c: vc[23]
00000000
0x810901a0: vc[24]     00000000      0x810901a4: vc[25]
00000000
0x810901a8: vc[26]     00000000      0x810901ac: vc[27]
00000000
0x810901b0: vc[28]     00000000      0x810901b4: vc[29]
00000000
0x810901b8: vc[30]     00000000      0x810901bc: vc[31]
00000000
0x810901c0: vc[32]     00000000      0x810901c4: vc[33]
00000000
0x810901c8: vc[34]     00000000      0x810901cc: vc[35]
00000000
0x810901d0: vc[36]     00000000      0x810901d4: vc[37]
00000000
0x810901d8: vc[38]     00000000      0x810901dc: vc[39]
00000000

```

Logical STS registers

=====

```

0x81584204: sts_ftb_type1_miss      00000000
0x81584208: sts_ftb_type2_miss      00000000
0x8158420c: sts_ftb_type6_miss      00000000
0x81584210: sts_hard_zoning_miss     00000000
0x81584214: sts_lun_zoning_miss     00000000
0x8158421c: sts_unroutable          00000000
0x81581234: sts_rte_cl2             00000000      0x81581238:
sts_rte_cl3             00000000      0x8158123c: sts_rte_link_ctl
00000000      0x81584228: sts_tx_timeout      00000000

```

Logical STS filter registers

=====

```

0x81584180: stsflt_trig      [00] 00000000 00000000 00000000
00000000
0x81584190: stsflt_trig      [04] 00000000 00000000 00000000

```

```

00000000
0x815841a0: sts_flt_trig [08] 00000000 00000000 00000000
00000000
0x815841b0: sts_flt_trig [12] 00000000 00000000 00000000
00000000
0x815841c0: sts_flt_trig [16] 00000000 00000000 00000000
00000000
0x815841d0: sts_flt_trig [20] 00000000 00000000 00000000
00000000
0x815841e0: sts_flt_trig [24] 00000000 00000000 00000000
00000000
0x815841f0: sts_flt_trig [28] 00000000 00000000 00000000
00000000
0x81584200: sts_flt_trig [32]

```

Logical STS discard registers

=====

```

0x815812e8: disc_mcast_wka 00000000 0x815812ec:
disc_inv_did 00000000
0x815812f0: disc_cl1_cl4 00000000 0x815812f4:
disc_sid_chk_fail 00000000
0x815812f8: disc_inv_dom_egid_txpt 00000000 0x815812fc:
disc_vft_hop_cnt_1 00000000
0x81581300: disc_classf 00000000 0x81581304:
disc_fcp_cdb_inv 00000000
0x81581308: disc_vfid_trap_enabled 00000000 0x8158130c:
disc_vfid_hdr_chk_fail 00000000
0x81581310: disc_shim_cksum_fail 00000000 0x81581314:
disc_fed_edit_cmd_err 00000000
0x81581318: disc_ftb_vm_mode 00000000 0x8158131c:
disc_ftb_agn_t2_miss 00000000
0x81581320: disc_ecb_reserved 00000000 0x81581324:
disc_ecb_de_pad_err 00000000
0x81581328: disc_ecb_de_tag_err 00000000 0x8158132c:
disc_ecb_de_seq_err 00000000
0x81581330: disc_ecb_err 00000000 0x81581334:
disc_ftb_type4_match 00000000
0x81581338: disc_fcp_rsp_ftb_type4 00000000 0x8158133c:
disc_ftb_type5_match 00000000
0x81581340: disc_ftb_type3_match 00000000 0x81581344:
disc_els_ftb_type3 00000000
0x81581348: disc_ftb_type1_match 00000000 0x8158134c:
disc_els_rsp_ex_port 00000000
0x81581350: disc_inv_drp_dps 00000000 0x81581354:
disc_did_lookup_miss 00000000
0x81581358: disc_ftb_type2_match 00000000 0x8158135c:
disc_trpd_plogi_pdisc 00000000
0x81581360: disc_type2_lookup_miss 00000000 0x81581364:
disc_ftb_type6_match 00000000
0x81581368: disc_els_rep_ex_port 00000000 0x8158136c:
disc_els_sid_lkup_bit1 00000000
0x81581370: disc_els_sid_lkup_bit0 00000000 0x81581374:
disc_bls_frm_trap_bit1 00000000
0x81581378: disc_ftb_token_err 00000000 0x8158137c:

```

```

disc_asic_internal_err 00000000
0x81581380: disc_hard_zone_miss 00000000 0x81581384:
disc_lun_zone_miss 00000000
0x81581388: disc_flt_frame_disc 00000000 0x8158138c:
disc_flt_parity_err 00000000
0x81581390: disc_frame_marked_du 00000000 0x81581394:
disc_frame_marked_to 00000000
0x81581398: disc_lkup_rte_prty_err 00000000

```

portstatsshow 57

```

stat_wtx 0 4-byte words transmitted
stat_wrx 0 4-byte words received
stat_ftx 0 Frames transmitted
stat_frx 0 Frames received
stat_c2_frx 0 Class 2 frames received
stat_c3_frx 0 Class 3 frames received
stat_lc_rx 0 Link control frames
received
stat_mc_rx 0 Multicast frames
received
stat_mc_to 0 Multicast timeouts
stat_mc_tx 0 Multicast frames
transmitted
tim_txcrd_z 0 Time TX Credit Zero
(2.5Us ticks)
tim_txcrd_z_vc 0- 3: 0 0 0 0
tim_txcrd_z_vc 4- 7: 0 0 0 0
tim_txcrd_z_vc 8-11: 0 0 0 0
tim_txcrd_z_vc 12-15: 0 0 0 0
lat_tot_pkt_vc 0- 3: 1 1 1 1
lat_tot_pkt_vc 4- 7: 1 1 1 1
lat_tot_pkt_vc 8-11: 1 1 1 1
lat_tot_pkt_vc 12-15: 1 1 1 1
lat_hi_time_vc 0- 3: 0 0 0 0
lat_hi_time_vc 4- 7: 0 0 0 0
lat_hi_time_vc 8-11: 0 0 0 0
lat_hi_time_vc 12-15: 0 0 0 0
lat_lo_time_vc 0- 3: 1 1 1 1
lat_lo_time_vc 4- 7: 1 1 1 1
lat_lo_time_vc 8-11: 1 1 1 1
lat_lo_time_vc 12-15: 1 1 1 1
max_latency_vc 0- 3: 1 1 1 1
max_latency_vc 4- 7: 1 1 1 1
max_latency_vc 8-11: 1 1 1 1
max_latency_vc 12-15: 1 1 1 1
latency_dma_ts 09-09-2024 UTC Mon 08:47:26 TXQ
Latency DMA TimeStamp
fec_cor_detected 0 Count of blocks that
were corrected by FEC
fec_uncor_detected 0 Count of blocks that
were left uncorrected by FEC
er_enc_in 0 Encoding errors inside
of frames

```

| | | |
|--------------------------|-----------------------------|--------------------------|
| er_crc | 0 | Frames with CRC errors |
| er_trunc | 0 | Frames shorter than |
| minimum | | |
| er_toolong | 0 | Frames longer than |
| maximum | | |
| er_bad_eof | 0 | Frames with bad end-of- |
| frame | | |
| er_enc_out | 0 | Encoding error outside |
| of frames | | |
| er_bad_os | 0 | Invalid ordered set |
| er_pcs_blk | 0 | PCS block errors |
| er_rx_c3_timeout | 0 | Class 3 receive frames |
| discarded due to timeout | | |
| er_tx_c3_timeout | 0 | Class 3 transmit frames |
| discarded due to timeout | | |
| er_unroutable | 0 | Frames that are |
| unroutable | | |
| er_unreachable | 0 | Frame with unreachable |
| destination | | |
| er_other_discard | 0 | Other discards |
| er_type1_miss | 0 | frames with FTB type 1 |
| miss | | |
| er_type2_miss | 0 | frames with FTB type 2 |
| miss | | |
| er_type6_miss | 0 | frames with FTB type 6 |
| miss | | |
| er_zone_miss | 0 | frames with hard zoning |
| miss | | |
| er_lun_zone_miss | 0 | frames with LUN zoning |
| miss | | |
| er_crc_good_eof | 0 | Crc error with good eof |
| er_inv_arb | 0 | Invalid ARB |
| er_single_credit_loss | 0 | Single vcrdy/frame loss |
| on link | | |
| er_multi_credit_loss | 0 | Multiple vcrdy/frame |
| loss on link | | |
| other_credit_loss | 0 | Link timeout/complete |
| credit loss | | |
| phy_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | Timestamp of |
| phy_port stats clear | | |
| lgc_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | Timestamp of |
| lgc_port stats clear | | |
| fec_corrected_rate | 0 | FEC Corrected blocks per |
| second | | |

portstats64show 57

| | | |
|------------|---|---------------------------------------|
| stat64_wtx | 0 | top_int : 4-byte words transmitted |
| | 0 | bottom_int : 4-byte words transmitted |
| stat64_wrx | 0 | top_int : 4-byte words received |
| | 0 | bottom_int : 4-byte words received |
| stat64_ftx | 0 | top_int : Frames transmitted |
| | 0 | bottom_int : Frames transmitted |
| stat64_frx | 0 | top_int : Frames received |
| | 0 | bottom_int : Frames received |

| | | |
|------------------------------|---|--|
| stat64_c2_frx | 0 | top_int : Class 2 frames received |
| | 0 | bottom_int : Class 2 frames received |
| stat64_c3_frx | 0 | top_int : Class 3 frames received |
| | 0 | bottom_int : Class 3 frames received |
| stat64_lc_rx | 0 | top_int : Link control frames received |
| | 0 | bottom_int : Link control frames |
| received | | |
| stat64_mc_rx | 0 | top_int : Multicast frames received |
| | 0 | bottom_int : Multicast frames received |
| stat64_mc_to | 0 | top_int : Multicast timeouts |
| | 0 | bottom_int : Multicast timeouts |
| stat64_mc_tx | 0 | top_int : Multicast frames transmitted |
| | 0 | bottom_int : Multicast frames |
| transmitted | | |
| tim64_rdy_pri | 0 | top_int : Time R_RDY high priority |
| | 0 | bottom_int : Time R_RDY high priority |
| tim64_txcrd_z | 0 | top_int : Time BB_credit zero |
| | 0 | bottom_int : Time BB_credit zero |
| er64_enc_in | 0 | top_int : Encoding errors inside of |
| frames | 0 | bottom_int : Encoding errors inside of |
| frames | | |
| er64_crc | 0 | top_int : Frames with CRC errors |
| | 0 | bottom_int : Frames with CRC errors |
| er64_trunc | 0 | top_int : Frames shorter than minimum |
| | 0 | bottom_int : Frames shorter than minimum |
| er64_toolong | 0 | top_int : Frames longer than maximum |
| | 0 | bottom_int : Frames longer than maximum |
| er64_bad_eof | 0 | top_int : Frames with bad end-of-frame |
| | 0 | bottom_int : Frames with bad end-of- |
| frame | | |
| er64_enc_out | 0 | top_int : Encoding error outside of |
| frames | 0 | bottom_int : Encoding error outside of |
| frames | | |
| er64_disc_c3 | 0 | top_int : Class 3 frames discarded |
| | 0 | bottom_int : Class 3 frames discarded |
| er64_pcs_blk | 0 | top_int : PCS block errors |
| | 0 | bottom_int : PCS block errors |
| stat64_rateTxFrame | 0 | Tx frame rate (fr/sec) |
| stat64_rateRxFrame | 0 | Rx frame rate (fr/sec) |
| stat64_rateTxPeakFrame | 0 | Tx peak frame rate (fr/sec) |
| stat64_rateRxPeakFrame | 0 | Rx peak frame rate (fr/sec) |
| stat64_rateTxWord | 0 | Tx Word rate (words/sec) |
| stat64_rateRxWord | 0 | Rx Word rate (words/sec) |
| stat64_rateTxPeakWord | 0 | Tx peak Word rate (words/sec) |
| stat64_rateRxPeakWord | 0 | Rx peak Word rate (words/sec) |
| stat64_PRJTFrames | 0 | top_int : Number of PRJT frames |
| returned to this port | 0 | bottom_int : Number of PRJT |
| frames returned to this port | | |
| stat64_PBSYFrames | 0 | top_int : Number of PBSY frames |
| returned to this port | 0 | bottom_int : Number of PBSY |

```

frames returned to this port
stat64_inputBuffersFull 0          top_int : Number of occurrences
when all input buffers full
                                0          bottom_int : Number of
occurrences when all input buffers full
stat64_rxClass1Frames 0          top_int : Number of class 1
frames received
                                0          bottom_int : Number of class 1
frames received
stat64_aveTxFrameSize 0          Average Tx Frame size
stat64_aveRxFrameSize 0          Average Rx Frame size
Lr_in          0          top_int
                                0          bottom_int
Ols_in         0          top_int
                                0          bottom_int
Lr_out         0          top_int
                                0          bottom_int
Ols_out        0          top_int
                                0          bottom_int
Link_failure   0          top_int
                                0          bottom_int
Invalid_CRC    0          top_int
                                0          bottom_int
Invalid_word   0          top_int
                                0          bottom_int
Protocol_err   0          top_int
                                0          bottom_int
Loss_of_sig    0          top_int
                                0          bottom_int
Loss_of_sync   0          top_int
                                0          bottom_int
er_bad_os      0          top_int : Invalid ordered set
                                0          bottom_int: Invalid ordered set

```

```

portrouteshow 57
port address ID: 0x013900
external unicast routing table:
  0: Embedded
 255: Embedded
internal unicast routing table:
  0: Embedded

```

```
portcamshow 57
```

```

-----
Port  SID used  DID used  SID entries  DID entries
57    0         0        000000     000000
-----

```

```

ptbufshow, ptcreditshow, ptdatashow, ptstatsshow 57
S:
S:VF Enable:          1
S:
S:C4 Global Variable:

```

```

S:-----
-----
S:trace_stop:          0
S:
S:C4 Phy Data Pointers: c4_phyp = 0xb6ab4100
S:-----
-----
S:tnodep                0xbb82d2a0      pt
   0x43028002
S:proto_phyp            0xb8806000      phy_cfg
0xb6ab5140
S:c4_chp                0x97e28000      c4_lgcp
0x97f50000
S:c4_phy_regp          0x81c10000      proc_dir
0xb8512aa0
S:-----
-----
S:magic_id              0xc4345678      num_port_timer    12
S:prev_if_id           0x43020002      S:ftx              0
   tov              0
S:initialized          0                port_idx           2
S:ui_idx               57                slot_no
   0
S:blade_idx            2                sw_usr_ports       400
S:unused               0                intr_debounced
   0
S:aec_status           0x0              reason_code
   0
S:debug                0x00000004      debug_trc_line     0
S:rxbuf_list_head     0xffffffff      rxbuf_list_tail
0xffffffff
S:isAePort             0                port_misc_data
   0
S:num_fault1_rx_disc   0                num_fault2_rx_disc 0
S:p_llli_cause0        0                p_sig_regained     0
S:p_sync_regained      0                enc_out
   0x0
S:cached_fps_status    0                cached_sts_status  0
S:cached_er_crc_good_eof 0
S:cached_er_bad_os     0                cached_er_too_long 0
S:cached_er_trunc      0
cached_tot_er_crc_good_eof 0
S:num_pt_excess_intr   0                num_no_fid         0
S:num_fault1_cnt       0                num_fault2_cnt
   0
S:num_fault_lip        0                num_fault_llli     0
S:num_fault_rx_fifo    0                num_fault_hss      0
S:num_fault_bwait      0                lli_intr_prim
   0
S:num_sw_link_to       0
be_link_err_mon_count  0
S:ecb_enc_enabled      0                ecb_comp_enabled
   0
S:ecb_rsv_enc          0                ecb_rsv_comp       0

```

```

S:ecb_enc_bm          0x0          ecb_key_index
0xffffffff
S:fab_idx            4
S:num_be_lto         0          lto_count_reset_intvl
0
S:lr_count_reset_intvl 0          num_be_lr
0
S:num_fault_qsfp     0          check_lto
0
S:credit_loaded      0          num_credit_overrun
0
S:fec_enabled        0x0          fec_los_to_flag          0x0
S:phy_stats_clear_ts 1725611419 pcs_err_online
0
S:pcs_err_light_det  0          pcs_err_ignore
0
S:pcs_blk_err        0          pcs_hiber                0
S:phy_port_status    0          ecb_enc_lr_count
0
S:dport_mode         0          avoid_lto_det            0
S:sn_debounced       0x0          sn_started_kr_reqd       0
S:major_timer_started 0x0          ready_bm                 0x0
S:parln_1_bm         0x0          parln_0_bm               0x0
S:be_los_of_sync_event_intvl
be_los_of_sync_event 0
S:errataPtenable_cntr 0          errataPoll_cntr
0
S:jda_rx_sig_loss_det 0          jda_rx_sig_loss_cnt
0
S:encrypt_blk_error  0
S:
S:      c4_trunk
S:=====
S:mark_ts            0x0          deskew                    0x0
S:master_phyp        0x0
S:
S:adelay[00]: 0x00000000 0x00000000 0x00000000 0x00000000
S:adelay[04]: 0x00000000 0x00000000 0x00000000 0x00000000
S:
S:      c4_buf
S:=====
S:tx_csc              0          rx_csc
0
S:ld_vc_credits       0          tx_flag                    0x0
S:alloc_buffers       0          req_buffers                 0
S:est_buffers         20          ld_use_est                  0
S:bb_sc_n             0          rx_bb_sc_n
0
S:data_cr             5          nondata_cr
6
S:cr_enable           0
S:ld_nondata_cr       6          tnodep
0xbb82d380
S:tx_credits[0] 0    0    0    0    0    0    0    0

```

```

S:tx_credits[8] 0 0 0 0 0 0 0 0
S:tx_credits[16] 0 0 0 0 0 0 0 0 0 0
S:tx_credits[24] 0 0 0 0 0 0 0 0 0 0
S:tx_credits[32] 0 0 0 0 0 0 0 0 0 0
S:rx_credits[0] 0 0 0 0 0 0 0 0
S:rx_credits[8] 0 0 0 0 0 0 0 0
S:rx_credits[16] 0 0 0 0 0 0 0 0 0 0
S:rx_credits[24] 0 0 0 0 0 0 0 0 0 0
S:rx_credits[32] 0 0 0 0 0 0 0 0 0 0
S:tx_mbc[0] 0 0 0 0 0 0 0 0
S:tx_mbc[8] 0 0 0 0 0 0 0 0
S:tx_mbc[16] 0 0 0 0 0 0 0 0
S:tx_mbc[24] 0 0 0 0 0 0 0 0
S:tx_mbc[32] 0 0 0 0 0 0 0 0
S:rx_mbc[0] 0 0 0 0 0 0 0 0
S:rx_mbc[8] 0 0 0 0 0 0 0 0
S:rx_mbc[16] 0 0 0 0 0 0 0 0
S:rx_mbc[24] 0 0 0 0 0 0 0 0
S:rx_mbc[32] 0 0 0 0 0 0 0 0

```

S:

S:C4 Chip Variables: c4_phy->c4_chp = 0x97e28000

S:-----

S:version = 2.1

S:magic_id 0xc4234567 init_state 0x8

S:reset_reg_mem 0x1

S:ch_int0_en_bm 0x0 intr0_cause 0x0

S:ch_int1_en_bm 0x0 intr1_cause 0x0

S:ch_int2_en_bm 0x0 intr2_cause 0x0

S:ch 0x43010080 ch_cfg

0xb7013ba0

S:raslog_hdl.hndl 0x0 obj_halted 0x0

S:c4_chip_regp 0x80000000 c4_fpg_regp

0x81800000

S:num_chip_timer 0x5

S:hi_task_bm 0x0 lo_task_bm 0x0

S:c4_deferq.q_head 0x0 c4_deferq.q_tail 0x0

S:c4_tmrq.q_head 0x0 c4_tmrq.q_tail 0x0

slot_no 0

S:chip_inst 0 chip_idx 0

S:pll_initialized 1

pll_serdes_initialized 1

S:init_tries 0 init_ptEnableBM

0xba01b488

S:tick_polling 0xb980c9c0 sec_polling

0xb980c960

S:bb_fid 129

S:ecb_key_bm[0] 0x0 ecb_key_bm[1] 0x0

S:ecb_key_bm[2] 0x0 ecb_key_bm[3] 0x0

S:is_chip_enc_enabled 0

is_chip_comp_enabled 0x0

S:ftb_rsrcp->ftb_flags 0x0 act_rsrcp->act_flag 0x1

S:lue_rsrcp->lue_flags[0] 0x0 lue_rsrcp-

>lue_flags[1] 0x0

```

S:c4_phyp[00]: 0xb6ab0000 0xb6ab2080 0xb6ab4100 0xb6ab6180
S:c4_phyp[04]: 0xb6ab9040 0xb6abb0c0 0xb6abd140 0xb6ac0000
S:c4_phyp[08]: 0xb6ac2080 0xb6ac4100 0xb6ac6180 0xb6ac9040
S:c4_phyp[12]: 0xb6acbc0c0 0xb6acd140 0xb6ad0000 0xb6ad2080
S:c4_phyp[16]: 0xb6ad4100 0xb6ad6180 0xb6ad9040 0xb6adb0c0
S:c4_phyp[20]: 0xb6add140 0xb6ae0000 0xb6ae2080 0xb6ae4100
S:c4_phyp[24]: 0xb6ae6180 0xb6ae9040 0xb6aeb0c0 0xb6aed140
S:c4_phyp[28]: 0xb6af0000 0xb6af2080 0xb6af4100 0xb6af6180
S:c4_phyp[32]: 0xb6af9040 0xb6afb0c0 0xb6afd140 0xb6b00000
S:c4_phyp[36]: 0xb6b02080 0xb6b04100 0xb6b06180 0xb6b09040
S:c4_phyp[40]: 0xb6b0bc0c0 0xb6b0d140 0xb6b10000 0xb6b12080
S:c4_phyp[44]: 0xb6b14100 0xb6b16180 0xb6b19040 0xb6b1b0c0
S:c4_phyp[48]: 0xb6b1d140 0xb6b20000 0xb6b22080 0xb6b24100
S:c4_phyp[52]: 0xb6b26180 0xb6b29040 0xb6b2b0c0 0xb6b2d140
S:c4_phyp[56]: 0xb6b30000 0xb6b32080 0xb6b34100 0xb6b36180
S:c4_phyp[60]: 0xb6b39040 0xb6b3b0c0 0xb6b3d140 0xb6b40000
S:c4_lgcp[00]: 0x97f48000 0x97f4c000 0x97f50000 0x97f54000
S:c4_lgcp[04]: 0x97f58000 0x97f5c000 0x97f60000 0x97f64000
S:c4_lgcp[08]: 0x97f68000 0x97f6c000 0x97f70000 0x97f74000
S:c4_lgcp[12]: 0x97f78000 0x97f7c000 0x97f80000 0x97f84000
S:c4_lgcp[16]: 0x97f88000 0x97f8c000 0x97f90000 0x97f94000
S:c4_lgcp[20]: 0x97f98000 0x97f9c000 0x97fa0000 0x97fa4000
S:c4_lgcp[24]: 0x97fa8000 0x97fac000 0x97fb0000 0x97fb4000
S:c4_lgcp[28]: 0x97fb8000 0x97fbc000 0x97fc0000 0x97fc4000
S:c4_lgcp[32]: 0x97fc8000 0x97fcc000 0x97fd0000 0x97fd4000
S:c4_lgcp[36]: 0x97fd8000 0x97fdc000 0x97fe0000 0x97fe4000
S:c4_lgcp[40]: 0x97fe8000 0x97fec000 0x97ff0000 0x97ff4000
S:c4_lgcp[44]: 0x97ff8000 0x97ffc000 0x8e000000 0x8e004000
S:c4_lgcp[48]: 0x8e008000 0x8e00c000 0x8e010000 0x8e014000
S:c4_lgcp[52]: 0x8e018000 0x8e01c000 0x8e020000 0x8e024000
S:c4_lgcp[56]: 0x8e028000 0x8e02c000 0x8e030000 0x8e034000
S:c4_lgcp[60]: 0x8e038000 0x8e03c000 0x8e040000 0x8e044000
S:chip_timers[00]: 0xb980c720 0xb980c780 0xb980c7e0 0xb980c840
S:chip_timers[04]: 0xb980c8a0 0xb980c900
S:disc_trap_enable_required      0x0          rxlp_disc_log_stop
      0x0
S:curr_rxlp_frm_cnt      0x0          curr_rxlp_disc_frm_cnt  0x0
S:sw_disc_frm_cnt      0x0          last_disc_frm_cnt      0x0
S:txq_nopop_pr_cnt      0x0          pollErrataDfe_ptBM
0xba01b4b0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][0]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][1] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][2]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][0] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][1]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][2] 0x0
S:
S:C4 Logical Port Variables
S:-----
-----
S:c4_lgc_regp      0x81c10000
S:c4_phyp:
S:      0xb6ab4100      0x0          0x0          0x0

```

```

S:      0x0          0x0          0x0          0x0

S:master_phyp      0xb6ab4100      if_id
0x43020002
S:min_phyp          0x0          max_phyp          0x0
S:num_phy_ports    1          lgc_num          2
S:num_iu_to        0          sw_txq_bm
0
S:port_fid         129          unused          0
S:port_group       0          lgc_stats_clear_ts
1725611419
S:domain_tbl_sel  0          area_tbl_sel
0
S:egid_tbl_sel     0
S:serv_lo_bm       0x0
S:
S:Proto Phy Variables:
S:-----
-----
S:magic_id         0xc4123456      asic_phyp
0xb6ab4100
S:port_id          0x43028002      phy_cfg
0xb6ab5140
S:upsm_hdl         0xb800f960      physm_hdl
0xb800f6e0
S:ov_snsn_hdl      0xb800f5a0      sw_snsn_hdl
0xb800f640
S:ov_lksm_hdl      0xb800f780      sw_lksm_hdl
0xb800f820
S:trksm_hdl        0xb800f8c0      lr_flag          0x0
S:lr_active        0x0          qsfp_txrx_rate_sel
0x0
S:
S:UPSM            UP00: UPST_PORT_DISABLED  --> UP00: UPST_PORT_DISABLED
S:SNSM(OV)        SN00: OV_SNST_STOPPED    --> SN00: OV_SNST_STOPPED
S:SNSM(SW)        SW00: SW_SNST_STAGE_WS  --> SW00: SW_SNST_STAGE_WS
S:PHYSM           PP00: PHYST_STOPPED      --> PP00: PHYST_STOPPED
S:LKSM(OV)        LK00: OV_LKST_INACTIVE   --> LK00: OV_LKST_INACTIVE
S:LKSM(SW)        SW13: INACTIVE      --> SW13: INACTIVE
S:TRKSM           TRK0: TRKST_INIT      --> TRK0: TRKST_INIT
S:
S:physm variables:
S:-----
-----
S:proto_phyp       0xb8806000      physm_hdl
0xb800f6e0
S:force_offline    0          copper          0
S:fault_reason     0: UNKNOWN
S:phy_media_present 0
S:
S:snsn variables:
S:-----
-----
S:speed            0xff          proto_phyp

```

```

0xb8806000
S:hw_sn_tries_left      0x0          sw_sn_tries_left      0x0
S:curr_txsp_count      0x0          curr_tx_indx
S:tx_max                0x0          curr_rxsp_count
      0x0
S:curr_tx               0x0          curr_rx_indx
      0x0
S:rx_max                0x0          rx_mem
      0x0
S:curr_rx               0x0
      0x0
S:rxsp_rec_count       0x0
S:nc_start              0x0          tx_start              0x0
S:sync_start           0x0          sync_present          0x0
S:diag_auto            0x0          diag_speed            0xff
S:striped_wd_tov       3000          hw_wd_tov
      3000
S:step                  0x0          qsfp28_speed_mode
      0x0
S:qsfp_mode0_hw_sn_tries_left  0x0
S:qsfp_mode1_hw_sn_tries_left  0x0
S:
S:lksm variables:
S:-----
-----
S:proto_phyph          0xb8806000    ov_lksm_hdl
0xb800f780
sw_lksm_hdl            0xb800f820
num_lf1                0
S:hw_link_tries_left  0          sw_link_tries_left    0
S:buf_ptype            0x0          stored_entry_state    0x6
S:handshake_owner      0x0          mark_unsent
      0x0
S:busybuf_stuck        0x0          lr_wait               0x0
S:
S:trksm variables:
S:-----
-----
S:Not a trunk port
S:
S:upsm variables:
S:-----
-----
S:proto_phyph          0xb8806000    upsm_hdl
0xb800f960
S:bb_credits           0          port_beacon           0
S:port_diag_flag       0          force_offline
      0
S:port_fault_rsn       0: PORT_NO_FAULT
S:retry_init_rsn       0: UNKNOWN
S:linit_reason         0          linit_result          0
S:ie_fctl_mode         0          fec_in_sync_tries_left 0
S:retry_sn_fail_init   0
retry_link_fail_init   0

```



```

S:excess_lr_count      0
S:
S:c4_ch_cfg
S:-----
-----
S:c4_desc_ring_size   256      292      256      256      292
292      2      292      292
S:thresh_def          0      16      1      0
S:intr_tries          500      cmem_pattern
0xdeadbeef
S:cmem_pattern_upwd   2      cmem_init_time      16
S:cmem_init_tries      5
S:ctrl_par_thresh     2      data_par_thresh
4
S:cam_par_thresh      4      buf_loss_thresh
12
S:crit_par_thresh     2      non_crit_par_thresh
6
S:pci_abort_thresh    10      pci_err_thresh      5
S:excess_chintr_thresh 8      sw_err_thresh      20
S:err_sample_period   300      intr_sleep
20000
S:frame_timeout       2500      proxy_dev      16384
S:vf_route            81920      qos      2048
S:stats 2048          f_redirect      2048
S:rsp_trap            2048      lun_zoning      20480
S:area_mode           0      ftb_max_loop[0]    0
S:ftb_max_loop[1]     6      ftb_max_loop[2]    9
S:ftb_max_loop[3]     10     ftb_max_loop[4]    10
S:ftb_max_loop[5]     5      ftb_max_loop[6]    6
S:ftb_seg_size[0]     0      ftb_seg_size[1]
16384
S:ftb_seg_size[2]     65536     ftb_seg_size[3]
16384
S:ftb_seg_size[4]     16384     ftb_seg_size[5]
65536
S:ftb_seg_size[6]     16384     ftb_seg_base[0]    0
S:ftb_seg_base[1]     0      ftb_seg_base[2]
65536
S:ftb_seg_base[3]     16384     ftb_seg_base[4]
32768
S:ftb_seg_base[5]     131072    ftb_seg_base[6]
49152
asic_err_monitor_period1 300
asic_err_monitor_period2 86400
zone_chk_to_poll_period 25
zone_chk_class2_reject_tov 220
S:
S:c4_phy_cfg
S:-----
-----
S:version = 2.1
S:pt                  0x43028002      fab_ptr
0x9a800000

```

```

S:fabattr                                0x9a8000d4      fab_iop
      0x9a800050
S:cfgbm                                  0xbb82d0e4      port_ctrl
0xb6ab5158
S:pcap.pcap_bm                            0x8d215547      pcap.pcap2_bm
0x2588289
S:pcap.pcap3_bm                            0x1bebe0c
ui_idx                                     57              S:slot_no
      0
is_icl                                     0              S:sw_usr_ports      400
S:neg_speed                               0 0 0 0 0 0
S:my_domain                               0x1             port_mode           0x0
S:hw_sn_maxtries                           100            sw_sn_maxtries
      0
S:hw_link_maxtries                         10            sw_link_maxtries   5
S:rx_cyc_tov                              28            rttov              300
S:bufrdy_tov                              300           busybuf_tov        286
S:mark_tov                                300           lksm_tov           3000
S:buf_dealloc_wait                         4             hw_wd_tov          3000
S:hw_lk_train_tov                          540           hw_lk_test_tov
      150
S:syswait_tx_12_lips                       1             lip_rx_tov         55
S:al_time_tov                              15           lp_tov             2000
S:intr_tries_port                          500           intr_mod_debounce
      250
S:intr_lsrflt_debounce                     500           intr_efifo_debounce 100
S:port_no_fid                              3             excess_ptintr_thresh 8
S:port_fault1_thresh                       100           port_fault1_spur_thresh 250
S:port_fault1_disc_thresh                   500
port_fault1_disc_spur_thresh               1000
S:port_fault2_thresh                        5             losync_tov         100
S:port_sw_link_to                          15           en_8g_scramble
      1
frc_hw_sn_mode                             0x1
S:enc_poll_thresh                          0             fec_enable
      0
S:fec_in_sync_to                           50           fec_in_sync_try_max
      4
S:port_be_lto_threshold                     100           port_be_lr_threshold
      2
S:be_cr_in_sync_to                         5
port_credit_overnrun_thresh                10
S:jda_sfp_losig_tov                       400
jda_sfp_losig_try_max                      30
S:striped_wd_tov                           3000
no_sync_debounce                           1200
S:
S:      fab_iop
S:=====
S:fab_iop->interop_mode 0x0                fab_iop->lab_mode   0x0
S:fab_iop->fl_bbc          0x0                fab_iop->fl_fan
      0x0
S:fab_iop->fl_cls          0x4                fab_iop->fl_rscn
      0x0

```

```

S:fab_iop->domain_id_offset      0x60          fab_iop-
>mcmt_fabric_mode      0x0
S:fab_iop->mcmt_default_zone      0x0          fab_iop-
>mcmt_safe_zone      0x0
S:
S:      port_ctrl
S:=====
S:port_ctrl.port_type      1          port_ctrl.port_grp      0
S:port_ctrl.port_number 57          port_ctrl.vc_mode      1
S:
S:      port_ctrl.lcap
S:=====
S:has_serdes      0          has_media      1
S:topology      1          skip_nego      0
S:skip_pnego      0          skip_init_event      0
S:en_shim      0          speed_neg
      1
S:loop_back      0          num_speeds      5
S:fec_enable      0
S:
S:      port_ctrl.speed_list array
S:=====
S:speed_list[0].auto_neg 1          speed_list[0].lnk_speed 0x0000000a
S:speed_list[1].auto_neg 1          speed_list[1].lnk_speed 0x00000008
S:speed_list[2].auto_neg 1          speed_list[2].lnk_speed 0x00000006
S:speed_list[3].auto_neg 1          speed_list[3].lnk_speed 0x00000005
S:speed_list[4].auto_neg 1          speed_list[4].lnk_speed 0x00000003
S:speed_list[5].auto_neg 0          speed_list[5].lnk_speed 0x00000000
S:
S:      port_ctrl.cm
S:=====
S:port_ctrl.cm.num_vcs      8
S:port_ctrl.cm.min_bufs      8
S:port_ctrl.cm.cr_shar_bufs 0
S:port_ctrl.vc_alloc
S:port_ctrl.vc_alloc      2 0 1 1 1 1 1 1
S:port_ctrl.vc_alloc      0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.norm_vc_alloc
S:port_ctrl.norm_vc_alloc      4 0 5 5 5 5 1 1
S:port_ctrl.norm_vc_alloc      0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.cm.skip_bb_credit      0
S:port_ctrl.cm.use_shim_based_sublist      0
S:
S:      port_ctrl.serdes_set
S:=====
S:serdes_type      0x8
S:serdes_data_t.ibm_hss_serdes.tx_drive_power      0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b_sign      0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b      0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_a      0x0
S:serdes_data_t.ibm_hss_serdes.rxeq      0x0
S:

```

```

S:      cfgbm
S:=====
S:old_distance      0x0          gport_lockdown      0x0
S:tpport            0x1          speed                0x0
S:disable_eport     0x0          fcacc                0x0
S:lport_lockdown    0x0          0x0                  priv_lport_lockdown
                        0x0
S:vcxlt_linit       0x0          delay_flogi          0x0
S:isl_interop       0x0          distance              0x0
S:BufStarvFlag      0x0          credit_sharing        0x0
S:lport_halfduplex  0x0          lport_fairness        0x0
S:soft_neg          0x0          asn_frc_hwretry      0x0
S:cr_recov          0x0          fport_buffers         0x0
S:export            0x0          0x0                  export_mode
                        0x0
S:csctl_en          0x0          mirror_port          0x0
S:fault_delay       0x0          non_dfe              0x0
S:fec_configured*(0=ENAB) 0          0                    fec_tts
                        0
S:port_persistently_disabled (permanently) 0 (0)
S:
S:      cfg property
S:=====
S:priv_pcfg_bm      0x00000000      lgcl_pcfg_bm
0xbb82d124
S:fport_buffer      0x00000000
S:
S:
S:C4 Discard Cntrs: rxlp_stats = 0xb6ab44b0
S:-----
-----
S:disc_mcast_wka    0x0          disc_inv_did          0x0
S:disc_cl1_cl4      0x0          disc_sid_chk_fail    0x0
S:disc_inv_dom_egid_txpt 0x0          disc_vft_hop_cnt_1
                        0x0
S:disc_classf       0x0          disc_fcp_cdb_inv      0x0
S:disc_vfid_trap_enabled 0x0          0x0
disc_vfid_hdr_chk_fail 0x0
S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err 0x0
S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err 0x0
S:disc_ftb_vm_mode  0x0          disc_ftb_agnt2_miss   0x0
S:disc_ecb_de_pad_err 0x0          disc_ecb_de_tag_err   0x0
S:disc_ecb_de_seq_err 0x0          disc_ecb_err           0x0
S:disc_ftb_type4_match 0x0          disc_fcp_rsp_ftb_type4 0x0
S:disc_fcp_rsp_ftb_type4 0x0          disc_ftb_type5_match
                        0x0
S:disc_ftb_type3_match 0x0          disc_els_ftb_type3    0x0
S:disc_ftb_type1_match 0x0          disc_els_rsp_ex_port  0x0
S:disc_inv_drp_dps  0x0          disc_did_lookup_miss  0x0
S:disc_ftb_type2_match 0x0          disc_trpd_plogi_pdisc 0x0
S:disc_type2_lookup_miss 0x0          disc_ftb_type6_match
                        0x0
S:disc_els_rep_ex_port 0x0          disc_els_sid_lkup_bit1 0x0
S:disc_els_sid_lkup_bit0 0x0          0x0

```

```

disc_bls_frm_trap_bit1 0x0
S:disc_ftb_token_err 0x0
S:disc_hard_zone_miss 0x0
S:discflt_frame_disc 0x0
S:disc_frame_marked_du 0x0
E:Connection type: FE
E:Port type: E_port
E:Trunk port: No
E:Configured Speed: AUTO_SPEED_NEGO
E:Max Capable Speed: 32G
E:Current SNSM Speed: UNDEFINED
E:Hardware TX Speed: 32G (0x00000004)
E:Hardware RX Speed: 32G (0x00000040)
E:
E:Interrupts: 0 Link_failure: 0
Loss_of_sync: 0 Loss_of_sig: 0
E:Lli: 0 Invalid_word: 0
E:trapped_frm: 0 fwd_status_ok: 0
E:fwd_timeout: 0 fwd_tx_unavail: 0
E:fwd_unroutable: 0 fwd_zone_out: 0
E:fwd_other_err: 0 frm_err_discard: 0
E:Fltr listA: 0 Fltr listB: 0
E:Zone trap fwd: 0 Zone trap disc: 0
E:shim_csum: 0 RTE_perr: 0
E:Invalid_crc: 0 Delim_err: 0
E:Protocol_err: 0
E:Lr_in: 0 Lr_out: 0
E:Ols_in: 0 Ols_out: 0

```

filterportshow 57

FILTER DATA

```

-----
Shadow settings:
Filter Enable: 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000

```

Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass: 0x00000000

Real settings:

Enable RAM: 0x00000000, 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass RAM: 0x00000000

Shadowed filters:

Filter 0: Not Installed (MIRROR1)(LISTA)

```
    c4_fldenable[0] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[0] = 0x00000000,c4_fltr_config[0] = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
    c4_fldenable[1] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[1] = 0x00000000,c4_fltr_config[1] = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
    c4_fldenable[2] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[2] = 0x00000000,c4_fltr_config[2] = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
    c4_fldenable[3] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[3] = 0x00000000,c4_fltr_config[3] = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
    c4_fldenable[4] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[4] = 0x00000000,c4_fltr_config[4] = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
    c4_fldenable[5] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[5] = 0x00000000,c4_fltr_config[5] = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
    c4_fldenable[6] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[6] = 0x00000000,c4_fltr_config[6] = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
    c4_fldenable[7] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[7] = 0x00000000,c4_fltr_config[7] = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
    c4_fldenable[8] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[8] = 0x00000000,c4_fltr_config[8] = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
    c4_fldenable[9] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[9] = 0x00000000,c4_fltr_config[9] = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
    c4_fldenable[10] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[10] = 0x00000000,c4_fltr_config[10] =
0x00000000
Filter 11: Not Installed (SIM)(LISTA)
    c4_fldenable[11] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[11] = 0x00000000,c4_fltr_config[11] =
0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
    c4_fldenable[12] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[12] = 0x00000000,c4_fltr_config[12] =
0x00000000
```

Filter 13: Not Installed (UNUSED)(LISTA)
c4_fldenable[13] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[13] = 0x00000000,c4_fltr_config[13] =
0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
c4_fldenable[14] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[14] = 0x00000000,c4_fltr_config[14] =
0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
c4_fldenable[15] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[15] = 0x00000000,c4_fltr_config[15] =
0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
c4_fldenable[16] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[16] = 0x00000000,c4_fltr_config[16] =
0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
c4_fldenable[17] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[17] = 0x00000000,c4_fltr_config[17] =
0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
c4_fldenable[18] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[18] = 0x00000000,c4_fltr_config[18] =
0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
c4_fldenable[19] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[19] = 0x00000000,c4_fltr_config[19] =
0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
c4_fldenable[20] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[20] = 0x00000000,c4_fltr_config[20] =
0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
c4_fldenable[21] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[21] = 0x00000000,c4_fltr_config[21] =
0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
c4_fldenable[22] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[22] = 0x00000000,c4_fltr_config[22] =
0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
c4_fldenable[23] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[23] = 0x00000000,c4_fltr_config[23] =


```
0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
    c4_fldenable[24] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[24] = 0x00000000,c4_fltr_config[24] =
0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
    c4_fldenable[25] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[25] = 0x00000000,c4_fltr_config[25] =
0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
    c4_fldenable[26] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[26] = 0x00000000,c4_fltr_config[26] =
0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
    c4_fldenable[27] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[27] = 0x00000000,c4_fltr_config[27] =
0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
    c4_fldenable[28] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[28] = 0x00000000,c4_fltr_config[28] =
0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
    c4_fldenable[29] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[29] = 0x00000000,c4_fltr_config[29] =
0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    c4_fldenable[30] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[30] = 0x00000000,c4_fltr_config[30] =
0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    c4_fldenable[31] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[31] = 0x00000000,c4_fltr_config[31] =
0x00000000
```

Real filters:

```
Filter 0: Not Installed (MIRROR1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
```

```
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 11: Not Installed (SIM)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
```

fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 29: Not Installed (OPM2)(LISTA)

```
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter dirty indicator: 0x00000000
Performance filters: 0
Port Mirror filters: 0 (0x0)
```

FIELD DATA

Shadowed fields:

```
fldoffset[0] = 0x00, fldmask[0] = 0x00, fldvalue_dyna[0]: 0x00 0x00
0x00 0x00
fldcontrol[0].inuse = 0x0  fldcontrol[0].refcnt = 0x00 0x00 0x00
0x00
fldoffset[1] = 0x00, fldmask[1] = 0x00, fldvalue_dyna[1]: 0x00 0x00
0x00 0x00
fldcontrol[1].inuse = 0x0  fldcontrol[1].refcnt = 0x00 0x00 0x00
0x00
fldoffset[2] = 0x00, fldmask[2] = 0x00, fldvalue_dyna[2]: 0x00 0x00
0x00 0x00
fldcontrol[2].inuse = 0x0  fldcontrol[2].refcnt = 0x00 0x00 0x00
0x00
fldoffset[3] = 0x00, fldmask[3] = 0x00, fldvalue_dyna[3]: 0x00 0x00
0x00 0x00
fldcontrol[3].inuse = 0x0  fldcontrol[3].refcnt = 0x00 0x00 0x00
0x00
fldoffset[4] = 0x00, fldmask[4] = 0x00, fldvalue_dyna[4]: 0x00 0x00
0x00 0x00
fldcontrol[4].inuse = 0x0  fldcontrol[4].refcnt = 0x00 0x00 0x00
0x00
fldoffset[5] = 0x00, fldmask[5] = 0x00, fldvalue_dyna[5]: 0x00 0x00
0x00 0x00
fldcontrol[5].inuse = 0x0  fldcontrol[5].refcnt = 0x00 0x00 0x00
0x00
fldoffset[6] = 0x00, fldmask[6] = 0x00, fldvalue_dyna[6]: 0x00 0x00
0x00 0x00
fldcontrol[6].inuse = 0x0  fldcontrol[6].refcnt = 0x00 0x00 0x00
0x00
fldoffset[7] = 0x00, fldmask[7] = 0x00, fldvalue_dyna[7]: 0x00 0x00
0x00 0x00
fldcontrol[7].inuse = 0x0  fldcontrol[7].refcnt = 0x00 0x00 0x00
0x00
```

```
fldoffset[8] = 0x00, fldmask[8] = 0x00, fldvalue_dyna[8]:0x00 0x00
0x00 0x00
fldcontrol[8].inuse = 0x0 fldcontrol[8].refcnt = 0x00 0x00 0x00
0x00
fldoffset[9] = 0x00, fldmask[9] = 0x00, fldvalue_dyna[9]:0x00 0x00
0x00 0x00
fldcontrol[9].inuse = 0x0 fldcontrol[9].refcnt = 0x00 0x00 0x00
0x00
fldoffset[10] = 0x00, fldmask[10] = 0x00, fldvalue_dyna[10]:0x00 0x00
0x00 0x00
fldcontrol[10].inuse = 0x0 fldcontrol[10].refcnt = 0x00 0x00 0x00
0x00
fldoffset[11] = 0x00, fldmask[11] = 0x00, fldvalue_dyna[11]:0x00 0x00
0x00 0x00
fldcontrol[11].inuse = 0x0 fldcontrol[11].refcnt = 0x00 0x00 0x00
0x00
fldoffset[12] = 0x00, fldmask[12] = 0x00, fldvalue_dyna[12]:0x00 0x00
0x00 0x00
fldcontrol[12].inuse = 0x0 fldcontrol[12].refcnt = 0x00 0x00 0x00
0x00
fldoffset[13] = 0x00, fldmask[13] = 0x00, fldvalue_dyna[13]:0x00 0x00
0x00 0x00
fldcontrol[13].inuse = 0x0 fldcontrol[13].refcnt = 0x00 0x00 0x00
0x00
fldoffset[14] = 0x00, fldmask[14] = 0x00, fldvalue_dyna[14]:0x00 0x00
0x00 0x00
fldcontrol[14].inuse = 0x0 fldcontrol[14].refcnt = 0x00 0x00 0x00
0x00
fldoffset[15] = 0x00, fldmask[15] = 0x00, fldvalue_dyna[15]:0x00 0x00
0x00 0x00
fldcontrol[15].inuse = 0x0 fldcontrol[15].refcnt = 0x00 0x00 0x00
0x00
fldoffset[16] = 0x00, fldmask[16] = 0x00, fldvalue_dyna[16]:0x00 0x00
0x00 0x00
fldcontrol[16].inuse = 0x0 fldcontrol[16].refcnt = 0x00 0x00 0x00
0x00
fldoffset[17] = 0x00, fldmask[17] = 0x00, fldvalue_dyna[17]:0x00 0x00
0x00 0x00
fldcontrol[17].inuse = 0x0 fldcontrol[17].refcnt = 0x00 0x00 0x00
0x00
fldoffset[18] = 0x00, fldmask[18] = 0x00, fldvalue_dyna[18]:0x00 0x00
0x00 0x00
fldcontrol[18].inuse = 0x0 fldcontrol[18].refcnt = 0x00 0x00 0x00
0x00
fldoffset[19] = 0x00, fldmask[19] = 0x00, fldvalue_dyna[19]:0x00 0x00
0x00 0x00
fldcontrol[19].inuse = 0x0 fldcontrol[19].refcnt = 0x00 0x00 0x00
0x00
```

Real fields:

```
fldoffset RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000
```

```
fldmask RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
```

0x00000000
fld value4 RAM:
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000

Field dirty indicator: 0x00000000

FDB reference count fdb: 0 [0 0 0 0]
FDB reference count fdb: 1 [0 0 0 0]
FDB reference count fdb: 2 [0 0 0 0]
FDB reference count fdb: 3 [0 0 0 0]
FDB reference count fdb: 4 [0 0 0 0]
FDB reference count fdb: 5 [0 0 0 0]
FDB reference count fdb: 6 [0 0 0 0]
FDB reference count fdb: 7 [0 0 0 0]
FDB reference count fdb: 8 [0 0 0 0]
FDB reference count fdb: 9 [0 0 0 0]
FDB reference count fdb: 10 [0 0 0 0]
FDB reference count fdb: 11 [0 0 0 0]
FDB reference count fdb: 12 [0 0 0 0]
FDB reference count fdb: 13 [0 0 0 0]
FDB reference count fdb: 14 [0 0 0 0]
FDB reference count fdb: 15 [0 0 0 0]
FDB reference count fdb: 16 [0 0 0 0]
FDB reference count fdb: 17 [0 0 0 0]
FDB reference count fdb: 18 [0 0 0 0]
FDB reference count fdb: 19 [0 0 0 0]

Filter counters:

Filter counter 0: 0 (MIRROR1)
Filter counter 1: 0 (MIRROR2)
Filter counter 2: 0 (MIRROR3)
Filter counter 3: 0 (MIRROR4)
Filter counter 4: 0 (AEPORT_NON_MIRR_DROP)
Filter counter 5: 0 (ZONING TRAP)
Filter counter 6: 0 (FCR_EXPORT_DC)
Filter counter 7: 0 (TIN TRAP)

Filter counter 8: 0 (FICON CUP)
Filter counter 9: 0 (FICON CUP DST)
Filter counter 10: 0 (WELL KNOWN ADDR)
Filter counter 11: 0 (SIM)
Filter counter 12: 0 (UNUSED)
Filter counter 13: 0 (UNUSED)
Filter counter 14: 0 (UNUSED)
Filter counter 15: 0 (UNUSED)
Filter counter 16: 0 (PERF1)
Filter counter 17: 0 (PERF2)
Filter counter 18: 0 (PERF3)
Filter counter 19: 0 (PERF4)
Filter counter 20: 0 (PERF5)
Filter counter 21: 0 (PERF6)
Filter counter 22: 0 (PERF7)
Filter counter 23: 0 (PERF8)
Filter counter 24: 0 (PERF9)
Filter counter 25: 0 (PERF10)
Filter counter 26: 0 (PERF11)
Filter counter 27: 0 (PERF12)
Filter counter 28: 0 (OPM1)
Filter counter 29: 0 (OPM2)
Filter counter 30: 0 (IPM1)
Filter counter 31: 0 (IPM2)

ACL DATA

Logical port 2: Hard Zoning disabled, Soft Zoning disabled
Zone type: WWN Zoning
Frames with hard zone miss: 0

*** Please use filterportshow on user port 56 to display ACL hash tables and Mirroring resources of thischip.
***We show this data only for the first physical port which is an external port.

portFcPortCmdShow --slot 0 58 3
doing portFcPortCmdShow: arg1 = 3, arg2 = -2

portshow 58
portDisableReason: None
portCFlags: 0x0
portFlags: 0x4021 PRESENT U_PORT DISABLED LED
LocalSwcFlags: 0x0
portType: 26.0
POD Port: Need license to enable the port
portState: 2 Offline
Protocol: FC
portPhys: 2 No_Module portScn: 2 Offline
port generation number: 0
state transition count: 0

portId: 013a00
portIfId: 43020003

portWwn: 20:3a:d8:1f:cc:2c:99:90
portWwn of device(s) connected:
16b Area list:
Distance: normal
portSpeed: N32Gbps

FEC: Inactive
Credit Recovery: Inactive
LE domain: 0
Peer beacon: Off
FC Fastwrite: OFF

| | | | | |
|-------------|---|---------------|---|-------|
| Interrupts: | 0 | Link_failure: | 0 | Frjt: |
| 0 | | | | |
| Unknown: | 0 | Loss_of_sync: | 0 | Fbsy: |
| 0 | | | | |
| Lli: | 0 | Loss_of_sig: | 0 | |
| Proc_rqrd: | 0 | Protocol_err: | 0 | |
| Timed_out: | 0 | Invalid_word: | 0 | |
| Tx_unavail: | 0 | Invalid_crc: | 0 | |
| Delim_err: | 0 | Address_err: | 0 | |
| Lr_in: | 0 | Ols_in: | 0 | |
| Lr_out: | 0 | Ols_out: | 0 | |

portloginshow 58

| Type | PID | World Wide Name | credit | df_sz | cos |
|-------|-----|-----------------|--------|-------|-----|
| ===== | | | | | |

portloginshow 58 -history

| Type | PID | World Wide Name | logout time |
|-------|-----|-----------------|-------------|
| ===== | | | |

portregshow 58

LED registers

=====

| | | | |
|-------------|---------------|----------|-------------|
| 0x81c1a000: | c4_led_status | 00000000 | 0x81c1a004: |
| | c4_led_ctl | 00000000 | |

FPL registers

=====

| | | | |
|-------------|-----------------------|----------|-------------|
| 0x81c18200: | fpl_port_config | 23490000 | |
| 0x81c1820c: | fpl_port_id_ctl | 00000000 | 0x81c18210: |
| | fpl_port_id_addr | 00013a00 | |
| 0x81c18214: | fpl_port_speed | 00000004 | 0x81c1821c: |
| | fpl_lli_ctl | 00000903 | |
| 0x81c18228: | fpl_lli_os_ctl | bc95b5b5 | 0x81c1822c: |
| | fpl_lli_send_word | bc95b5b5 | |
| 0x81c18230: | fpl_lli_mark_rx | 00000000 | 0x81c18234: |
| | fpl_lli_rnd_trip_time | 00000000 | |
| 0x81c18238: | fpl_lli_ns_status | 00070007 | 0x81c1823c: |
| | fpl_lli_intr_status | 80070007 | |

| | | |
|---------------------------------|----------|-------------|
| 0x81c18244: fpl_lli_def | 00000000 | 0x81c18254: |
| fpl_lli_intr_enable_clr | 00100000 | |
| 0x81c18258: fpl_err_intr_status | 00000000 | 0x81c18260: |
| fpl_err_intr_enable_clr | 00000000 | |
| 0x81c18268: fpl_err_first_error | 00000000 | 0x81c1826c: |
| fpl_speed_neg_ctl | 00000000 | |
| 0x81c18270: fpl_speed_neg_stat | 00000000 | 0x81c18274: |
| fpl_softasn_ctl | 0000000f | |
| 0x81c18278: fpl_link_init_ctl | 00000000 | 0x81c1827c: |
| fpl_link_init_stat | 00000000 | |
| 0x81c18280: fpl_aec_ctl | 00051060 | 0x81c18284: |
| fpl_aec_ctl2 | 04009f60 | |
| 0x81c18288: fpl_pcs_ctl | 00000160 | 0x81c1828c: |
| fpl_fec_ctl | 00000441 | |
| 0x81c18290: fpl_fec_cor | 00000000 | 0x81c18294: |
| fpl_fec_uncor | 00000000 | |
| 0x81c18298: fpl_hss_link_ctl | 0031f040 | 0x81c1829c: |
| fpl_afifo_link_ctl | 00000a86 | |
| 0x81c182a0: fpl_echo_lb_ctl | 0000028c | 0x81c182a4: |
| fpl_scratch | 00000121 | |
| 0x81c182a8: fpl_debug | 00030005 | 0x81c182ac: |
| fpl_misc_debug | 00001800 | |
| 0x00000000: SW_shadow_reg | 00000000 | 0x00000000: |
| SW_c4_phyp->cfgptr | 00030000 | |

per-fpg (per octet) registers

=====

| | | |
|-------------------------------------|----------|-------------|
| 0x8180382c: fpg_serdes_ctla0 | 81a37be7 | 0x81803830: |
| fpg_serdes_ctla1 | 81a37be7 | |
| 0x81803834: fpg_serdes_ctlb0 | 81a1c3c3 | 0x81803838: |
| fpg_serdes_ctlb1 | 81a1c3c3 | |
| 0x8180383c: fpg_serdes_xgmii_1ms | 00067c28 | 0x81803840: |
| fpg_serdes_regtimctl | 40e47946 | |
| 0x81803844: fpg_serdes_asnrsttimctl | 00000102 | |

HSS PLL registers

=====

| | | |
|--|----------|-------------|
| 0x81801400: 00_hssplla_vco_coarse_cal0 | 00000000 | 0x81801404: |
| 01_hssplla_vco_coarse_cal1 | 00000014 | |
| 0x81801408: 02_hssplla_vco_coarse_cal2 | 00000000 | 0x8180140c: |
| 03_hssplla_vco_coarse_cal3 | 00000000 | |
| 0x81801410: 04_hssplla_vco_coarse_cal4 | 00000000 | 0x81801424: |
| 09_hssplla_power_ctl | 00000000 | |
| 0x81801428: 0A_hssplla_charge_pump_ctl | 00000004 | 0x81801438: |
| 0E_hssplla_pll_misc_ctl | 00000000 | |
| 0x8180143c: 0F_hssplla_pclk_ctl | 000000f8 | 0x81801440: |
| 10_hssplla_eyem_intv_ctl | 00000000 | |
| 0x81801444: 11_hssplla_eyem_intv_lim1 | 00000000 | 0x81801448: |
| 12_hssplla_eyem_intv_lim2 | 00000000 | |
| 0x8180144c: 13_hssplla_eyem_intv_lim3 | 00000000 | 0x81801450: |
| 14_hssplla_eyem_intv_lim4 | 00000000 | |
| 0x818014f0: 3C_hssplla_macro_tst_ctl4 | 00000000 | 0x818014f4: |
| 3D_hssplla_macro_tst_ctl3 | 00000000 | |
| 0x818014f8: 3E_hssplla_macro_tst_ctl2 | 00000000 | 0x818014fc: |

| | | | |
|--|----------|----------|-------------|
| 3F_hssplla_macro_tst_ctl1 | 00000000 | | |
| 0x81801500: 00_hsspllb_vco_coarse_cal0 | | 0000000a | 0x81801504: |
| 01_hsspllb_vco_coarse_cal1 | 00000014 | | |
| 0x81801508: 02_hsspllb_vco_coarse_cal2 | | 00000000 | 0x8180150c: |
| 03_hsspllb_vco_coarse_cal3 | 00000000 | | |
| 0x81801510: 04_hsspllb_vco_coarse_cal4 | | 00000000 | 0x81801524: |
| 09_hsspllb_power_ctl | 00000000 | | |
| 0x81801528: 0A_hsspllb_charge_pump_ctl | | 00000004 | 0x81801538: |
| 0E_hsspllb_pll_misc_ctl | 00000000 | | |
| 0x8180153c: 0F_hsspllb_pclk_ctl | | 000000f8 | 0x81801540: |
| 10_hsspllb_eyem_intv_ctl | 00000000 | | |
| 0x81801544: 11_hsspllb_eyem_intv_lim1 | | 00000000 | 0x81801548: |
| 12_hsspllb_eyem_intv_lim2 | 00000000 | | |
| 0x8180154c: 13_hsspllb_eyem_intv_lim3 | | 00000000 | 0x81801550: |
| 14_hsspllb_eyem_intv_lim4 | 00000000 | | |
| 0x818015f0: 3C_hsspllb_macro_tst_ctl4 | | 00000000 | 0x818015f4: |
| 3D_hsspllb_macro_tst_ctl3 | 00000000 | | |
| 0x818015f8: 3E_hsspllb_macro_tst_ctl2 | | 00000000 | 0x818015fc: |
| 3F_hsspllb_macro_tst_ctl1 | 00000000 | | |

HSS TX registers

=====

| | | | |
|--|----------|----------|-------------|
| 0x81800500: 00_hsstx_cfg_mode_PHY | | 00009f48 | 0x81800504: |
| 01_hsstx_test_ctl | 00000000 | | |
| 0x81800508: 02_hsstx_coeff_ctl_INV | | 00000000 | 0x8180050c: |
| 03_hsstx_drv_mode_ctl | 00000000 | | |
| 0x81800510: 04_hsstx_drv_ovrd_ctl | | 00000010 | 0x81800514: |
| 05_hsstx_dclk_align_ovrd | 00000080 | | |
| 0x81800518: 06_hsstx_imp_cal_ovrd | | 00000c0c | 0x8180051c: |
| 07_hsstx_dclk_drift_tol | 00000004 | | |
| 0x81800520: 08_hsstx_tap0_coeff_TUNE | | 00000000 | 0x81800524: |
| 09_hsstx_tap1_coeff_TUNE | 00000003 | | |
| 0x81800528: 0A_hsstx_tap2_coeff_TUNE | | 00000018 | 0x8180052c: |
| 0B_hsstx_tap3_coeff_TUNE | 0000000d | | |
| 0x81800534: 0D_hsstx_pol_INV | | 00000004 | 0x81800538: |
| 0E_hsstx_ae_cmd | 00000000 | | |
| 0x8180053c: 0F_hsstx_ae_stat | | 00000000 | 0x81800540: |
| 10_hsstx_ae_tap0_TUNE | 00000000 | | |
| 0x81800544: 11_hsstx_ae_tap1_TUNE | | 00000000 | 0x81800548: |
| 12_hsstx_ae_tap2_TUNE | 00000028 | | |
| 0x8180054c: 13_hsstx_ae_tap3_TUNE | | 00000000 | 0x81800554: |
| 15_hsstx_app_tune | 0000120e | | |
| 0x81800558: 16_hsstx_analog_diag | | 00000000 | 0x81800560: |
| 18_hsstx_4x_seg_app | 0000aafa | | |
| 0x81800564: 19_hsstx_2x_seg_app | | 00000000 | 0x81800568: |
| 1A_hsstx_1x_seg_app | 0000ff5d | | |
| 0x8180056c: 1B_hsstx_seg_4x_term_app | | 00000000 | 0x81800570: |
| 1C_hsstx_seg_2x1x_term_app | 00000f00 | | |
| 0x81800574: 1D_hsstx_tap_sign_app | | 00000004 | 0x81800578: |
| 1E_hsstx_ext_addr_data | 00000001 | | |
| 0x8180057c: 1F_hsstx_ext_addr_addr | | 00000000 | 0x81800580: |
| 20_hsstx_pat_buf_bytes_1_0 | 00000000 | | |
| 0x81800584: 21_hsstx_pat_buf_bytes_3_2 | | 00000000 | 0x81800588: |
| 22_hsstx_pat_buf_bytes_5_4 | 00000000 | | |

| | | |
|---|----------|-------------|
| 0x8180058c: 23_hsstx_pat_buf_bytes_7_6 | 00000000 | 0x8180059c: |
| 27_hsstx_8023az_ctl | 00000000 | |
| 0x818005a0: 28_hsstx_dcc_ctl | 000060c0 | 0x818005a4: |
| 29_hsstx_dcc_ovrd | 00000000 | |
| 0x818005a8: 2A_hsstx_dcc_app | 00000000 | 0x818005ac: |
| 2B_hsstx_dcc_timeout | 0000ffff | |
| 0x818005c0: 30_hsstx_tap_sign_ovrd | 00000000 | 0x818005c8: |
| 32_hsstx_seg_4x_ovrd | 00000000 | |
| 0x818005cc: 33_hsstx_seg_2x_ovrd | 00000000 | 0x818005d0: |
| 34_hsstx_seg_1x_ovrd | 00000000 | |
| 0x818005d8: 36_hsstx_tap_seg_4x_term_ovrd | 00000000 | 0x818005dc: |
| 37_hsstx_tap_seg_2x_term_ovrd | 00000000 | |
| 0x818005e0: 38_hsstx_tap_seg_1x_term_ovrd | 00000000 | 0x818005ec: |
| 3B_hsstx_mac_test_ctl5 | 00000000 | |
| 0x818005f0: 3C_hsstx_mac_test_ctl4 | 00000000 | 0x818005f4: |
| 3D_hsstx_mac_test_ctl3 | 00000000 | |
| 0x818005f8: 3E_hsstx_mac_test_ctl2 | 00000000 | 0x818005fc: |
| 3F_hsstx_mac_test_ctl1 | 000000c6 | |

HSS RX registers

=====

| | | |
|---|----------|-------------|
| 0x81800700: 00_hssrx_cfg_mode_PHY | 00009e78 | 0x81800704: |
| 01_hssrx_test_ctl | 00000000 | |
| 0x81800708: 02_hssrx_phs_rot_ctl | 0000cb80 | 0x8180070c: |
| 03_hssrx_phs_rot_ofs_ctl | 00001610 | |
| 0x81800710: 04_hssrx_phs_rot_posn1 | 00000202 | 0x81800714: |
| 05_hssrx_phs_rot_posn2 | 00000031 | |
| 0x81800718: 06_hssrx_phs_rot_sta_ofs1 | 00000000 | 0x8180071c: |
| 07_hssrx_phs_rot_sta_ofs2 | 00000000 | |
| 0x81800720: 08_hssrx_dfe_ctl_PHY | 00002002 | 0x81800724: |
| 09_hssrx_dfe_smpl_snap1 | 00000000 | |
| 0x81800728: 0A_hssrx_dfe_smpl_snap2 | 00008000 | 0x8180072c: |
| 0B_hssrx_vga_ctl1 | 00004001 | |
| 0x81800730: 0C_hssrx_vga_ctl2 | 00007aa0 | 0x81800734: |
| 0D_hssrx_vga_ctl3 | 000009e4 | |
| 0x81800738: 0E_hssrx_pwr_mgmt_ctl | 0000001f | 0x8180073c: |
| 0F_hssrx_iqamp_ctl1 | 0000001a | |
| 0x81800740: 10_hssrx_iqamp_ctl2 | 00000006 | 0x81800744: |
| 11_hssrx_dacap_dacan_sel | 00000003 | |
| 0x81800748: 12_hssrx_dacap_dacan | 0000ffff | 0x8180074c: |
| 13_hssrx_daca_min | 00000000 | |
| 0x81800750: 14_hssrx_adac_ctl | 00000000 | 0x81800754: |
| 15_hssrx_ac_cp_ctl | 000031c3 | |
| 0x81800758: 16_hssrx_ac_cp_val | 00008052 | 0x8180075c: |
| 17_hssrx_dfe_h1h2h3_lcl_off_ch | 00000014 | |
| 0x81800760: 18_hssrx_dfe_h1h2h3_lcl_off_val | 00000000 | 0x81800764: |
| 19_hssrx_peaked_intg | 000000ff | |
| 0x81800768: 1A_hssrx_cdr_analog_sw | 0000ce00 | 0x8180076c: |
| 1B_hssrx_peaking_amp_init_c_PHY | 00000000 | |
| 0x81800770: 1C_hssrx_dac_dpc | 00000040 | 0x81800774: |
| 1D_hssrx_ddc | 00000000 | |
| 0x81800778: 1E_hssrx_int_stat_PHY | 00001c0f | 0x8180077c: |
| 1F_hssrx_dfe_func_ctl1_PHY | 0000ffff | |
| 0x81800780: 20_hssrx_dfe_func_ctl2_INV | 00007eff | 0x81800784: |

| | | | |
|--|----------|-----------|-------------|
| 21_hssrx_ofs_ch_dcc_qcc_idx | 00002000 | | |
| 0x81800788: 22_hssrx_dfe_ofs_val | | 00000c7b | 0x8180078c: |
| 23_hssrx_h_coeff_bist | 00000401 | | |
| 0x81800790: 24_hssrx_ac_cap_bist | | 00002009 | 0x81800794: |
| 25_hssrx_max_gain_path_idx_res | 00007800 | | |
| 0x81800798: 26_hssrx_loff_ctl | | 00000040 | 0x8180079c: |
| 27_hssrx_sigdet_ctl | 00003780 | | |
| 0x818007a0: 28_hssrx_ana_ctl_sw | | 00000000 | 0x818007a4: |
| 29_hssrx_intg_dac_ofs | 0000dfe0 | | |
| 0x818007a8: 2A_hssrx_eye_ctl | | 00000000 | 0x818007ac: |
| 2B_hssrx_eye_met | 00000004 | | |
| 0x818007b0: 2C_hssrx_eye_met_err_cnt | | 00000000 | 0x818007b4: |
| 2D_hssrx_eye_met_pdf_eyec | 00000000 | | |
| 0x818007b8: 2E_hssrx_eye_met_pat_len | | 0000007f | 0x818007bc: |
| 2F_hssrx_dfe_func_ctl3 | 0000dfff | | |
| 0x818007c0: 30_hssrx_dfe_tap_ctl_idx_ptr | | 00000008 | 0x818007c4: |
| 31_hssrx_dfe_tap | 00003030 | | |
| 0x818007c8: 32_hssrx_lte_ctl_TUNE | | 00001601 | 0x818007e4: |
| 39_hssrx_int_stat2 | 0000c1ff | | |
| 0x818007e8: 3A_hssrx_ac_cpl_cur_src_adj | | 00000041 | 0x818007ec: |
| 3B_hssrx_dcd_ctl | 00007c42 | | |
| 0x818007f0: 3C_hssrx_dcc_ctl | | 00000d83 | 0x818007f4: |
| 3D_hssrx_qcc_ctl | 00006949 | | |
| 0x818007f8: 3E_hssrx_mac_test_ctl2 | | 00000000 | 0x818007fc: |
| 3F_hssrx_mac_test_ctl1 | 00000000 | | |
| 0x81800748: 12_hssrx_dacap_dacan[02] | | 00ff ffff | |
| 0x81800760: 18_hssrx_dfe_h1h2h3_lcl_off_va[00] | | 0000 0000 | 0000 |
| 0000 0000 0000 0000 0000 | | | |
| 0x81800760: 18_hssrx_dfe_h1h2h3_lcl_off_va[08] | | 0000 0000 | 0000 |
| 0000 0000 0000 0000 0000 | | | |
| 0x81800760: 18_hssrx_dfe_h1h2h3_lcl_off_va[16] | | 0000 0000 | 0000 |
| 0000 0000 | | | |
| 0x81800788: 22_hssrx_dfe_ofs_val[00][00] | | 0c7b 7f00 | 097d |
| 0000 097c 7f00 | | | |
| 0x81800788: 22_hssrx_dfe_ofs_val[03][00] | | 7b03 007f | 7f7d |
| 0000 0200 0000 | | | |
| 0x81800788: 22_hssrx_dfe_ofs_val[06][00] | | 7b7f 0000 | 7903 |
| 0000 0402 7f00 | | | |
| 0x81800788: 22_hssrx_dfe_ofs_val[09][00] | | 067b 7f00 | 7b7d |
| 0000 027b 0000 | | | |
| 0x81800788: 22_hssrx_dfe_ofs_val[12][00] | | 7901 0000 | 7903 |
| 0000 087c 7f00 | | | |
| 0x81800788: 22_hssrx_dfe_ofs_val[15][00] | | 7f04 007f | 7d04 |
| 0000 087d 7f00 | | | |
| 0x81800788: 22_hssrx_dfe_ofs_val[18][00] | | 0906 7f00 | 7d03 |
| 0000 007f 0000 | | | |
| 0x81800788: 22_hssrx_dfe_ofs_val[21][00] | | 007f 0000 | 007f |
| 0000 007f 0000 | | | |
| 0x81800788: 22_hssrx_dfe_ofs_val[24][00] | | 057d 7f00 | 0501 |
| 0000 7f7b 0000 | | | |
| 0x81800794: 25_hssrx_max_gain_path_idx_res[00] | | 005f 0840 | 1111 |
| 18be 2100 28ba 30a0 3800 | | | |
| 0x81800794: 25_hssrx_max_gain_path_idx_res[08] | | 40b0 4890 | 5080 |
| 5800 6044 6800 70fe 7800 | | | |

```

0x818007c4: 31_hssrx_dfe_tap[00]          fffe 8080  0000
0000  0030 0030  3030 3030
0x818007c4: 31_hssrx_dfe_tap[08]          3030 3030  3030
0000
0x818007e8: 3A_hssrx_ac_cpl_cur_src_adj[00]    0041 0041  0041
0041
0x818007ec: 3B_hssrx_dcd_ctl[00]              7c42 5c00  7c85
5c00  7c00
0x818007f0: 3C_hssrx_dcc_ctl[00]              0d83 0d81  0d00
0d81
0x818007f4: 3D_hssrx_qcc_ctl[00]              6982 6949

```

xfipcs, fec, aec, & aet registers

=====

```

0x81c18400: xfipcs_reg          [00] 00002040 00000080 00000000
00000000  00000001 00000008 00000000 00000000
0x81c18420: xfipcs_reg          [08] 00008c01 00000000 00000000
00000000  00000000 00000000 00000000 00000000
0x81c18440: xfipcs_reg          [16] 00000000 00000000 00000000
00000000  00000040 00000000 00000000 00000000
0x81c18460: xfipcs_reg          [24] 00000000 00000000 00000000
00000000  00000000 00000000 00000000 00000000
0x81c18480: xfipcs_reg          [32] 00000004 00000000 00000000
00000000  00000000 00000000 00000000 00000000
0x81c18620: fec_32g_128g_reg    [08] 00000000 00000000 00000000
00000000  00000000 00000000 00000000
0x81c18648: fec_32g_128g_reg    [18] 00000000 00000000 00000000
00000000  00000000 00000000 00000000
0x81c18a00: aec_reg             [00] 00000000 00000000 00000000
00000000  00000000 00000000 00000000
0x81c18c00: aet_reg             [00] 00000000 00000000 00000000
00000000  00000000

```

bbc registers

=====

```

0x81c19800: bbc_trc             0  0  0  0  0  0  0
0
0x81c19840: bbc_trc             0  0  0  0  0  0  0
0
0x81c19880: bbc_trc             0  0  0  0  0  0  0
0
0x81c198c0: bbc_trc             0  0  0  0  0  0  0
0
0x81c19900: bbc_trc             0  0  0  0  0  0  0
0
0x81c19804: bbc_mbc             0  0  0  0  0  0  0
0
0x81c19844: bbc_mbc             0  0  0  0  0  0  0
0
0x81c19884: bbc_mbc             0  0  0  0  0  0  0
0
0x81c198c4: bbc_mbc             0  0  0  0  0  0  0
0
0x81c19904: bbc_mbc             0  0  0  0  0  0  0

```

| | | | | | | | |
|-------------------------------------|----------|---|---|---|---|----------------------|---|
| 0 | | | | | | | |
| 0x81c19a00: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c19a20: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c19a40: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c19a60: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c19a80: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c19c00: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c19c20: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c19c40: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c19c60: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c19c80: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c19d00: bbc_fbpc | 00000000 | | | | | 0x81c19d04: bbc_csc | |
| 00000000 | | | | | | | |
| 0x81c19d08: bbc_rcc_inc | 00000000 | | | | | 0x81c19d0c: | |
| bbc_rqc_inc | 00000000 | | | | | | |
| 0x81c19d10: bbc_fbpc_inc | 00000000 | | | | | 0x81c19d14: | |
| bbc_tmc_inc | 00000000 | | | | | | |
| 0x81c19d18: bbc_threshold | 00080100 | | | | | 0x81c19d1c: | |
| bbc_counter_clr | 00000000 | | | | | | |
| 0x81c19d20: bbc_debug_en | 00000000 | | | | | 0x81c19d24: bbc_ctrl | |
| 00200020 | | | | | | | |
| 0x81c19d28: bbc_rqc_rcc_thresh | 00000055 | | | | | 0x81c19d34: | |
| bbc_bb_sc_n | 00000000 | | | | | | |
| 0x81c19d38: bbc_crd_reco_debug | 00000000 | | | | | 0x81c19d3c: | |
| bbc_crd_reco_debug_data | 00000000 | | | | | | |
| 0x81c19d40: bbc_multi_frm_loss_cnt | 00000000 | | | | | 0x81c19d44: | |
| bbc_multi_rdy_loss_cnt | 00000000 | | | | | | |
| 0x81c19d48: bbc_1frm_loss_recov_cnt | 00000000 | | | | | 0x81c19d4c: | |
| bbc_1rdy_loss_recov_cnt | 00000000 | | | | | | |
| 0x81c19d58: bbc_int_status | 00000000 | | | | | 0x81c19d5c: | |
| bbc_int_set | 00000000 | | | | | | |
| 0x81c19d60: bbc_int_first | 00000000 | | | | | 0x81c19d64: | |
| bbc_frm_rdy_rx_err_addr | 00000000 | | | | | | |
| 0x81c19d68: bbc_frm_rdy_tx_err_addr | 00000000 | | | | | 0x81c19d6c: | |
| bbc_trc_mbc_err_addr | 00000000 | | | | | | |
| 0x81c19d70: bbc_frm_rdy_rx_dbl_ecc | 00000000 | | | | | 0x81c19d74: | |
| bbc_frm_rdy_tx_dbl_ecc | 00000000 | | | | | | |
| 0x81c19d78: bbc_trc_mbc_dbl_ecc | 00000000 | | | | | | |
| 0x81c19d7c: bbc_fsm_status | 00001011 | | | | | 0x81c19d80: | |
| bbc_force_err | 00000000 | | | | | | |
| 0x81c19d84: bbc_crdt_avail0 | ffffffff | | | | | 0x81c19d88: | |
| bbc_crdt_avail1 | 000000ff | | | | | | |
| 0x81c19d8c: bbc_scratch | 00000000 | | | | | | |

FPS registers

=====

| | | | |
|-------------|---------------------|----------|-------------|
| 0x81c18004: | fps_er_enc_in | 00000000 | 0x81c18008: |
| | fps_er_crc | 00000000 | |
| 0x81c1800c: | fps_er_trunc | 00000000 | 0x81c18010: |
| | fps_er_toolong | 00000000 | |
| 0x81c18014: | fps_er_bad_eof | 00000000 | 0x81c18018: |
| | fps_er_enc_out | 00000000 | |
| 0x81c1801c: | fps_er_bad_os | 00000000 | 0x81c18020: |
| | fps_er_flush | 00000000 | |
| 0x81c18024: | fps_er_ifg | 00000000 | 0x81c18038: |
| | fps_er_crc_good_eof | 00000000 | |
| 0x81c1803c: | fps_inv_arb | 00000000 | 0x81c18040: |
| | fps_slow_sts_status | 00000000 | |
| 0x81c18044: | fps_tx_frm_cnt | 00000000 | 0x81c18048: |
| | fps_rx_frm_cnt | 00000000 | |
| 0x81c18050: | fps_tx_word_cnt_hi | 00000000 | 0x81c1804c: |
| | fps_tx_word_cnt_lo | 00000000 | |
| 0x81c18058: | fps_rx_word_cnt_hi | 00000000 | 0x81c18054: |
| | fps_rx_word_cnt_lo | 00000000 | |

BAL registers

=====

| | | | |
|-------------|---------------------|----------|-------------|
| 0x81c1f000: | bal_desired_buf | 00000000 | 0x81c1f004: |
| | bal_alloc_buf | 00000000 | |
| 0x81c1f008: | bal_busy_buf | 00000000 | 0x81c1f00c: |
| | bal_usable_buf | 00000000 | |
| 0x81c1f010: | bal_max_bor_buf | 00000000 | |
| 0x81c1f014: | bal_busy_buf_thresh | 00000002 | |

TXQ registers

=====

| | | | |
|-------------|-------------------------|------------------------|--|
| 0x81c1b004: | txq_phys_port_ctl | 00430000 | |
| 0x81c1b050: | txq_link_skew | 00000000 | |
| 0x81c1b068: | txq_cr_lk_dttm_intr_sts | [00] 00000000 00000000 | |
| 0x81c1b070: | txq_cr_lk_dttm_intr_en | [00] 00000000 00000000 | |
| 0x81c1b024: | txq_disc_frm_trap_cnt | 00000014 | |

FDS registers

=====

| | | | |
|-------------|--------------------------|----------|-------------|
| 0x81c1c000: | fds_rxf_ctl | 00000002 | 0x81c1c004: |
| | fds_rxf_wait_thresh | 00000909 | |
| 0x81c1c018: | fds_rxf_first_error | 00000000 | 0x81c1c01c: |
| | fds_rxf_first_error_info | 00000000 | |
| 0x81c1c020: | fds_rxf_inout_pkt_cnt | 00000000 | |
| 0x81c1c008: | fds_rxf_err_int_status | 00000000 | 0x81c1c024: |
| | fds_rxf_fifo_status | 00888888 | |
| 0x81c1d000: | fds_txf_ctl | 0000003a | 0x81c1d004: |
| | fds_txf_wait_ifg_thresh | 00a00106 | |
| 0x81c1d008: | fds_txf_err_int_status | 00000000 | 0x81c1d024: |
| | fds_txf_fifo_status | 00088888 | |
| 0x81c1d02c: | fds_txf_bbc_scs | 00000000 | |

Logical TXQ registers

```

=====
0x81c1b000: txq_log_port_ctl          00000002    0x81c1b008:
txq_port_status          00000000
0x81c1b00c: txq_todo_flags                    [00] 00000000 00000000
0x81c1b014: txq_spd_match_desc          [00] 00000000 00000000 00000000
00000000
0x81c1b024: txq_spd_match_desc          [04] 00000014
0x81c1b028: txq_vc_weight                [00] 01010101 01010101 01010101
01010101
0x81c1b038: txq_vc_weight                [04] 01010101 01010101 01010101
01010101
0x81c1b048: txq_vc_weight                [08] 01010101 00010101
0x81c1b054: txq_cong_dttm_ctrl          00000000
0x81c1b058: txq_cong_dttm_intr_sts        [00] 00000000 00000000
0x81c1b060: txq_cong_dttm_intr_en            [00] 00000000 00000000
0x81c1b078: txq_bw_limit_en_reg                [00] 00000000 00000000
0x81c1b080: txq_bw_gua_en_reg                  [00] 00000000 00000000
0x81c1b088: txq_vc_group                        [00] 03030300 03030303 03030303
03030303
0x81c1b098: txq_vc_group                        [04] 03030303 03030303 03030303
03030303
0x81c1b0a8: txq_vc_group                        [08] 03030303 03030303 00000000
00000000
0x81c1b0b0: txq_bw_thresh_group            [00] 00000000 00000000 00000000
00000000
0x81c1b0c0: txq_bw_thresh_group            [04] 00000000 00000000 00000000
00000000
0x81c1b0d0: txq_bw_thresh_group            [08] 00000000 00000000 00000000
00000000
0x81c1b0e0: txq_bw_thresh_group            [12] 00000000 00000000 00000000
00000000
0x81c1b0f0: txq_bw_thresh_group            [16] 00000000 00000000 00000000
00000000
0x81c1b100: txq_bw_thresh_group            [20] 00000000 00000000 00000000
00000000
0x81c1b110: txq_bw_thresh_group            [24] 00000000 00000000 00000000
00000000
0x81c1b120: txq_bw_thresh_group            [28] 00000000 00000000 00000000
00000000
0x81c1b130: txq_bw_thresh_group            [32] 00000000 00000000 00000000
00000000
0x81c1b140: txq_bw_thresh_group            [36] 00000000 00000000 00000000
00000000

```

txq Congestion detection Statistics RAM

```

=====
0x810901e0: vc[0]          00000000    0x810901e4: vc[1]
00000000
0x810901e8: vc[2]          00000000    0x810901ec: vc[3]
00000000
0x810901f0: vc[4]          00000000    0x810901f4: vc[5]
00000000
0x810901f8: vc[6]          00000000    0x810901fc: vc[7]
00000000

```


| | | |
|--------------------|----------|--------------------|
| 0x81090200: vc[8] | 00000000 | 0x81090204: vc[9] |
| 00000000 | | |
| 0x81090208: vc[10] | 00000000 | 0x8109020c: vc[11] |
| 00000000 | | |
| 0x81090210: vc[12] | 00000000 | 0x81090214: vc[13] |
| 00000000 | | |
| 0x81090218: vc[14] | 00000000 | 0x8109021c: vc[15] |
| 00000000 | | |
| 0x81090220: vc[16] | 00000000 | 0x81090224: vc[17] |
| 00000000 | | |
| 0x81090228: vc[18] | 00000000 | 0x8109022c: vc[19] |
| 00000000 | | |
| 0x81090230: vc[20] | 00000000 | 0x81090234: vc[21] |
| 00000000 | | |
| 0x81090238: vc[22] | 00000000 | 0x8109023c: vc[23] |
| 00000000 | | |
| 0x81090240: vc[24] | 00000000 | 0x81090244: vc[25] |
| 00000000 | | |
| 0x81090248: vc[26] | 00000000 | 0x8109024c: vc[27] |
| 00000000 | | |
| 0x81090250: vc[28] | 00000000 | 0x81090254: vc[29] |
| 00000000 | | |
| 0x81090258: vc[30] | 00000000 | 0x8109025c: vc[31] |
| 00000000 | | |
| 0x81090260: vc[32] | 00000000 | 0x81090264: vc[33] |
| 00000000 | | |
| 0x81090268: vc[34] | 00000000 | 0x8109026c: vc[35] |
| 00000000 | | |
| 0x81090270: vc[36] | 00000000 | 0x81090274: vc[37] |
| 00000000 | | |
| 0x81090278: vc[38] | 00000000 | 0x8109027c: vc[39] |
| 00000000 | | |

Logical STS registers

=====

| | | |
|----------------------------------|----------------------------|------------------------------|
| 0x815842c4: sts_ftb_type1_miss | 00000000 | |
| 0x815842c8: sts_ftb_type2_miss | 00000000 | |
| 0x815842cc: sts_ftb_type6_miss | 00000000 | |
| 0x815842d0: sts_hard_zoning_miss | 00000000 | |
| 0x815842d4: sts_lun_zoning_miss | 00000000 | |
| 0x815842dc: sts_unroutable | 00000000 | |
| 0x815812f4: sts_rte_cl2 | 00000000 | 0x815812f8: |
| sts_rte_cl3 | 00000000 | 0x815812fc: sts_rte_link_ctl |
| 00000000 | 0x815842e8: sts_tx_timeout | 00000000 |

Logical STS filter registers

=====

| | | | | |
|-------------------------|------|----------|----------|----------|
| 0x81584240: stsflt_trig | [00] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584250: stsflt_trig | [04] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584260: stsflt_trig | [08] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |

| | | | | |
|-------------------------|------|----------|----------|----------|
| 0x81584270: stsflt_trig | [12] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584280: stsflt_trig | [16] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584290: stsflt_trig | [20] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x815842a0: stsflt_trig | [24] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x815842b0: stsflt_trig | [28] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x815842c0: stsflt_trig | [32] | | | |

Logical STS discard registers

=====

| | | |
|------------------------------------|----------|-------------|
| 0x8158145c: disc_mcast_wka | 00000000 | 0x81581460: |
| disc_inv_did | 00000000 | |
| 0x81581464: disc_cll_cl4 | 00000000 | 0x81581468: |
| disc_sid_chk_fail | 00000000 | |
| 0x8158146c: disc_inv_dom_egid_txpt | 00000000 | 0x81581470: |
| disc_vft_hop_cnt_1 | 00000000 | |
| 0x81581474: disc_classf | 00000000 | 0x81581478: |
| disc_fcp_cdb_inv | 00000000 | |
| 0x8158147c: disc_vfid_trap_enabled | 00000000 | 0x81581480: |
| disc_vfid_hdr_chk_fail | 00000000 | |
| 0x81581484: disc_shim_cksum_fail | 00000000 | 0x81581488: |
| disc_fed_edit_cmd_err | 00000000 | |
| 0x8158148c: disc_ftb_vm_mode | 00000000 | 0x81581490: |
| disc_ftb_agnt2_miss | 00000000 | |
| 0x81581494: disc_ecb_reserved | 00000000 | 0x81581498: |
| disc_ecb_de_pad_err | 00000000 | |
| 0x8158149c: disc_ecb_de_tag_err | 00000000 | 0x815814a0: |
| disc_ecb_de_seq_err | 00000000 | |
| 0x815814a4: disc_ecb_err | 00000000 | 0x815814a8: |
| disc_ftb_type4_match | 00000000 | |
| 0x815814ac: disc_fcp_rsp_ftb_type4 | 00000000 | 0x815814b0: |
| disc_ftb_type5_match | 00000000 | |
| 0x815814b4: disc_ftb_type3_match | 00000000 | 0x815814b8: |
| disc_els_ftb_type3 | 00000000 | |
| 0x815814bc: disc_ftb_type1_match | 00000000 | 0x815814c0: |
| disc_els_rsp_ex_port | 00000000 | |
| 0x815814c4: disc_inv_drp_dps | 00000000 | 0x815814c8: |
| disc_did_lookup_miss | 00000000 | |
| 0x815814cc: disc_ftb_type2_match | 00000000 | 0x815814d0: |
| disc_trpd_plogi_pdisc | 00000000 | |
| 0x815814d4: disc_type2_lookup_miss | 00000000 | 0x815814d8: |
| disc_ftb_type6_match | 00000000 | |
| 0x815814dc: disc_els_rep_ex_port | 00000000 | 0x815814e0: |
| disc_els_sid_lkup_bit1 | 00000000 | |
| 0x815814e4: disc_els_sid_lkup_bit0 | 00000000 | 0x815814e8: |
| disc_bls_frm_trap_bit1 | 00000000 | |
| 0x815814ec: disc_ftb_token_err | 00000000 | 0x815814f0: |
| disc_asic_internal_err | 00000000 | |
| 0x815814f4: disc_hard_zone_miss | 00000000 | 0x815814f8: |
| disc_lun_zone_miss | 00000000 | |

```

0x815814fc: disc_flt_frame_disc      00000000      0x81581500:
disc_flt_parity_err      00000000
0x81581504: disc_frame_marked_du      00000000      0x81581508:
disc_frame_marked_to      00000000
0x8158150c: disc_lkup_rte_prty_err  00000000

```

portstatsshow 58

```

stat_wtx      0      4-byte words transmitted
stat_wrx      0      4-byte words received
stat_ftx      0      Frames transmitted
stat_frx      0      Frames received
stat_c2_frx   0      Class 2 frames received
stat_c3_frx   0      Class 3 frames received
stat_lc_rx    0      Link control frames
received
stat_mc_rx    0      Multicast frames
received
stat_mc_to    0      Multicast timeouts
stat_mc_tx    0      Multicast frames
transmitted
tim_txcrd_z   0      Time TX Credit Zero
(2.5Us ticks)
tim_txcrd_z_vc 0- 3: 0      0      0      0
tim_txcrd_z_vc 4- 7: 0      0      0      0
tim_txcrd_z_vc 8-11: 0     0      0      0
tim_txcrd_z_vc 12-15: 0    0      0      0
lat_tot_pkt_vc 0- 3: 1      1      1      1
lat_tot_pkt_vc 4- 7: 1      1      1      1
lat_tot_pkt_vc 8-11: 1     1      1      1
lat_tot_pkt_vc 12-15: 1    1      1      1
lat_hi_time_vc 0- 3: 0      0      0      0
lat_hi_time_vc 4- 7: 0      0      0      0
lat_hi_time_vc 8-11: 0     0      0      0
lat_hi_time_vc 12-15: 0    0      0      0
lat_lo_time_vc 0- 3: 1      1      1      1
lat_lo_time_vc 4- 7: 1      1      1      1
lat_lo_time_vc 8-11: 1     1      1      1
lat_lo_time_vc 12-15: 1    1      1      1
max_latency_vc 0- 3: 1      1      1      1
max_latency_vc 4- 7: 1      1      1      1
max_latency_vc 8-11: 1     1      1      1
max_latency_vc 12-15: 1    1      1      1
latency_dma_ts 09-09-2024 UTC Mon 08:47:26      TXQ
Latency DMA TimeStamp
fec_cor_detected 0      Count of blocks that
were corrected by FEC
fec_uncor_detected 0     Count of blocks that
were left uncorrected by FEC
er_enc_in      0      Encoding errors inside
of frames
er_crc         0      Frames with CRC errors
er_trunc       0      Frames shorter than
minimum

```

| | | |
|---|-----------------------------|--------------------------|
| er_toolong maximum | 0 | Frames longer than |
| er_bad_eof frame | 0 | Frames with bad end-of- |
| er_enc_out of frames | 0 | Encoding error outside |
| er_bad_os | 0 | Invalid ordered set |
| er_pcs_blk | 0 | PCS block errors |
| er_rx_c3_timeout discarded due to timeout | 0 | Class 3 receive frames |
| er_tx_c3_timeout discarded due to timeout | 0 | Class 3 transmit frames |
| er_unroutable unroutable | 0 | Frames that are |
| er_unreachable destination | 0 | Frame with unreachable |
| er_other_discard | 0 | Other discards |
| er_type1_miss miss | 0 | frames with FTB type 1 |
| er_type2_miss miss | 0 | frames with FTB type 2 |
| er_type6_miss miss | 0 | frames with FTB type 6 |
| er_zone_miss miss | 0 | frames with hard zoning |
| er_lun_zone_miss miss | 0 | frames with LUN zoning |
| er_crc_good_eof | 0 | Crc error with good eof |
| er_inv_arb | 0 | Invalid ARB |
| er_single_credit_loss on link | 0 | Single vcrdy/frame loss |
| er_multi_credit_loss loss on link | 0 | Multiple vcrdy/frame |
| other_credit_loss credit loss | 0 | Link timeout/complete |
| phy_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | Timestamp of |
| phy_port stats clear | | |
| lgc_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | Timestamp of |
| lgc_port stats clear | | |
| fec_corrected_rate second | 0 | FEC Corrected blocks per |

portstats64show 58

| | | |
|---------------|---|---------------------------------------|
| stat64_wtx | 0 | top_int : 4-byte words transmitted |
| | 0 | bottom_int : 4-byte words transmitted |
| stat64_wrx | 0 | top_int : 4-byte words received |
| | 0 | bottom_int : 4-byte words received |
| stat64_ftx | 0 | top_int : Frames transmitted |
| | 0 | bottom_int : Frames transmitted |
| stat64_frx | 0 | top_int : Frames received |
| | 0 | bottom_int : Frames received |
| stat64_c2_frx | 0 | top_int : Class 2 frames received |
| | 0 | bottom_int : Class 2 frames received |
| stat64_c3_frx | 0 | top_int : Class 3 frames received |

| | | |
|------------------------------|---|---|
| stat64_lc_rx | 0 | bottom_int : Class 3 frames received |
| | 0 | top_int : Link control frames received |
| | 0 | bottom_int : Link control frames received |
| stat64_mc_rx | 0 | top_int : Multicast frames received |
| | 0 | bottom_int : Multicast frames received |
| stat64_mc_to | 0 | top_int : Multicast timeouts |
| | 0 | bottom_int : Multicast timeouts |
| stat64_mc_tx | 0 | top_int : Multicast frames transmitted |
| | 0 | bottom_int : Multicast frames transmitted |
| tim64_rdy_pri | 0 | top_int : Time R_RDY high priority |
| | 0 | bottom_int : Time R_RDY high priority |
| tim64_txcrd_z | 0 | top_int : Time BB_credit zero |
| | 0 | bottom_int : Time BB_credit zero |
| er64_enc_in | 0 | top_int : Encoding errors inside of |
| frames | 0 | bottom_int : Encoding errors inside of |
| er64_crc | 0 | top_int : Frames with CRC errors |
| | 0 | bottom_int : Frames with CRC errors |
| er64_trunc | 0 | top_int : Frames shorter than minimum |
| | 0 | bottom_int : Frames shorter than minimum |
| er64_toolong | 0 | top_int : Frames longer than maximum |
| | 0 | bottom_int : Frames longer than maximum |
| er64_bad_eof | 0 | top_int : Frames with bad end-of-frame |
| | 0 | bottom_int : Frames with bad end-of- |
| er64_enc_out | 0 | top_int : Encoding error outside of |
| frames | 0 | bottom_int : Encoding error outside of |
| er64_disc_c3 | 0 | top_int : Class 3 frames discarded |
| | 0 | bottom_int : Class 3 frames discarded |
| er64_pcs_blk | 0 | top_int : PCS block errors |
| | 0 | bottom_int : PCS block errors |
| stat64_rateTxFrame | 0 | Tx frame rate (fr/sec) |
| stat64_rateRxFrame | 0 | Rx frame rate (fr/sec) |
| stat64_rateTxPeakFrame | 0 | Tx peak frame rate (fr/sec) |
| stat64_rateRxPeakFrame | 0 | Rx peak frame rate (fr/sec) |
| stat64_rateTxWord | 0 | Tx Word rate (words/sec) |
| stat64_rateRxWord | 0 | Rx Word rate (words/sec) |
| stat64_rateTxPeakWord | 0 | Tx peak Word rate (words/sec) |
| stat64_rateRxPeakWord | 0 | Rx peak Word rate (words/sec) |
| stat64_PRJTFrames | 0 | top_int : Number of PRJT frames |
| returned to this port | 0 | bottom_int : Number of PRJT |
| frames returned to this port | 0 | top_int : Number of PBSY frames |
| stat64_PBSYFrames | 0 | bottom_int : Number of PBSY |
| returned to this port | 0 | top_int : Number of occurrences |
| frames returned to this port | 0 | |
| stat64_inputBuffersFull | 0 | |
| when all input buffers full | | |

```

0 bottom_int : Number of
occurrences when all input buffers full
stat64_rxClass1Frames 0 top_int : Number of class 1
frames received
0 bottom_int : Number of class 1
frames received
stat64_aveTxFrameSize 0 Average Tx Frame size
stat64_aveRxFrameSize 0 Average Rx Frame size
Lr_in 0 top_int
0 bottom_int
Ols_in 0 top_int
0 bottom_int
Lr_out 0 top_int
0 bottom_int
Ols_out 0 top_int
0 bottom_int
Link_failure 0 top_int
0 bottom_int
Invalid_CRC 0 top_int
0 bottom_int
Invalid_word 0 top_int
0 bottom_int
Protocol_err 0 top_int
0 bottom_int
Loss_of_sig 0 top_int
0 bottom_int
Loss_of_sync 0 top_int
0 bottom_int
er_bad_os 0 top_int : Invalid ordered set
0 bottom_int: Invalid ordered set

```

```

portrouteshow 58
port address ID: 0x013a00
external unicast routing table:
0: Embedded
255: Embedded
internal unicast routing table:
0: Embedded

```

portcamshow 58

```

-----
Port  SID used  DID used  SID entries  DID entries
58    0         0        000000      000000
-----

```

ptbufshow, ptcreditshow, ptdatashow, ptstatsshow 58

```

S:
S:VF Enable:          1
S:

```

S:C4 Global Variable:

```

S:-----
-----

```

```

S:trace_stop:        0

```

```

S:
S:C4 Phy Data Pointers: c4_phyp = 0xb6ab6180
S:-----
-----
S:tnodep                0xbb82e540      pt
      0x43028003
S:proto_phyp            0xb8806360      phy_cfg
0xb6ab8000
S:c4_chp                0x97e28000      c4_lgcp
0x97f54000
S:c4_phy_regp           0x81c18000      proc_dir
0xb85131e0
S:-----
-----
S:magic_id              0xc4345678      num_port_timer    12
S:prev_if_id            0x43020003      S:ftx              0
      tov          0
S:initialized           0                port_idx           3
S:ui_idx                58              slot_no
      0
S:blade_idx             3                sw_usr_ports       400
S:unused                0                intr_debounced
      0
S:aec_status            0x0             reason_code
      0
S:debug                 0x00000004      debug_trc_line     0
S:rxbuf_list_head       0xffffffff      rxbuf_list_tail
0xffffffff
S:isAePort              0                port_misc_data
      0
S:num_fault1_rx_disc    0                num_fault2_rx_disc 0
S:p_lli_cause0          0                p_sig_regained     0
S:p_sync_regained       0                enc_out
      0x0
S:cached_fps_status     0                cached_sts_status  0
S:cached_er_crc_good_eof 0
S:cached_er_bad_os      0                cached_er_too_long 0
S:cached_er_trunc       0
cached_tot_er_crc_good_eof 0
S:num_pt_excess_intr    0                num_no_fid         0
S:num_fault1_cnt        0                num_fault2_cnt
      0
S:num_fault_lip         0                num_fault_lli      0
S:num_fault_rx_fifo     0                num_fault_hss      0
S:num_fault_bwait       0                lli_intr_prim
      0
S:num_sw_link_to        0
be_link_err_mon_count   0
S:ecb_enc_enabled       0                ecb_comp_enabled
      0
S:ecb_rsv_enc           0                ecb_rsv_comp       0
S:ecb_enc_bm            0x0             ecb_key_index
0xffffffff
S:fab_idx               4

```

```

S:num_be_lto          0          lto_count_reset_intvl
  0
S:lr_count_reset_intvl      0          num_be_lr
  0
S:num_fault_qsfps      0          check_lto
  0
S:credit_loaded          0          num_credit_overrun
  0
S:fec_enabled           0x0          fec_los_to_flag          0x0
S:phy_stats_clear_ts      1725611419  pcs_err_online
  0
S:pcs_err_light_det      0          pcs_err_ignore
  0
S:pcs_blk_err           0          pcs_hiber          0
S:phy_port_status        0          ecb_enc_lr_count
  0

S:dport_mode            0          avoid_lto_det          0
S:sn_debounced          0x0        sn_started_kr_reqd     0
S:major_timer_started    0x0        ready_bm              0x0
S:parln_1_bm            0x0        parln_0_bm           0x0
S:be_los_of_sync_event_intvl
be_los_of_sync_event      0
S:errataPtenable_cntr    0          errataPoll_cntr
  0
S:jda_rx_sig_loss_det    0          jda_rx_sig_loss_cnt
  0

S:encrypt_blk_error      0
S:
S:      c4_trunk
S:=====
S:mark_ts                0x0          deskew          0x0
S:master_phyp            0x0
S:
S:adelay[00]: 0x00000000 0x00000000 0x00000000 0x00000000
S:adelay[04]: 0x00000000 0x00000000 0x00000000 0x00000000
S:
S:      c4_buf
S:=====
S:tx_csc                  0          rx_csc
  0
S:ld_vc_credits          0          tx_flag          0x0
S:alloc_buffers          0          req_buffers      0
S:est_buffers            20          ld_use_est      0
S:bb_sc_n                0          rx_bb_sc_n
  0
S:data_cr                 5          nondata_cr
  6
S:cr_enable              0
S:ld_nondata_cr          6          tnodep
0xbb82e620
S:tx_credits[0] 0 0 0 0 0 0 0 0
S:tx_credits[8] 0 0 0 0 0 0 0 0
S:tx_credits[16] 0 0 0 0 0 0 0 0 0
S:tx_credits[24] 0 0 0 0 0 0 0 0 0

```



```

S:tx_credits[32]      0      0      0      0      0      0      0      0      0
S:rx_credits[0] 0    0    0    0    0    0    0    0    0
S:rx_credits[8] 0    0    0    0    0    0    0    0    0
S:rx_credits[16]      0    0    0    0    0    0    0    0    0
S:rx_credits[24]      0    0    0    0    0    0    0    0    0
S:rx_credits[32]      0    0    0    0    0    0    0    0    0
S:tx_mbc[0]      0    0    0    0    0    0    0    0    0
S:tx_mbc[8]      0    0    0    0    0    0    0    0    0
S:tx_mbc[16]     0    0    0    0    0    0    0    0    0
S:tx_mbc[24]     0    0    0    0    0    0    0    0    0
S:tx_mbc[32]     0    0    0    0    0    0    0    0    0
S:rx_mbc[0]      0    0    0    0    0    0    0    0    0
S:rx_mbc[8]      0    0    0    0    0    0    0    0    0
S:rx_mbc[16]     0    0    0    0    0    0    0    0    0
S:rx_mbc[24]     0    0    0    0    0    0    0    0    0
S:rx_mbc[32]     0    0    0    0    0    0    0    0    0

```

S:

S:C4 Chip Variables: c4_phyp->c4_chp = 0x97e28000

S:-----

S:version = 2.1

S:magic_id 0xc4234567 init_state 0x8

S:reset_reg_mem 0x1

S:ch_int0_en_bm 0x0 intr0_cause 0x0

S:ch_int1_en_bm 0x0 intr1_cause 0x0

S:ch_int2_en_bm 0x0 intr2_cause 0x0

S:ch 0x43010080 ch_cfg

0xb7013ba0

S:raslog_hndl.hndl 0x0 obj_halted 0x0

S:c4_chip_regp 0x80000000 c4_fpg_regp

0x81800000

S:num_chip_timer 0x5

S:hi_task_bm 0x0 lo_task_bm 0x0

S:c4_deferq.q_head 0x0 c4_deferq.q_tail 0x0

S:c4_tmrq.q_head 0x0 c4_tmrq.q_tail 0x0

slot_no 0

S:chip_inst 0 chip_idx 0

S:pll_initialized 1

pll_serdes_initialized 1

S:init_tries 0 init_ptEnableBM

0xba01b488

S:tick_polling 0xb980c9c0 sec_polling

0xb980c960

S:bb_fid 129

S:ecb_key_bm[0] 0x0 ecb_key_bm[1] 0x0

S:ecb_key_bm[2] 0x0 ecb_key_bm[3] 0x0

S:is_chip_enc_enabled 0

is_chip_comp_enabled 0x0

S:ftb_rsrcp->ftb_flags 0x0 act_rsrcp->act_flag 0x1

S:lue_rsrcp->lue_flags[0] 0x0 lue_rsrcp-

>lue_flags[1] 0x0

S:c4_phyp[00]: 0xb6ab0000 0xb6ab2080 0xb6ab4100 0xb6ab6180

S:c4_phyp[04]: 0xb6ab9040 0xb6abb0c0 0xb6abd140 0xb6ac0000

S:c4_phyp[08]: 0xb6ac2080 0xb6ac4100 0xb6ac6180 0xb6ac9040

```

S:c4_phyp[12]: 0xb6acb0c0 0xb6acd140 0xb6ad0000 0xb6ad2080
S:c4_phyp[16]: 0xb6ad4100 0xb6ad6180 0xb6ad9040 0xb6adb0c0
S:c4_phyp[20]: 0xb6add140 0xb6ae0000 0xb6ae2080 0xb6ae4100
S:c4_phyp[24]: 0xb6ae6180 0xb6ae9040 0xb6aeb0c0 0xb6aed140
S:c4_phyp[28]: 0xb6af0000 0xb6af2080 0xb6af4100 0xb6af6180
S:c4_phyp[32]: 0xb6af9040 0xb6afb0c0 0xb6afd140 0xb6b00000
S:c4_phyp[36]: 0xb6b02080 0xb6b04100 0xb6b06180 0xb6b09040
S:c4_phyp[40]: 0xb6b0b0c0 0xb6b0d140 0xb6b10000 0xb6b12080
S:c4_phyp[44]: 0xb6b14100 0xb6b16180 0xb6b19040 0xb6b1b0c0
S:c4_phyp[48]: 0xb6b1d140 0xb6b20000 0xb6b22080 0xb6b24100
S:c4_phyp[52]: 0xb6b26180 0xb6b29040 0xb6b2b0c0 0xb6b2d140
S:c4_phyp[56]: 0xb6b30000 0xb6b32080 0xb6b34100 0xb6b36180
S:c4_phyp[60]: 0xb6b39040 0xb6b3b0c0 0xb6b3d140 0xb6b40000
S:c4_lgcp[00]: 0x97f48000 0x97f4c000 0x97f50000 0x97f54000
S:c4_lgcp[04]: 0x97f58000 0x97f5c000 0x97f60000 0x97f64000
S:c4_lgcp[08]: 0x97f68000 0x97f6c000 0x97f70000 0x97f74000
S:c4_lgcp[12]: 0x97f78000 0x97f7c000 0x97f80000 0x97f84000
S:c4_lgcp[16]: 0x97f88000 0x97f8c000 0x97f90000 0x97f94000
S:c4_lgcp[20]: 0x97f98000 0x97f9c000 0x97fa0000 0x97fa4000
S:c4_lgcp[24]: 0x97fa8000 0x97fac000 0x97fb0000 0x97fb4000
S:c4_lgcp[28]: 0x97fb8000 0x97fbc000 0x97fc0000 0x97fc4000
S:c4_lgcp[32]: 0x97fc8000 0x97fcc000 0x97fd0000 0x97fd4000
S:c4_lgcp[36]: 0x97fd8000 0x97fdc000 0x97fe0000 0x97fe4000
S:c4_lgcp[40]: 0x97fe8000 0x97fec000 0x97ff0000 0x97ff4000
S:c4_lgcp[44]: 0x97ff8000 0x97ffc000 0x8e000000 0x8e004000
S:c4_lgcp[48]: 0x8e008000 0x8e00c000 0x8e010000 0x8e014000
S:c4_lgcp[52]: 0x8e018000 0x8e01c000 0x8e020000 0x8e024000
S:c4_lgcp[56]: 0x8e028000 0x8e02c000 0x8e030000 0x8e034000
S:c4_lgcp[60]: 0x8e038000 0x8e03c000 0x8e040000 0x8e044000
S:chip_timers[00]: 0xb980c720 0xb980c780 0xb980c7e0 0xb980c840
S:chip_timers[04]: 0xb980c8a0 0xb980c900
S:disc_trap_enable_required      0x0          rxlp_disc_log_stop
          0x0
S:curr_rxlp_frm_cnt      0x0          curr_rxlp_disc_frm_cnt  0x0
S:sw_disc_frm_cnt      0x0          last_disc_frm_cnt      0x0
S:txq_nopop_pr_cnt      0x0          pollErrataDfe_ptBM
0xba01b4b0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][0]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][1] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][2]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][0] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][1]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][2] 0x0
S:
S:C4 Logical Port Variables
S:-----
-----
S:c4_lgc_regp      0x81c18000
S:c4_phyp:
S:      0xb6ab6180      0x0          0x0          0x0

S:      0x0          0x0          0x0          0x0

S:master_phyp      0xb6ab6180      if_id

```

```

0x43020003
S:min_phyp          0x0          max_phyp          0x0
S:num_phy_ports     1          lgc_num           3
S:num_iu_to         0          sw_txq_bm
0
S:port_fid         129         unused            0
S:port_group       0          lgc_stats_clear_ts
1725611419
S:domain_tbl_sel   0          area_tbl_sel
0
S:egid_tbl_sel     0
S:serv_lo_bm       0x0
S:

```

S:Proto Phy Variables:

S:-----

```

S:magic_id         0xc4123456   asic_phyp
0xb6ab6180
S:port_id          0x43028003   phy_cfg
0xb6ab8000
S:upsm_hdl         0xb800ff00   physm_hdl
0xb800fc80
S:ov_snsn_hdl     0xb800fb40   sw_snsn_hdl
0xb800fbe0
S:ov_lksm_hdl     0xb800fd20   sw_lksm_hdl
0xb800fdc0
S:trksm_hdl       0xb800fe60   lr_flag           0x0
S:lr_active        0x0          qsfm_txxrx_rate_sel
0x0

```

S:

```

S:UPSM            UP00: UPST_PORT_DISABLED  --> UP00: UPST_PORT_DISABLED
S:SNSM(OV)        SN00: OV_SNST_STOPPED    --> SN00: OV_SNST_STOPPED
S:SNSM(SW)        SW00: SW_SNST_STAGE_WS  --> SW00: SW_SNST_STAGE_WS
S:PHYSM           PP00: PHYST_STOPPED      --> PP00: PHYST_STOPPED
S:LKSM(OV)        LK00: OV_LKST_INACTIVE  --> LK00: OV_LKST_INACTIVE
S:LKSM(SW)        SW13: INACTIVE         --> SW13: INACTIVE
S:TRKSM           TRK0: TRKST_INIT       --> TRK0: TRKST_INIT

```

S:
S:physm variables:

S:-----

```

S:proto_phyp      0xb8806360   physm_hdl
0xb800fc80
S:force_offline   0          copper            0
S:fault_reason    0: UNKNOWN
S:phy_media_present 0
S:

```

S:snsn variables:

S:-----

```

S:speed           0xff          proto_phyp
0xb8806360
S:hw_sn_tries_left 0x0          sw_sn_tries_left 0x0
S:curr_txsp_count 0x0          0x0

```

```

S:tx_max          0x0          curr_tx_indx
   0x0
S:curr_tx         0x0          curr_rxsp_count
   0x0
S:rx_max          0x0          curr_rx_indx
   0x0
S:curr_rx         0x0          rx_mem
   0x0
S:rxsp_rec_count  0x0
S:nc_start        0x0          tx_start          0x0
S:sync_start      0x0          sync_present    0x0
S:diag_auto       0x0          diag_speed      0xff
S:striped_wd_tov  3000          hw_wd_tov
   3000
S:step            0x0          qsfp28_speed_mode
   0x0
S:qsfp_mode0_hw_sn_tries_left  0x0
S:qsfp_mode1_hw_sn_tries_left  0x0
S:
S:lksm variables:
S:-----
-----
S:proto_phyp      0xb8806360    ov_lksm_hdl
0xb800fd20
sw_lksm_hdl       0xb800fdc0
num_lf1           0
S:hw_link_tries_left  0          sw_link_tries_left    0
S:buf_ptype       0x0          stored_entry_state    0x6
S:handshake_owner 0x0          mark_unsent
   0x0
S:busybuf_stuck   0x0          lr_wait             0x0
S:
S:trksm variables:
S:-----
-----
S:Not a trunk port
S:
S:upsm variables:
S:-----
-----
S:proto_phyp      0xb8806360    upsm_hdl
0xb800ff00
S:bb_credits      0          port_beacon          0
S:port_diag_flag  0          force_offline
   0
S:port_fault_rsn  0: PORT_NO_FAULT
S:retry_init_rsn  0: UNKNOWN
S:limit_reason    0          limit_result          0
S:ie_fctl_mode    0          fec_in_sync_tries_left  0
S:retry_sn_fail_init  0
retry_link_fail_init  0
S:excess_lr_count  0
S:
S:c4_ch_cfg

```

```

S:-----
-----
S:c4_desc_ring_size      256      292      256      256      292
292      2      292      292
S:thresh_def            0      16      1      0
S:intr_tries            500      cmem_pattern
0xdeadbeef
S:cmem_pattern_upwd     2      cmem_init_time      16
S:cmem_init_tries      5
S:ctrl_par_thresh      2      data_par_thresh
4
S:cam_par_thresh        4      buf_loss_thresh
12
S:crit_par_thresh      2      non_crit_par_thresh
6
S:pci_abort_thresh     10      pci_err_thresh      5
S:excess_chintr_thresh 8      sw_err_thresh      20
S:err_sample_period    300      intr_sleep
20000
S:frame_timeout        2500      proxy_dev      16384
S:vf_route             81920      qos      2048
S:stats 2048          f_redirect      2048
S:rsp_trap             2048      lun_zoning      20480
S:area_mode            0      ftb_max_loop[0]    0
S:ftb_max_loop[1]      6      ftb_max_loop[2]    9
S:ftb_max_loop[3]      10     ftb_max_loop[4]    10
S:ftb_max_loop[5]      5      ftb_max_loop[6]    6
S:ftb_seg_size[0]      0      ftb_seg_size[1]
16384
S:ftb_seg_size[2]      65536     ftb_seg_size[3]
16384
S:ftb_seg_size[4]      16384     ftb_seg_size[5]
65536
S:ftb_seg_size[6]      16384     ftb_seg_base[0]    0
S:ftb_seg_base[1]      0      ftb_seg_base[2]
65536
S:ftb_seg_base[3]      16384     ftb_seg_base[4]
32768
S:ftb_seg_base[5]      131072    ftb_seg_base[6]
49152
asic_err_monitor_period1 300
asic_err_monitor_period2 86400
zone_chk_to_poll_period 25
zone_chk_class2_reject_tov
S:
S:c4_phy_cfg
S:-----
-----
S:version = 2.1
S:pt                    0x43028003      fab_ptr
0x9a800000
S:fabattr                0x9a8000d4      fab_iop
0x9a800050
S:cfgbm                  0xbb82e384      port_ctrl

```

```

0xb6ab8018
S:pcap.pcap_bm          0x8d215547      pcap.pcap2_bm
0x2588289
S:pcap.pcap3_bm        0x1bebe0c
ui_idx                  58              S:slot_no
    0
is_icl                  0              S:sw_usr_ports      400
S:neg_speed             0 0 0 0 0
S:my_domain             0x1            port_mode            0x0
S:hw_sn_maxtries       100           sw_sn_maxtries
    0
S:hw_link_maxtries     10            sw_link_maxtries    5
S:rx_cyc_tov           28            rttov               300
S:bufrdy_tov           300           busybuf_tov         286
S:mark_tov             300           lksm_tov            3000
S:buf_dealloc_wait     4             hw_wd_tov           3000
S:hw_lk_train_tov     540           hw_lk_test_tov
    150
S:syswait_tx_12_lips   1             lip_rx_tov          55
S:al_time_tov          15            lp_tov              2000
S:intr_tries_port      500           intr_mod_debounce
    250
S:intr_lsrflt_debounce 500           intr_efifo_debounce 100
S:port_no_fid           3             excess_ptintr_thresh 8
S:port_fault1_thresh   100           port_fault1_spur_thresh 250
S:port_fault1_disc_thresh 500
port_fault1_disc_spur_thresh 1000
S:port_fault2_thresh   5             losync_tov          100
S:port_sw_link_to      15            en_8g_scramble
    1
frc_hw_sn_mode          0x1
S:enc_poll_thresh      0             fec_enable
    0
S:fec_in_sync_to       50            fec_in_sync_try_max
    4
S:port_be_lto_threshold 100           port_be_lr_threshold
    2
S:be_cr_in_sync_to     5
port_credit_overrun_thresh 10
S:jda_sfp_losig_tov    400
jda_sfp_losig_try_max  30
S:striped_wd_tov       3000
no_sync_debounce       1200
S:
S:    fab_iop
S:=====
S:fab_iop->interop_mode 0x0      fab_iop->lab_mode    0x0
S:fab_iop->fl_bbc       0x0      fab_iop->fl_fan
    0x0
S:fab_iop->fl_cls       0x4      fab_iop->fl_rscn
    0x0
S:fab_iop->domain_id_offset 0x60    fab_iop-
>mcdt_fabric_mode      0x0
S:fab_iop->mcdt_default_zone 0x0      fab_iop-

```

```

>mcdt_safe_zone          0x0
S:
S:   port_ctrl
S:=====
S:port_ctrl.port_type    1          port_ctrl.port_grp      0
S:port_ctrl.port_number 58          port_ctrl.vc_mode        1
S:
S:   port_ctrl.lcap
S:=====
S:has_serdes              0          has_media                1
S:topology                1          skip_nego                 0
S:skip_pnego              0          skip_init_event          0
S:en_shim                  0          speed_neg                 0
S:en_shim                  1
S:loop_back                0          num_speeds                5
S:fec_enable               0
S:
S:   port_ctrl.speed_list array
S:=====
S:speed_list[0].auto_neg  1          speed_list[0].lnk_speed  0x0000000a
S:speed_list[1].auto_neg  1          speed_list[1].lnk_speed  0x00000008
S:speed_list[2].auto_neg  1          speed_list[2].lnk_speed  0x00000006
S:speed_list[3].auto_neg  1          speed_list[3].lnk_speed  0x00000005
S:speed_list[4].auto_neg  1          speed_list[4].lnk_speed  0x00000003
S:speed_list[5].auto_neg  0          speed_list[5].lnk_speed  0x00000000
S:
S:   port_ctrl.cm
S:=====
S:port_ctrl.cm.num_vcs      8
S:port_ctrl.cm.min_bufs     8
S:port_ctrl.cm.cr_shar_bufs 0
S:port_ctrl.vc_alloc
S:port_ctrl.vc_alloc        2 0 1 1 1 1 1 1
S:port_ctrl.vc_alloc        0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.norm_vc_alloc
S:port_ctrl.norm_vc_alloc   4 0 5 5 5 5 1 1
S:port_ctrl.norm_vc_alloc   0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.cm.skip_bb_credit      0
S:port_ctrl.cm.use_shim_based_sublist 0
S:
S:   port_ctrl.serdes_set
S:=====
S:serdes_type                0x8
S:serdes_data_t.ibm_hss_serdes.tx_drive_power      0x1
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b_sign  0x1
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b      0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_a      0x0
S:serdes_data_t.ibm_hss_serdes.rxeq                0x0
S:
S:   cfgbm
S:=====
S:old_distance                0x0          gport_lockdown          0x0

```

```

S:tport          0x1          speed          0x0
S:disable_eport  0x0          fcacc          0x0
S:lport_lockdown 0x0          0x0          priv_lport_lockdown
          0x0
S:vcxlt_linit   0x0          delay_flogi    0x0
S:isl_interop   0x0          distance       0x0
S:BufStarvFlag  0x0          credit_sharing 0x0
S:lport_halfduplex 0x0          lport_fairness 0x0
S:soft_neg      0x0          asn_frc_hwretry 0x0
S:cr_recov      0x0          fport_buffers  0x0
S:export        0x0          0x0          export_mode
          0x0
S:csctl_en      0x0          mirror_port    0x0
S:fault_delay   0x0          non_dfe       0x0
S:fec_configured*(0=ENAB) 0          0          fec_tts
          0
S:port_persistently_disabled (permanently) 0 (0)
S:
S:      cfg property
S:=====
S:priv_pcfg_bm  0x00000000          lgcl_pcfg_bm
0xbb82e3c4
S:fport_buffer  0x00000000
S:
S:
S:C4 Discard Cntrs: rxlp_stats = 0xb6ab6530
S:-----
-----
S:disc_mcast_wka 0x0          disc_inv_did   0x0
S:disc_cl1_cl4   0x0          disc_sid_chk_fail 0x0
S:disc_inv_dom_egid_txpt 0x0          0x0          disc_vft_hop_cnt_1
          0x0
S:disc_classf    0x0          0x0          disc_fcp_cdb_inv  0x0
S:disc_vfid_trap_enabled 0x0          0x0
disc_vfid_hdr_chk_fail 0x0
S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err 0x0
S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err 0x0
S:disc_ftb_vm_mode 0x0          disc_ftb_agnt2_miss 0x0
S:disc_ecb_de_pad_err 0x0          disc_ecb_de_tag_err  0x0
S:disc_ecb_de_seq_err 0x0          disc_ecb_err         0x0
S:disc_ftb_type4_match 0x0          disc_fcp_rsp_ftb_type4 0x0
S:disc_fcp_rsp_ftb_type4 0x0          0x0          disc_ftb_type5_match
          0x0
S:disc_ftb_type3_match 0x0          disc_els_ftb_type3   0x0
S:disc_ftb_type1_match 0x0          disc_els_rsp_ex_port 0x0
S:disc_inv_drp_dps  0x0          disc_did_lookup_miss 0x0
S:disc_ftb_type2_match 0x0          disc_trpd_plogi_pdisc 0x0
S:disc_type2_lookup_miss 0x0          0x0          disc_ftb_type6_match
          0x0
S:disc_els_rep_ex_port 0x0          0x0          disc_els_sid_lkup_bit1 0x0
S:disc_els_sid_lkup_bit0 0x0          0x0
disc_bls_frm_trap_bit1 0x0
S:disc_ftb_token_err 0x0          disc_asic_internal_err 0x0
S:disc_hard_zone_miss 0x0          disc_lun_zone_miss   0x0

```



```

S:disc_flt_frame_disc  0x0          disc_flt_parity_err  0x0
S:disc_frame_marked_du 0x0          disc_frame_marked_to 0x0
E:Connection type: FE
E:Port type: E_port
E:Trunk port: No
E:Configured Speed: AUTO_SPEED_NEGO
E:Max Capable Speed: 32G
E:Current SNSM Speed: UNDEFINED
E:Hardware TX Speed: 32G (0x00000004)
E:Hardware RX Speed: 32G (0x00000040)
E:
E:Interrupts: 0          Link_failure: 0
Loss_of_sync: 0          Loss_of_sig: 0
E:Lli: 0                Invalid_word: 0
E:trapped_frm: 0          fwd_status_ok: 0
E:fwd_timeout: 0          fwd_tx_unavail: 0
E:fwd_unroutable: 0      fwd_zone_out: 0
E:fwd_other_err: 0        frm_err_discard: 0
E:Fltr listA: 0          Fltr listB: 0
E:Zone trap fwd: 0        Zone trap disc: 0
E:shim_csum: 0           RTE_perr: 0
E:Invalid_crc: 0          Delim_err: 0
E:Protocol_err: 0
E:Lr_in: 0                Lr_out: 0
E:Ols_in: 0               Ols_out: 0

```

filterportshow 58

FILTER DATA

Shadow settings:

```

Filter Enable: 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000

```

Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass: 0x00000000

Real settings:

Enable RAM: 0x00000000, 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass RAM: 0x00000000

Shadowed filters:

Filter 0: Not Installed (MIRROR1)(LISTA)

c4_fldenable[0] = 0x00000000 0x00000000 0x00000000
0x00000000

c4_fldnegate[0] = 0x00000000, c4_fltr_config[0] = 0x00000000

Filter 1: Not Installed (MIRROR2)(LISTA)
c4_fldenable[1] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[1] = 0x00000000,c4_fltr_config[1] = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
c4_fldenable[2] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[2] = 0x00000000,c4_fltr_config[2] = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
c4_fldenable[3] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[3] = 0x00000000,c4_fltr_config[3] = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
c4_fldenable[4] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[4] = 0x00000000,c4_fltr_config[4] = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
c4_fldenable[5] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[5] = 0x00000000,c4_fltr_config[5] = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
c4_fldenable[6] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[6] = 0x00000000,c4_fltr_config[6] = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
c4_fldenable[7] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[7] = 0x00000000,c4_fltr_config[7] = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
c4_fldenable[8] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[8] = 0x00000000,c4_fltr_config[8] = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
c4_fldenable[9] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[9] = 0x00000000,c4_fltr_config[9] = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
c4_fldenable[10] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[10] = 0x00000000,c4_fltr_config[10] =
0x00000000
Filter 11: Not Installed (SIM)(LISTA)
c4_fldenable[11] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[11] = 0x00000000,c4_fltr_config[11] =
0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
c4_fldenable[12] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[12] = 0x00000000,c4_fltr_config[12] =
0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
c4_fldenable[13] = 0x00000000 0x00000000 0x00000000
0x00000000

```
    c4_fldnegate[13] = 0x00000000,c4_fltr_config[13] =
0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
    c4_fldenable[14] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[14] = 0x00000000,c4_fltr_config[14] =
0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
    c4_fldenable[15] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[15] = 0x00000000,c4_fltr_config[15] =
0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
    c4_fldenable[16] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[16] = 0x00000000,c4_fltr_config[16] =
0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
    c4_fldenable[17] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[17] = 0x00000000,c4_fltr_config[17] =
0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
    c4_fldenable[18] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[18] = 0x00000000,c4_fltr_config[18] =
0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
    c4_fldenable[19] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[19] = 0x00000000,c4_fltr_config[19] =
0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
    c4_fldenable[20] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[20] = 0x00000000,c4_fltr_config[20] =
0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
    c4_fldenable[21] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[21] = 0x00000000,c4_fltr_config[21] =
0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
    c4_fldenable[22] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[22] = 0x00000000,c4_fltr_config[22] =
0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
    c4_fldenable[23] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[23] = 0x00000000,c4_fltr_config[23] =
0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
    c4_fldenable[24] = 0x00000000 0x00000000 0x00000000
```

```
0x00000000
    c4_fldnegate[24] = 0x00000000,c4_fltr_config[24] =
0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
    c4_fldenable[25] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[25] = 0x00000000,c4_fltr_config[25] =
0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
    c4_fldenable[26] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[26] = 0x00000000,c4_fltr_config[26] =
0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
    c4_fldenable[27] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[27] = 0x00000000,c4_fltr_config[27] =
0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
    c4_fldenable[28] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[28] = 0x00000000,c4_fltr_config[28] =
0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
    c4_fldenable[29] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[29] = 0x00000000,c4_fltr_config[29] =
0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    c4_fldenable[30] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[30] = 0x00000000,c4_fltr_config[30] =
0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    c4_fldenable[31] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[31] = 0x00000000,c4_fltr_config[31] =
0x00000000
```

Real filters:

```
Filter 0: Not Installed (MIRROR1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
```

Filter 3: Not Installed (MIRROR4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 5: Not Installed (ZONING TRAP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 7: Not Installed (TIN TRAP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 8: Not Installed (FICON CUP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 9: Not Installed (FICON CUP DST)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 11: Not Installed (SIM)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 12: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 13: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 14: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 15: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 16: Not Installed (PERF1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,

0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 30: Not Installed (IPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter dirty indicator: 0x00000000
Performance filters: 0
Port Mirror filters: 0 (0x0)

FIELD DATA

Shadowed fields:

fldoffset[0] = 0x00, fldmask[0] = 0x00, fldvalue_dyna[0]: 0x00 0x00
0x00 0x00
fldcontrol[0].inuse = 0x0 fldcontrol[0].refcnt = 0x00 0x00 0x00
0x00
fldoffset[1] = 0x00, fldmask[1] = 0x00, fldvalue_dyna[1]: 0x00 0x00
0x00 0x00
fldcontrol[1].inuse = 0x0 fldcontrol[1].refcnt = 0x00 0x00 0x00
0x00
fldoffset[2] = 0x00, fldmask[2] = 0x00, fldvalue_dyna[2]: 0x00 0x00
0x00 0x00
fldcontrol[2].inuse = 0x0 fldcontrol[2].refcnt = 0x00 0x00 0x00
0x00
fldoffset[3] = 0x00, fldmask[3] = 0x00, fldvalue_dyna[3]: 0x00 0x00
0x00 0x00
fldcontrol[3].inuse = 0x0 fldcontrol[3].refcnt = 0x00 0x00 0x00
0x00
fldoffset[4] = 0x00, fldmask[4] = 0x00, fldvalue_dyna[4]: 0x00 0x00
0x00 0x00
fldcontrol[4].inuse = 0x0 fldcontrol[4].refcnt = 0x00 0x00 0x00
0x00
fldoffset[5] = 0x00, fldmask[5] = 0x00, fldvalue_dyna[5]: 0x00 0x00
0x00 0x00
fldcontrol[5].inuse = 0x0 fldcontrol[5].refcnt = 0x00 0x00 0x00
0x00
fldoffset[6] = 0x00, fldmask[6] = 0x00, fldvalue_dyna[6]: 0x00 0x00
0x00 0x00
fldcontrol[6].inuse = 0x0 fldcontrol[6].refcnt = 0x00 0x00 0x00
0x00
fldoffset[7] = 0x00, fldmask[7] = 0x00, fldvalue_dyna[7]: 0x00 0x00
0x00 0x00
fldcontrol[7].inuse = 0x0 fldcontrol[7].refcnt = 0x00 0x00 0x00
0x00
fldoffset[8] = 0x00, fldmask[8] = 0x00, fldvalue_dyna[8]: 0x00 0x00
0x00 0x00
fldcontrol[8].inuse = 0x0 fldcontrol[8].refcnt = 0x00 0x00 0x00


```
0x00
fldoffset[9] = 0x00, fldmask[9] = 0x00, fldvalue_dyna[9]:0x00 0x00
0x00 0x00
fldcontrol[9].inuse = 0x0 fldcontrol[9].refcnt = 0x00 0x00 0x00
0x00
fldoffset[10] = 0x00, fldmask[10] = 0x00, fldvalue_dyna[10]:0x00 0x00
0x00 0x00
fldcontrol[10].inuse = 0x0 fldcontrol[10].refcnt = 0x00 0x00 0x00
0x00
fldoffset[11] = 0x00, fldmask[11] = 0x00, fldvalue_dyna[11]:0x00 0x00
0x00 0x00
fldcontrol[11].inuse = 0x0 fldcontrol[11].refcnt = 0x00 0x00 0x00
0x00
fldoffset[12] = 0x00, fldmask[12] = 0x00, fldvalue_dyna[12]:0x00 0x00
0x00 0x00
fldcontrol[12].inuse = 0x0 fldcontrol[12].refcnt = 0x00 0x00 0x00
0x00
fldoffset[13] = 0x00, fldmask[13] = 0x00, fldvalue_dyna[13]:0x00 0x00
0x00 0x00
fldcontrol[13].inuse = 0x0 fldcontrol[13].refcnt = 0x00 0x00 0x00
0x00
fldoffset[14] = 0x00, fldmask[14] = 0x00, fldvalue_dyna[14]:0x00 0x00
0x00 0x00
fldcontrol[14].inuse = 0x0 fldcontrol[14].refcnt = 0x00 0x00 0x00
0x00
fldoffset[15] = 0x00, fldmask[15] = 0x00, fldvalue_dyna[15]:0x00 0x00
0x00 0x00
fldcontrol[15].inuse = 0x0 fldcontrol[15].refcnt = 0x00 0x00 0x00
0x00
fldoffset[16] = 0x00, fldmask[16] = 0x00, fldvalue_dyna[16]:0x00 0x00
0x00 0x00
fldcontrol[16].inuse = 0x0 fldcontrol[16].refcnt = 0x00 0x00 0x00
0x00
fldoffset[17] = 0x00, fldmask[17] = 0x00, fldvalue_dyna[17]:0x00 0x00
0x00 0x00
fldcontrol[17].inuse = 0x0 fldcontrol[17].refcnt = 0x00 0x00 0x00
0x00
fldoffset[18] = 0x00, fldmask[18] = 0x00, fldvalue_dyna[18]:0x00 0x00
0x00 0x00
fldcontrol[18].inuse = 0x0 fldcontrol[18].refcnt = 0x00 0x00 0x00
0x00
fldoffset[19] = 0x00, fldmask[19] = 0x00, fldvalue_dyna[19]:0x00 0x00
0x00 0x00
fldcontrol[19].inuse = 0x0 fldcontrol[19].refcnt = 0x00 0x00 0x00
0x00
```

Real fields:

```
fldoffset RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000
fldmask RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000
fld value4 RAM:
0x00000000
```

0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000

Field dirty indicator: 0x00000000

FDB reference count fdb: 0 [0 0 0 0]
FDB reference count fdb: 1 [0 0 0 0]
FDB reference count fdb: 2 [0 0 0 0]
FDB reference count fdb: 3 [0 0 0 0]
FDB reference count fdb: 4 [0 0 0 0]
FDB reference count fdb: 5 [0 0 0 0]
FDB reference count fdb: 6 [0 0 0 0]
FDB reference count fdb: 7 [0 0 0 0]
FDB reference count fdb: 8 [0 0 0 0]
FDB reference count fdb: 9 [0 0 0 0]
FDB reference count fdb: 10 [0 0 0 0]
FDB reference count fdb: 11 [0 0 0 0]
FDB reference count fdb: 12 [0 0 0 0]
FDB reference count fdb: 13 [0 0 0 0]
FDB reference count fdb: 14 [0 0 0 0]
FDB reference count fdb: 15 [0 0 0 0]
FDB reference count fdb: 16 [0 0 0 0]
FDB reference count fdb: 17 [0 0 0 0]
FDB reference count fdb: 18 [0 0 0 0]
FDB reference count fdb: 19 [0 0 0 0]

Filter counters:

Filter counter 0: 0 (MIRROR1)
Filter counter 1: 0 (MIRROR2)
Filter counter 2: 0 (MIRROR3)
Filter counter 3: 0 (MIRROR4)
Filter counter 4: 0 (AEPORT_NON_MIRR_DROP)
Filter counter 5: 0 (ZONING TRAP)
Filter counter 6: 0 (FCR_EXPORT_DC)
Filter counter 7: 0 (TIN TRAP)
Filter counter 8: 0 (FICON CUP)
Filter counter 9: 0 (FICON CUP DST)
Filter counter 10: 0 (WELL KNOWN ADDR)

Filter counter 11: 0 (SIM)
Filter counter 12: 0 (UNUSED)
Filter counter 13: 0 (UNUSED)
Filter counter 14: 0 (UNUSED)
Filter counter 15: 0 (UNUSED)
Filter counter 16: 0 (PERF1)
Filter counter 17: 0 (PERF2)
Filter counter 18: 0 (PERF3)
Filter counter 19: 0 (PERF4)
Filter counter 20: 0 (PERF5)
Filter counter 21: 0 (PERF6)
Filter counter 22: 0 (PERF7)
Filter counter 23: 0 (PERF8)
Filter counter 24: 0 (PERF9)
Filter counter 25: 0 (PERF10)
Filter counter 26: 0 (PERF11)
Filter counter 27: 0 (PERF12)
Filter counter 28: 0 (OPM1)
Filter counter 29: 0 (OPM2)
Filter counter 30: 0 (IPM1)
Filter counter 31: 0 (IPM2)

ACL DATA

Logical port 3: Hard Zoning disabled, Soft Zoning disabled
Zone type: WWN Zoning
Frames with hard zone miss: 0

*** Please use filterportshow on user port 56 to display ACL hash tables and Mirroring resources of thischip.
***We show this data only for the first physical port which is an external port.

portFcPortCmdShow --slot 0 59 3
doing portFcPortCmdShow: arg1 = 3, arg2 = -2

portshow 59
portDisableReason: None
portCFlags: 0x0
portFlags: 0x4021 PRESENT U_PORT DISABLED LED
LocalSwcFlags: 0x0
portType: 26.0
POD Port: Need license to enable the port
portState: 2 Offline
Protocol: FC
portPhys: 2 No_Module portScn: 2 Offline
port generation number: 0
state transition count: 0

portId: 013b00
portIfId: 43020001
portWwn: 20:3b:d8:1f:cc:2c:99:90
portWwn of device(s) connected:
16b Area list:

Distance: normal
portSpeed: N32Gbps

FEC: Inactive
Credit Recovery: Inactive
LE domain: 0
Peer beacon: Off
FC Fastwrite: OFF

| | | | | |
|-------------|---|---------------|---|-------|
| Interrupts: | 0 | Link_failure: | 0 | Frjt: |
| 0 | | | | |
| Unknown: | 0 | Loss_of_sync: | 0 | Fbsy: |
| 0 | | | | |
| Lli: | 0 | Loss_of_sig: | 0 | |
| Proc_rqrd: | 0 | Protocol_err: | 0 | |
| Timed_out: | 0 | Invalid_word: | 0 | |
| Tx_unavail: | 0 | Invalid_crc: | 0 | |
| Delim_err: | 0 | Address_err: | 0 | |
| Lr_in: | 0 | Ols_in: | 0 | |
| Lr_out: | 0 | Ols_out: | 0 | |

portloginshow 59

| Type | PID | World Wide Name | credit | df_sz | cos |
|-------|-----|-----------------|--------|-------|-----|
| ===== | | | | | |

portloginshow 59 -history

| Type | PID | World Wide Name | logout | time |
|-------|-----|-----------------|--------|------|
| ===== | | | | |

portregshow 59

LED registers

| | | | |
|-------------|---------------|----------|-------------|
| 0x81c0a000: | c4_led_status | 00000000 | 0x81c0a004: |
| | c4_led_ctl | 00000000 | |

FPL registers

| | | | |
|-------------|-------------------------|----------|-------------|
| 0x81c08200: | fpl_port_config | 23490000 | |
| 0x81c0820c: | fpl_port_id_ctl | 00000000 | 0x81c08210: |
| | fpl_port_id_addr | 00013b00 | |
| 0x81c08214: | fpl_port_speed | 00000004 | 0x81c0821c: |
| | fpl_lli_ctl | 00000903 | |
| 0x81c08228: | fpl_lli_os_ctl | bc95b5b5 | 0x81c0822c: |
| | fpl_lli_send_word | bc95b5b5 | |
| 0x81c08230: | fpl_lli_mark_rx | 00000000 | 0x81c08234: |
| | fpl_lli_rnd_trip_time | 00000000 | |
| 0x81c08238: | fpl_lli_ns_status | 00070007 | 0x81c0823c: |
| | fpl_lli_intr_status | 80070007 | |
| 0x81c08244: | fpl_lli_def | 00000000 | 0x81c08254: |
| | fpl_lli_intr_enable_clr | 00100000 | |
| 0x81c08258: | fpl_err_intr_status | 00000000 | 0x81c08260: |

```

fpl_err_intr_enable_clr 00000000
0x81c08268: fpl_err_first_error 00000000 0x81c0826c:
fpl_speed_neg_ctl 00000000
0x81c08270: fpl_speed_neg_stat 00000000 0x81c08274:
fpl_softasn_ctl 0000000f
0x81c08278: fpl_link_init_ctl 00000000 0x81c0827c:
fpl_link_init_stat 00000000
0x81c08280: fpl_aec_ctl 00051060 0x81c08284:
fpl_aec_ctl2 04009f60
0x81c08288: fpl_pcs_ctl 00000160 0x81c0828c:
fpl_fec_ctl 00000441
0x81c08290: fpl_fec_cor 00000000 0x81c08294:
fpl_fec_uncor 00000000
0x81c08298: fpl_hss_link_ctl 0031f040 0x81c0829c:
fpl_afifo_link_ctl 00000a86
0x81c082a0: fpl_echo_lb_ctl 0000028c 0x81c082a4:
fpl_scratch 00000121
0x81c082a8: fpl_debug 00030005 0x81c082ac:
fpl_misc_debug 00001800
0x00000000: SW_shadow_reg 00000000 0x00000000:
SW_c4_phyp->cfgptr 00030000

```

per-fpg (per octet) registers

=====

```

0x8180382c: fpg_serdes_ctla0 81a37be7 0x81803830:
fpg_serdes_ctla1 81a37be7
0x81803834: fpg_serdes_ctlb0 81a1c3c3 0x81803838:
fpg_serdes_ctlb1 81a1c3c3
0x8180383c: fpg_serdes_xgmii_1ms 00067c28 0x81803840:
fpg_serdes_regtimctl 40e47946
0x81803844: fpg_serdes_asnrsttimctl 00000102

```

HSS PLL registers

=====

```

0x81801400: 00_hssplla_vco_coarse_cal0 00000000 0x81801404:
01_hssplla_vco_coarse_cal1 00000014
0x81801408: 02_hssplla_vco_coarse_cal2 00000000 0x8180140c:
03_hssplla_vco_coarse_cal3 00000000
0x81801410: 04_hssplla_vco_coarse_cal4 00000000 0x81801424:
09_hssplla_power_ctl 00000000
0x81801428: 0A_hssplla_charge_pump_ctl 00000004 0x81801438:
0E_hssplla_pll_misc_ctl 00000000
0x8180143c: 0F_hssplla_pclk_ctl 000000f8 0x81801440:
10_hssplla_eyem_intv_ctl 00000000
0x81801444: 11_hssplla_eyem_intv_lim1 00000000 0x81801448:
12_hssplla_eyem_intv_lim2 00000000
0x8180144c: 13_hssplla_eyem_intv_lim3 00000000 0x81801450:
14_hssplla_eyem_intv_lim4 00000000
0x818014f0: 3C_hssplla_macro_tst_ctl4 00000000 0x818014f4:
3D_hssplla_macro_tst_ctl3 00000000
0x818014f8: 3E_hssplla_macro_tst_ctl2 00000000 0x818014fc:
3F_hssplla_macro_tst_ctl1 00000000
0x81801500: 00_hssppll_vco_coarse_cal0 0000000a 0x81801504:
01_hssppll_vco_coarse_cal1 00000014

```

| | | |
|---|----------|-------------|
| 0x81801508: 02_hsspll_b_vco_coarse_cal2 | 00000000 | 0x8180150c: |
| 03_hsspll_b_vco_coarse_cal3 | 00000000 | |
| 0x81801510: 04_hsspll_b_vco_coarse_cal4 | 00000000 | 0x81801524: |
| 09_hsspll_b_power_ctl | 00000000 | |
| 0x81801528: 0A_hsspll_b_charge_pump_ctl | 00000004 | 0x81801538: |
| 0E_hsspll_b_pll_misc_ctl | 00000000 | |
| 0x8180153c: 0F_hsspll_b_pclk_ctl | 000000f8 | 0x81801540: |
| 10_hsspll_b_eyem_intv_ctl | 00000000 | |
| 0x81801544: 11_hsspll_b_eyem_intv_lim1 | 00000000 | 0x81801548: |
| 12_hsspll_b_eyem_intv_lim2 | 00000000 | |
| 0x8180154c: 13_hsspll_b_eyem_intv_lim3 | 00000000 | 0x81801550: |
| 14_hsspll_b_eyem_intv_lim4 | 00000000 | |
| 0x818015f0: 3C_hsspll_b_macro_tst_ctl4 | 00000000 | 0x818015f4: |
| 3D_hsspll_b_macro_tst_ctl3 | 00000000 | |
| 0x818015f8: 3E_hsspll_b_macro_tst_ctl2 | 00000000 | 0x818015fc: |
| 3F_hsspll_b_macro_tst_ctl1 | 00000000 | |

HSS TX registers

=====

| | | |
|--|----------|-------------|
| 0x81800100: 00_hsstx_cfg_mode_PHY | 00009f48 | 0x81800104: |
| 01_hsstx_test_ctl | 00000000 | |
| 0x81800108: 02_hsstx_coeff_ctl_INV | 00000000 | 0x8180010c: |
| 03_hsstx_drv_mode_ctl | 00000000 | |
| 0x81800110: 04_hsstx_drv_ovrd_ctl | 00000010 | 0x81800114: |
| 05_hsstx_dclk_align_ovrd | 00000080 | |
| 0x81800118: 06_hsstx_imp_cal_ovrd | 00000c0c | 0x8180011c: |
| 07_hsstx_dclk_drift_tol | 00000004 | |
| 0x81800120: 08_hsstx_tap0_coeff_TUNE | 00000000 | 0x81800124: |
| 09_hsstx_tap1_coeff_TUNE | 00000003 | |
| 0x81800128: 0A_hsstx_tap2_coeff_TUNE | 00000018 | 0x8180012c: |
| 0B_hsstx_tap3_coeff_TUNE | 0000000d | |
| 0x81800134: 0D_hsstx_pol_INV | 00000004 | 0x81800138: |
| 0E_hsstx_ae_cmd | 00000000 | |
| 0x8180013c: 0F_hsstx_ae_stat | 00000000 | 0x81800140: |
| 10_hsstx_ae_tap0_TUNE | 00000000 | |
| 0x81800144: 11_hsstx_ae_tap1_TUNE | 00000000 | 0x81800148: |
| 12_hsstx_ae_tap2_TUNE | 00000028 | |
| 0x8180014c: 13_hsstx_ae_tap3_TUNE | 00000000 | 0x81800154: |
| 15_hsstx_app_tune | 0000120e | |
| 0x81800158: 16_hsstx_analog_diag | 00000000 | 0x81800160: |
| 18_hsstx_4x_seg_app | 0000aafa | |
| 0x81800164: 19_hsstx_2x_seg_app | 00000000 | 0x81800168: |
| 1A_hsstx_1x_seg_app | 0000ff5d | |
| 0x8180016c: 1B_hsstx_seg_4x_term_app | 00000000 | 0x81800170: |
| 1C_hsstx_seg_2x1x_term_app | 00000f00 | |
| 0x81800174: 1D_hsstx_tap_sign_app | 00000004 | 0x81800178: |
| 1E_hsstx_ext_addr_data | 00000001 | |
| 0x8180017c: 1F_hsstx_ext_addr_addr | 00000000 | 0x81800180: |
| 20_hsstx_pat_buf_bytes_1_0 | 00000000 | |
| 0x81800184: 21_hsstx_pat_buf_bytes_3_2 | 00000000 | 0x81800188: |
| 22_hsstx_pat_buf_bytes_5_4 | 00000000 | |
| 0x8180018c: 23_hsstx_pat_buf_bytes_7_6 | 00000000 | 0x8180019c: |
| 27_hsstx_8023az_ctl | 00000000 | |
| 0x818001a0: 28_hsstx_dcc_ctl | 000060c0 | 0x818001a4: |

| | | | |
|---|----------|----------|-------------|
| 29_hsstx_dcc_ovrd | 00001000 | | |
| 0x818001a8: 2A_hsstx_dcc_app | | 0000008a | 0x818001ac: |
| 2B_hsstx_dcc_timeout | 0000ffff | | |
| 0x818001c0: 30_hsstx_tap_sign_ovrd | | 00000000 | 0x818001c8: |
| 32_hsstx_seg_4x_ovrd | 00000000 | | |
| 0x818001cc: 33_hsstx_seg_2x_ovrd | | 00000000 | 0x818001d0: |
| 34_hsstx_seg_1x_ovrd | 00000000 | | |
| 0x818001d8: 36_hsstx_tap_seg_4x_term_ovrd | | 00000000 | 0x818001dc: |
| 37_hsstx_tap_seg_2x_term_ovrd | 00000000 | | |
| 0x818001e0: 38_hsstx_tap_seg_1x_term_ovrd | | 00000000 | 0x818001ec: |
| 3B_hsstx_mac_test_ctl5 | 00000000 | | |
| 0x818001f0: 3C_hsstx_mac_test_ctl4 | | 00000000 | 0x818001f4: |
| 3D_hsstx_mac_test_ctl3 | 00000000 | | |
| 0x818001f8: 3E_hsstx_mac_test_ctl2 | | 00000000 | 0x818001fc: |
| 3F_hsstx_mac_test_ctl1 | 000000c6 | | |

HSS RX registers

=====

| | | | |
|---|----------|----------|-------------|
| 0x81800300: 00_hssrx_cfg_mode_PHY | | 00009e78 | 0x81800304: |
| 01_hssrx_test_ctl | 00000000 | | |
| 0x81800308: 02_hssrx_phs_rot_ctl | | 0000cb80 | 0x8180030c: |
| 03_hssrx_phs_rot_ofs_ctl | 00000610 | | |
| 0x81800310: 04_hssrx_phs_rot_posn1 | | 00001614 | 0x81800314: |
| 05_hssrx_phs_rot_posn2 | 00000006 | | |
| 0x81800318: 06_hssrx_phs_rot_sta_ofs1 | | 00000000 | 0x8180031c: |
| 07_hssrx_phs_rot_sta_ofs2 | 0000001e | | |
| 0x81800320: 08_hssrx_dfe_ctl_PHY | | 00002002 | 0x81800324: |
| 09_hssrx_dfe_smpl_snap1 | 00000000 | | |
| 0x81800328: 0A_hssrx_dfe_smpl_snap2 | | 00008000 | 0x8180032c: |
| 0B_hssrx_vga_ctl1 | 00004001 | | |
| 0x81800330: 0C_hssrx_vga_ctl2 | | 00007aa0 | 0x81800334: |
| 0D_hssrx_vga_ctl3 | 000009e4 | | |
| 0x81800338: 0E_hssrx_pwr_mgmt_ctl | | 0000001f | 0x8180033c: |
| 0F_hssrx_iqamp_ctl1 | 0000001a | | |
| 0x81800340: 10_hssrx_iqamp_ctl2 | | 00000006 | 0x81800344: |
| 11_hssrx_dacap_dacan_sel | 00000003 | | |
| 0x81800348: 12_hssrx_dacap_dacan | | 0000ffff | 0x8180034c: |
| 13_hssrx_daca_min | 00000000 | | |
| 0x81800350: 14_hssrx_adac_ctl | | 000000ff | 0x81800354: |
| 15_hssrx_ac_cp_ctl | 000031c3 | | |
| 0x81800358: 16_hssrx_ac_cp_val | | 00000051 | 0x8180035c: |
| 17_hssrx_dfe_h1h2h3_lcl_off_ch | 00000014 | | |
| 0x81800360: 18_hssrx_dfe_h1h2h3_lcl_off_val | | 00000000 | 0x81800364: |
| 19_hssrx_peaked_intg | 000000ff | | |
| 0x81800368: 1A_hssrx_cdr_analog_sw | | 0000ce00 | 0x8180036c: |
| 1B_hssrx_peaking_amp_init_c_PHY | 00000000 | | |
| 0x81800370: 1C_hssrx_dac_dpc | | 00000040 | 0x81800374: |
| 1D_hssrx_ddc | 00000000 | | |
| 0x81800378: 1E_hssrx_int_stat_PHY | | 00000c0f | 0x8180037c: |
| 1F_hssrx_dfe_func_ctl1_PHY | 0000ffff | | |
| 0x81800380: 20_hssrx_dfe_func_ctl2_INV | | 00007eff | 0x81800384: |
| 21_hssrx_ofs_ch_dcc_qcc_idx | 00002000 | | |
| 0x81800388: 22_hssrx_dfe_ofs_val | | 00000706 | 0x8180038c: |
| 23_hssrx_h_coeff_bist | 0000040b | | |

| | | |
|--|----------------|-------------|
| 0x81800390: 24_hssrx_ac_cap_bist | 0000002f | 0x81800394: |
| 25_hssrx_max_gain_path_idx_res | 00007800 | |
| 0x81800398: 26_hssrx_loff_ctl | 00000054 | 0x8180039c: |
| 27_hssrx_sigdet_ctl | 00002f80 | |
| 0x818003a0: 28_hssrx_ana_ctl_sw | 00000000 | 0x818003a4: |
| 29_hssrx_intg_dac_ofs | 0000dfde | |
| 0x818003a8: 2A_hssrx_eye_ctl | 00000000 | 0x818003ac: |
| 2B_hssrx_eye_met | 00000004 | |
| 0x818003b0: 2C_hssrx_eye_met_err_cnt | 00000000 | 0x818003b4: |
| 2D_hssrx_eye_met_pdf_eyec | 00000000 | |
| 0x818003b8: 2E_hssrx_eye_met_pat_len | 0000007f | 0x818003bc: |
| 2F_hssrx_dfe_func_ctl3 | 0000dfff | |
| 0x818003c0: 30_hssrx_dfe_tap_ctl_idx_ptr | 00000008 | 0x818003c4: |
| 31_hssrx_dfe_tap | 00003030 | |
| 0x818003c8: 32_hssrx_lte_ctl_TUNE | 00001601 | 0x818003e4: |
| 39_hssrx_int_stat2 | 000041ff | |
| 0x818003e8: 3A_hssrx_ac_cpl_cur_src_adj | 00000040 | 0x818003ec: |
| 3B_hssrx_dcd_ctl | 00007c50 | |
| 0x818003f0: 3C_hssrx_dcc_ctl | 00000d41 | 0x818003f4: |
| 3D_hssrx_qcc_ctl | 00006947 | |
| 0x818003f8: 3E_hssrx_mac_test_ctl2 | 00000000 | 0x818003fc: |
| 3F_hssrx_mac_test_ctl1 | 00000000 | |
| 0x81800348: 12_hssrx_dacap_dacan[02] | 00fd fffd | |
| 0x81800360: 18_hssrx_dfe_h1h2h3_lcl_off_va[00] | 0000 0000 0000 | |
| 0000 0000 0000 0000 0000 | | |
| 0x81800360: 18_hssrx_dfe_h1h2h3_lcl_off_va[08] | 0000 0000 0000 | |
| 0000 0000 0000 0000 0000 | | |
| 0x81800360: 18_hssrx_dfe_h1h2h3_lcl_off_va[16] | 0000 0000 0000 | |
| 0000 0000 | | |
| 0x81800388: 22_hssrx_dfe_ofs_val[00][00] | 0706 7f00 797f | |
| 0000 0b09 7f7f | | |
| 0x81800388: 22_hssrx_dfe_ofs_val[03][00] | 057f 7f7f 017a | |
| 0000 067d 7f00 | | |
| 0x81800388: 22_hssrx_dfe_ofs_val[06][00] | 037f 7f00 0208 | |
| 7f7f 0401 7e7f | | |
| 0x81800388: 22_hssrx_dfe_ofs_val[09][00] | 7e03 007f 017f | |
| 0000 7f05 0000 | | |
| 0x81800388: 22_hssrx_dfe_ofs_val[12][00] | 7906 0000 0506 | |
| 0000 7902 0000 | | |
| 0x81800388: 22_hssrx_dfe_ofs_val[15][00] | 0105 0000 7f05 | |
| 0000 7a79 0000 | | |
| 0x81800388: 22_hssrx_dfe_ofs_val[18][00] | 7c7f 0000 7f79 | |
| 0000 0004 0000 | | |
| 0x81800388: 22_hssrx_dfe_ofs_val[21][00] | 0004 0000 0004 | |
| 0000 0004 0000 | | |
| 0x81800388: 22_hssrx_dfe_ofs_val[24][00] | 0605 0000 7d01 | |
| 0000 7b7d 0000 | | |
| 0x81800394: 25_hssrx_max_gain_path_idx_res[00] | 005c 084a 1011 | |
| 189f 20cf 289f 3086 3800 | | |
| 0x81800394: 25_hssrx_max_gain_path_idx_res[08] | 409f 487f 506f | |
| 5800 6040 6800 70fa 7800 | | |
| 0x818003c4: 31_hssrx_dfe_tap[00] | fffe 8080 0000 | |
| 0000 0030 0030 3030 3030 | | |
| 0x818003c4: 31_hssrx_dfe_tap[08] | 3030 3030 3030 | |


```

0000
0x818003e8: 3A_hssrx_ac_cpl_cur_src_adj[00]      0040 0040   0040
0040
0x818003ec: 3B_hssrx_dcd_ctl[00]                      7c50 5c00   7c83
5c00   7c81
0x818003f0: 3C_hssrx_dcc_ctl[00]                      0d41 0d00   0d41
0d83
0x818003f4: 3D_hssrx_qcc_ctl[00]                      6947 6947

```

xfipcs, fec, aec, & aet registers

```

=====
0x81c08400: xfipcs_reg      [00] 00002040 00000080 00000000
00000000 00000001 00000008 00000000 00000000
0x81c08420: xfipcs_reg      [08] 00008c01 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c08440: xfipcs_reg      [16] 00000000 00000000 00000000
00000000 00000040 00000000 00000000 00000000
0x81c08460: xfipcs_reg      [24] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c08480: xfipcs_reg      [32] 00000004 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c08620: fec_32g_128g_reg [08] 00000000 00000000 00000000
00000000 00000000 00000000 00000000
0x81c08648: fec_32g_128g_reg [18] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c08a00: aec_reg         [00] 00000000 00000000 00000000
00000000 00000000 00000000 00000000
0x81c08c00: aet_reg         [00] 00000000 00000000 00000000
00000000 00000000

```

bbc registers

```

=====
0x81c09800: bbc_trc      0 0 0 0 0 0 0
0
0x81c09840: bbc_trc      0 0 0 0 0 0 0
0
0x81c09880: bbc_trc      0 0 0 0 0 0 0
0
0x81c098c0: bbc_trc      0 0 0 0 0 0 0
0
0x81c09900: bbc_trc      0 0 0 0 0 0 0
0
0x81c09804: bbc_mbc      0 0 0 0 0 0 0
0
0x81c09844: bbc_mbc      0 0 0 0 0 0 0
0
0x81c09884: bbc_mbc      0 0 0 0 0 0 0
0
0x81c098c4: bbc_mbc      0 0 0 0 0 0 0
0
0x81c09904: bbc_mbc      0 0 0 0 0 0 0
0
0x81c09a00: bbc_rcc      0 0 0 0 0 0 0
0

```

| | | | | | | | |
|-------------------------------------|----------|---|---|---|---|----------------------|---|
| 0x81c09a20: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c09a40: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c09a60: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c09a80: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c09c00: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c09c20: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c09c40: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c09c60: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c09c80: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c09d00: bbc_fbpc | 00000000 | | | | | 0x81c09d04: bbc_csc | |
| 00000000 | | | | | | | |
| 0x81c09d08: bbc_rcc_inc | 00000000 | | | | | 0x81c09d0c: | |
| bbc_rqc_inc | 00000000 | | | | | | |
| 0x81c09d10: bbc_fbpc_inc | 00000000 | | | | | 0x81c09d14: | |
| bbc_tmc_inc | 00000000 | | | | | | |
| 0x81c09d18: bbc_threshold | 00080100 | | | | | 0x81c09d1c: | |
| bbc_counter_clr | 00000000 | | | | | | |
| 0x81c09d20: bbc_debug_en | 00000000 | | | | | 0x81c09d24: bbc_ctrl | |
| 00200020 | | | | | | | |
| 0x81c09d28: bbc_rqc_rcc_thresh | 00000055 | | | | | 0x81c09d34: | |
| bbc_bb_sc_n | 00000000 | | | | | | |
| 0x81c09d38: bbc_crd_reco_debug | 00000000 | | | | | 0x81c09d3c: | |
| bbc_crd_reco_debug_data | 00000000 | | | | | | |
| 0x81c09d40: bbc_multi_frm_loss_cnt | 00000000 | | | | | 0x81c09d44: | |
| bbc_multi_rdy_loss_cnt | 00000000 | | | | | | |
| 0x81c09d48: bbc_1frm_loss_recov_cnt | 00000000 | | | | | 0x81c09d4c: | |
| bbc_1rdy_loss_recov_cnt | 00000000 | | | | | | |
| 0x81c09d58: bbc_int_status | 00000000 | | | | | 0x81c09d5c: | |
| bbc_int_set | 00000000 | | | | | | |
| 0x81c09d60: bbc_int_first | 00000000 | | | | | 0x81c09d64: | |
| bbc_frm_rdy_rx_err_addr | 00000000 | | | | | | |
| 0x81c09d68: bbc_frm_rdy_tx_err_addr | 00000000 | | | | | 0x81c09d6c: | |
| bbc_trc_mbc_err_addr | 00000000 | | | | | | |
| 0x81c09d70: bbc_frm_rdy_rx_dbl_ecc | 00000000 | | | | | 0x81c09d74: | |
| bbc_frm_rdy_tx_dbl_ecc | 00000000 | | | | | | |
| 0x81c09d78: bbc_trc_mbc_dbl_ecc | 00000000 | | | | | | |
| 0x81c09d7c: bbc_fsm_status | 00001011 | | | | | 0x81c09d80: | |
| bbc_force_err | 00000000 | | | | | | |
| 0x81c09d84: bbc_crdt_avail0 | ffffffff | | | | | 0x81c09d88: | |
| bbc_crdt_avail1 | 000000ff | | | | | | |
| 0x81c09d8c: bbc_scratch | 00000000 | | | | | | |

FPS registers

=====

| | | | | | | | |
|---------------------------|----------|--|--|--|--|-------------|--|
| 0x81c08004: fps_er_enc_in | 00000000 | | | | | 0x81c08008: | |
|---------------------------|----------|--|--|--|--|-------------|--|

```

fps_er_crc          00000000
0x81c0800c: fps_er_trunc      00000000      0x81c08010:
fps_er_toolong     00000000
0x81c08014: fps_er_bad_eof    00000000      0x81c08018:
fps_er_enc_out     00000000
0x81c0801c: fps_er_bad_os     00000000      0x81c08020:
fps_er_flush       00000000
0x81c08024: fps_er_ifg        00000000      0x81c08038:
fps_er_crc_good_eof 00000000
0x81c0803c: fps_inv_arb       00000000      0x81c08040:
fps_slow_sts_status 00000000
0x81c08044: fps_tx_frm_cnt     00000000      0x81c08048:
fps_rx_frm_cnt     00000000
0x81c08050: fps_tx_word_cnt_hi 00000000      0x81c0804c:
fps_tx_word_cnt_lo 00000000
0x81c08058: fps_rx_word_cnt_hi 00000000      0x81c08054:
fps_rx_word_cnt_lo 00000000

```

BAL registers

=====

```

0x81c0f000: bal_desired_buf      00000000      0x81c0f004:
bal_alloc_buf      00000000
0x81c0f008: bal_busy_buf              00000000      0x81c0f00c:
bal_usable_buf     00000000
0x81c0f010: bal_max_bor_buf          00000000
0x81c0f014: bal_busy_buf_thresh     00000002

```

TXQ registers

=====

```

0x81c0b004: txq_phys_port_ctl      00410000
0x81c0b050: txq_link_skew           00000000
0x81c0b068: txq_cr_lk_dttm_intr_sts [00] 00000000 00000000
0x81c0b070: txq_cr_lk_dttm_intr_en [00] 00000000 00000000
0x81c0b024: txq_disc_frm_trap_cnt   00000014

```

FDS registers

=====

```

0x81c0c000: fds_rxf_ctl              00000002      0x81c0c004:
fds_rxf_wait_thresh 00000909
0x81c0c018: fds_rxf_first_error      00000000      0x81c0c01c:
fds_rxf_first_error_info 00000000
0x81c0c020: fds_rxf_inout_pkt_cnt    00000000
0x81c0c008: fds_rxf_err_int_status   00000000      0x81c0c024:
fds_rxf_fifo_status  00888888
0x81c0d000: fds_txf_ctl              0000003a      0x81c0d004:
fds_txf_wait_ifg_thresh 00a00106
0x81c0d008: fds_txf_err_int_status   00000000      0x81c0d024:
fds_txf_fifo_status  00088888
0x81c0d02c: fds_txf_bbc_scs         00000000

```

Logical TXQ registers

=====

```

0x81c0b000: txq_log_port_ctl        00000002      0x81c0b008:
txq_port_status     00000000

```

```

0x81c0b00c: txq_todo_flags [00] 00000000 00000000
0x81c0b014: txq_spd_match_desc [00] 00000000 00000000 00000000
00000000
0x81c0b024: txq_spd_match_desc [04] 00000014
0x81c0b028: txq_vc_weight [00] 01010101 01010101 01010101
01010101
0x81c0b038: txq_vc_weight [04] 01010101 01010101 01010101
01010101
0x81c0b048: txq_vc_weight [08] 01010101 00010101
0x81c0b054: txq_cong_dttn_ctrl 00000000
0x81c0b058: txq_cong_dttn_intr_sts [00] 00000000 00000000
0x81c0b060: txq_cong_dttn_intr_en [00] 00000000 00000000
0x81c0b078: txq_bw_limit_en_reg [00] 00000000 00000000
0x81c0b080: txq_bw_gua_en_reg [00] 00000000 00000000
0x81c0b088: txq_vc_group [00] 03030300 03030303 03030303
03030303
0x81c0b098: txq_vc_group [04] 03030303 03030303 03030303
03030303
0x81c0b0a8: txq_vc_group [08] 03030303 03030303 00000000
00000000
0x81c0b0b0: txq_bw_thresh_group [00] 00000000 00000000 00000000
00000000
0x81c0b0c0: txq_bw_thresh_group [04] 00000000 00000000 00000000
00000000
0x81c0b0d0: txq_bw_thresh_group [08] 00000000 00000000 00000000
00000000
0x81c0b0e0: txq_bw_thresh_group [12] 00000000 00000000 00000000
00000000
0x81c0b0f0: txq_bw_thresh_group [16] 00000000 00000000 00000000
00000000
0x81c0b100: txq_bw_thresh_group [20] 00000000 00000000 00000000
00000000
0x81c0b110: txq_bw_thresh_group [24] 00000000 00000000 00000000
00000000
0x81c0b120: txq_bw_thresh_group [28] 00000000 00000000 00000000
00000000
0x81c0b130: txq_bw_thresh_group [32] 00000000 00000000 00000000
00000000
0x81c0b140: txq_bw_thresh_group [36] 00000000 00000000 00000000
00000000

```

txq Congestion detection Statistics RAM

```

=====
0x810900a0: vc[0] 00000000 0x810900a4: vc[1]
00000000
0x810900a8: vc[2] 00000000 0x810900ac: vc[3]
00000000
0x810900b0: vc[4] 00000000 0x810900b4: vc[5]
00000000
0x810900b8: vc[6] 00000000 0x810900bc: vc[7]
00000000
0x810900c0: vc[8] 00000000 0x810900c4: vc[9]
00000000
0x810900c8: vc[10] 00000000 0x810900cc: vc[11]

```

```

00000000
0x810900d0: vc[12]      00000000      0x810900d4: vc[13]
00000000
0x810900d8: vc[14]      00000000      0x810900dc: vc[15]
00000000
0x810900e0: vc[16]      00000000      0x810900e4: vc[17]
00000000
0x810900e8: vc[18]      00000000      0x810900ec: vc[19]
00000000
0x810900f0: vc[20]      00000000      0x810900f4: vc[21]
00000000
0x810900f8: vc[22]      00000000      0x810900fc: vc[23]
00000000
0x81090100: vc[24]      00000000      0x81090104: vc[25]
00000000
0x81090108: vc[26]      00000000      0x8109010c: vc[27]
00000000
0x81090110: vc[28]      00000000      0x81090114: vc[29]
00000000
0x81090118: vc[30]      00000000      0x8109011c: vc[31]
00000000
0x81090120: vc[32]      00000000      0x81090124: vc[33]
00000000
0x81090128: vc[34]      00000000      0x8109012c: vc[35]
00000000
0x81090130: vc[36]      00000000      0x81090134: vc[37]
00000000
0x81090138: vc[38]      00000000      0x8109013c: vc[39]
00000000

```

Logical STS registers

=====

```

0x81584144: sts_ftb_type1_miss      00000000
0x81584148: sts_ftb_type2_miss      00000000
0x8158414c: sts_ftb_type6_miss      00000000
0x81584150: sts_hard_zoning_miss    00000000
0x81584154: sts_lun_zoning_miss     00000000
0x8158415c: sts_unroutable          00000000
0x81581174: sts_rte_cl2              00000000      0x81581178:
sts_rte_cl3              00000000      0x8158117c: sts_rte_link_ctl
00000000      0x81584168: sts_tx_timeout      00000000

```

Logical STS filter registers

=====

```

0x815840c0: stsflt_trig      [00] 00000000 00000000 00000000
00000000
0x815840d0: stsflt_trig      [04] 00000000 00000000 00000000
00000000
0x815840e0: stsflt_trig      [08] 00000000 00000000 00000000
00000000
0x815840f0: stsflt_trig      [12] 00000000 00000000 00000000
00000000
0x81584100: stsflt_trig      [16] 00000000 00000000 00000000

```

```

00000000
0x81584110: stsflt_trig [20] 00000000 00000000 00000000
00000000
0x81584120: stsflt_trig [24] 00000000 00000000 00000000
00000000
0x81584130: stsflt_trig [28] 00000000 00000000 00000000
00000000
0x81584140: stsflt_trig [32]

```

Logical STS discard registers

=====

```

0x81581174: disc_mcast_wka 00000000 0x81581178:
disc_inv_did 00000000
0x8158117c: disc_cl1_cl4 00000000 0x81581180:
disc_sid_chk_fail 00000000
0x81581184: disc_inv_dom_egid_txpt 00000000 0x81581188:
disc_vft_hop_cnt_1 00000000
0x8158118c: disc_classf 00000000 0x81581190:
disc_fcp_cdb_inv 00000000
0x81581194: disc_vfid_trap_enabled 00000000 0x81581198:
disc_vfid_hdr_chk_fail 00000000
0x8158119c: disc_shim_cksum_fail 00000000 0x815811a0:
disc_fed_edit_cmd_err 00000000
0x815811a4: disc_ftb_vm_mode 00000000 0x815811a8:
disc_ftb_agnt2_miss 00000000
0x815811ac: disc_ecb_reserved 00000000 0x815811b0:
disc_ecb_de_pad_err 00000000
0x815811b4: disc_ecb_de_tag_err 00000000 0x815811b8:
disc_ecb_de_seq_err 00000000
0x815811bc: disc_ecb_err 00000000 0x815811c0:
disc_ftb_type4_match 00000000
0x815811c4: disc_fcp_rsp_ftb_type4 00000000 0x815811c8:
disc_ftb_type5_match 00000000
0x815811cc: disc_ftb_type3_match 00000000 0x815811d0:
disc_els_ftb_type3 00000000
0x815811d4: disc_ftb_type1_match 00000000 0x815811d8:
disc_els_rsp_ex_port 00000000
0x815811dc: disc_inv_drp_dps 00000000 0x815811e0:
disc_did_lookup_miss 00000000
0x815811e4: disc_ftb_type2_match 00000000 0x815811e8:
disc_trpd_plogi_pdisc 00000000
0x815811ec: disc_type2_lookup_miss 00000000 0x815811f0:
disc_ftb_type6_match 00000000
0x815811f4: disc_els_rep_ex_port 00000000 0x815811f8:
disc_els_sid_lkup_bit1 00000000
0x815811fc: disc_els_sid_lkup_bit0 00000000 0x81581200:
disc_bls_frm_trap_bit1 00000000
0x81581204: disc_ftb_token_err 00000000 0x81581208:
disc_asic_internal_err 00000000
0x8158120c: disc_hard_zone_miss 00000000 0x81581210:
disc_lun_zone_miss 00000000
0x81581214: discflt_frame_disc 00000000 0x81581218:
discflt_parity_err 00000000
0x8158121c: disc_frame_marked_du 00000000 0x81581220:

```

disc_frame_marked_to 00000000
0x81581224: disc_lkup_rte_prty_err 00000000

portstatsshow 59

| | | | | | |
|------------------------------|---|------------|---------|----------|--------------------------|
| stat_wtx | 0 | | | | 4-byte words transmitted |
| stat_wrx | 0 | | | | 4-byte words received |
| stat_ftx | 0 | | | | Frames transmitted |
| stat_frx | 0 | | | | Frames received |
| stat_c2_frx | 0 | | | | Class 2 frames received |
| stat_c3_frx | 0 | | | | Class 3 frames received |
| stat_lc_rx | 0 | | | | Link control frames |
| received | | | | | |
| stat_mc_rx | 0 | | | | Multicast frames |
| received | | | | | |
| stat_mc_to | 0 | | | | Multicast timeouts |
| stat_mc_tx | 0 | | | | Multicast frames |
| transmitted | | | | | |
| tim_txcrd_z | 0 | | | | Time TX Credit Zero |
| (2.5Us ticks) | | | | | |
| tim_txcrd_z_vc 0- 3: | 0 | 0 | 0 | 0 | |
| tim_txcrd_z_vc 4- 7: | 0 | 0 | 0 | 0 | |
| tim_txcrd_z_vc 8-11: | 0 | 0 | 0 | 0 | |
| tim_txcrd_z_vc 12-15: | 0 | 0 | 0 | 0 | |
| lat_tot_pkt_vc 0- 3: | 1 | 1 | 1 | 1 | |
| lat_tot_pkt_vc 4- 7: | 1 | 1 | 1 | 1 | |
| lat_tot_pkt_vc 8-11: | 1 | 1 | 1 | 1 | |
| lat_tot_pkt_vc 12-15: | 1 | 1 | 1 | 1 | |
| lat_hi_time_vc 0- 3: | 0 | 0 | 0 | 0 | |
| lat_hi_time_vc 4- 7: | 0 | 0 | 0 | 0 | |
| lat_hi_time_vc 8-11: | 0 | 0 | 0 | 0 | |
| lat_hi_time_vc 12-15: | 0 | 0 | 0 | 0 | |
| lat_lo_time_vc 0- 3: | 1 | 1 | 1 | 1 | |
| lat_lo_time_vc 4- 7: | 1 | 1 | 1 | 1 | |
| lat_lo_time_vc 8-11: | 1 | 1 | 1 | 1 | |
| lat_lo_time_vc 12-15: | 1 | 1 | 1 | 1 | |
| max_latency_vc 0- 3: | 1 | 1 | 1 | 1 | |
| max_latency_vc 4- 7: | 1 | 1 | 1 | 1 | |
| max_latency_vc 8-11: | 1 | 1 | 1 | 1 | |
| max_latency_vc 12-15: | 1 | 1 | 1 | 1 | |
| latency_dma_ts | | 09-09-2024 | UTC Mon | 08:47:26 | TXQ |
| Latency DMA TimeStamp | | | | | |
| fec_cor_detected | 0 | | | | Count of blocks that |
| were corrected by FEC | | | | | |
| fec_uncor_detected | 0 | | | | Count of blocks that |
| were left uncorrected by FEC | | | | | |
| er_enc_in | 0 | | | | Encoding errors inside |
| of frames | | | | | |
| er_crc | 0 | | | | Frames with CRC errors |
| er_trunc | 0 | | | | Frames shorter than |
| minimum | | | | | |
| er_toolong | 0 | | | | Frames longer than |
| maximum | | | | | |
| er_bad_eof | 0 | | | | Frames with bad end-of- |

| | | | |
|--------------------------|-----------------------------|--|--------------------------|
| frame | | | |
| er_enc_out | 0 | | Encoding error outside |
| of frames | | | |
| er_bad_os | 0 | | Invalid ordered set |
| er_pcs_blk | 0 | | PCS block errors |
| er_rx_c3_timeout | 0 | | Class 3 receive frames |
| discarded due to timeout | | | |
| er_tx_c3_timeout | 0 | | Class 3 transmit frames |
| discarded due to timeout | | | |
| er_unroutable | 0 | | Frames that are |
| unroutable | | | |
| er_unreachable | 0 | | Frame with unreachable |
| destination | | | |
| er_other_discard | 0 | | Other discards |
| er_type1_miss | 0 | | frames with FTB type 1 |
| miss | | | |
| er_type2_miss | 0 | | frames with FTB type 2 |
| miss | | | |
| er_type6_miss | 0 | | frames with FTB type 6 |
| miss | | | |
| er_zone_miss | 0 | | frames with hard zoning |
| miss | | | |
| er_lun_zone_miss | 0 | | frames with LUN zoning |
| miss | | | |
| er_crc_good_eof | 0 | | Crc error with good eof |
| er_inv_arb | 0 | | Invalid ARB |
| er_single_credit_loss | 0 | | Single vcrdy/frame loss |
| on link | | | |
| er_multi_credit_loss | 0 | | Multiple vcrdy/frame |
| loss on link | | | |
| other_credit_loss | 0 | | Link timeout/complete |
| credit loss | | | |
| phy_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | | Timestamp of |
| phy_port stats clear | | | |
| lgc_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | | Timestamp of |
| lgc_port stats clear | | | |
| fec_corrected_rate | 0 | | FEC Corrected blocks per |
| second | | | |

portstats64show 59

| | | |
|---------------|---|--|
| stat64_wtx | 0 | top_int : 4-byte words transmitted |
| | 0 | bottom_int : 4-byte words transmitted |
| stat64_wrx | 0 | top_int : 4-byte words received |
| | 0 | bottom_int : 4-byte words received |
| stat64_ftx | 0 | top_int : Frames transmitted |
| | 0 | bottom_int : Frames transmitted |
| stat64_frx | 0 | top_int : Frames received |
| | 0 | bottom_int : Frames received |
| stat64_c2_frx | 0 | top_int : Class 2 frames received |
| | 0 | bottom_int : Class 2 frames received |
| stat64_c3_frx | 0 | top_int : Class 3 frames received |
| | 0 | bottom_int : Class 3 frames received |
| stat64_lc_rx | 0 | top_int : Link control frames received |
| | 0 | bottom_int : Link control frames |

| | | | |
|---|---|------------|--------------------------------|
| received | | | |
| stat64_mc_rx | 0 | top_int | : Multicast frames received |
| | 0 | bottom_int | : Multicast frames received |
| stat64_mc_to | 0 | top_int | : Multicast timeouts |
| | 0 | bottom_int | : Multicast timeouts |
| stat64_mc_tx | 0 | top_int | : Multicast frames transmitted |
| | 0 | bottom_int | : Multicast frames |
| transmitted | | | |
| tim64_rdy_pri | 0 | top_int | : Time R_RDY high priority |
| | 0 | bottom_int | : Time R_RDY high priority |
| tim64_txcrd_z | 0 | top_int | : Time BB_credit zero |
| | 0 | bottom_int | : Time BB_credit zero |
| er64_enc_in | 0 | top_int | : Encoding errors inside of |
| frames | 0 | bottom_int | : Encoding errors inside of |
| frames | | | |
| er64_crc | 0 | top_int | : Frames with CRC errors |
| | 0 | bottom_int | : Frames with CRC errors |
| er64_trunc | 0 | top_int | : Frames shorter than minimum |
| | 0 | bottom_int | : Frames shorter than minimum |
| er64_toolong | 0 | top_int | : Frames longer than maximum |
| | 0 | bottom_int | : Frames longer than maximum |
| er64_bad_eof | 0 | top_int | : Frames with bad end-of-frame |
| | 0 | bottom_int | : Frames with bad end-of- |
| frame | | | |
| er64_enc_out | 0 | top_int | : Encoding error outside of |
| frames | 0 | bottom_int | : Encoding error outside of |
| frames | | | |
| er64_disc_c3 | 0 | top_int | : Class 3 frames discarded |
| | 0 | bottom_int | : Class 3 frames discarded |
| er64_pcs_blk | 0 | top_int | : PCS block errors |
| | 0 | bottom_int | : PCS block errors |
| stat64_rateTxFrame | 0 | | Tx frame rate (fr/sec) |
| stat64_rateRxFrame | 0 | | Rx frame rate (fr/sec) |
| stat64_rateTxPeakFrame | 0 | | Tx peak frame rate (fr/sec) |
| stat64_rateRxPeakFrame | 0 | | Rx peak frame rate (fr/sec) |
| stat64_rateTxWord | 0 | | Tx Word rate (words/sec) |
| stat64_rateRxWord | 0 | | Rx Word rate (words/sec) |
| stat64_rateTxPeakWord | 0 | | Tx peak Word rate (words/sec) |
| stat64_rateRxPeakWord | 0 | | Rx peak Word rate (words/sec) |
| stat64_PRJTFrames | 0 | top_int | : Number of PRJT frames |
| returned to this port | 0 | bottom_int | : Number of PRJT |
| frames returned to this port | | | |
| stat64_PBSYFrames | 0 | top_int | : Number of PBSY frames |
| returned to this port | 0 | bottom_int | : Number of PBSY |
| frames returned to this port | | | |
| stat64_inputBuffersFull | 0 | top_int | : Number of occurrences |
| when all input buffers full | 0 | bottom_int | : Number of |
| occurrences when all input buffers full | | | |
| stat64_rxClass1Frames | 0 | top_int | : Number of class 1 |

```

frames received          0          bottom_int : Number of class 1
frames received
stat64_aveTxFrameSize  0          Average Tx Frame size
stat64_aveRxFrameSize  0          Average Rx Frame size
Lr_in                   0          top_int
                        0          bottom_int
Ols_in                  0          top_int
                        0          bottom_int
Lr_out                  0          top_int
                        0          bottom_int
Ols_out                 0          top_int
                        0          bottom_int
Link_failure            0          top_int
                        0          bottom_int
Invalid_CRC             0          top_int
                        0          bottom_int
Invalid_word            0          top_int
                        0          bottom_int
Protocol_err            0          top_int
                        0          bottom_int
Loss_of_sig             0          top_int
                        0          bottom_int
Loss_of_sync            0          top_int
                        0          bottom_int
er_bad_os               0          top_int : Invalid ordered set
                        0          bottom_int: Invalid ordered set

```

```

portrouteshow 59
port address ID: 0x013b00
external unicast routing table:
  0: Embedded
 255: Embedded
internal unicast routing table:
  0: Embedded

```

```
portcamshow 59
```

```

-----
Port  SID used  DID used  SID entries  DID entries
59    0         0        000000     000000
-----

```

```
ptbufshow, ptcreditshow, ptdatashow, ptstatsshow 59
```

```

S:
S:VF Enable:          1
S:
S:C4 Global Variable:
S:-----
-----
S:trace_stop:        0
S:
S:C4 Phy Data Pointers: c4_phyp = 0xb6ab2080
S:-----

```

```

-----
S:tnodep                0xbb82c000      pt
    0x43028001
S:proto_phy             0xb8804c60      phy_cfg
0xb6ab30c0
S:c4_chp                0x97e28000      c4_lgcp
0x97f4c000
S:c4_phy_regp          0x81c08000      proc_dir
0xb85123c0
S:-----
-----
S:magic_id              0xc4345678      num_port_timer    12
S:prev_if_id           0x43020001      S:ftx              0
    tov              0
S:initialized           0                port_idx            1
S:ui_idx                59              slot_no
    0
S:blade_idx            1                sw_usr_ports        400
S:unused                0                intr_debounced
    0
S:aec_status            0x0              reason_code
    0
S:debug                 0x00000004      debug_trc_line     0
S:rxbuf_list_head      0xffffffff      rxbuf_list_tail
0xffffffff
S:isAePort              0                port_misc_data
    0
S:num_fault1_rx_disc    0                num_fault2_rx_disc 0
S:p_lli_cause0          0                p_sig_regained     0
S:p_sync_regained      0                enc_out
    0x0
S:cached_fps_status    0                cached_sts_status  0
S:cached_er_crc_good_eof 0
S:cached_er_bad_os     0                cached_er_too_long 0
S:cached_er_trunc      0
cached_tot_er_crc_good_eof 0
S:num_pt_excess_intr    0                num_no_fid          0
S:num_fault1_cnt        0                num_fault2_cnt
    0
S:num_fault_lip         0                num_fault_lli       0
S:num_fault_rx_fifo    0                num_fault_hss       0
S:num_fault_bwait      0                lli_intr_prim
    0
S:num_sw_link_to        0
be_link_err_mon_count  0
S:ecb_enc_enabled      0                ecb_comp_enabled
    0
S:ecb_rsv_enc           0                ecb_rsv_comp        0
S:ecb_enc_bm           0x0              ecb_key_index
0xffffffff
S:fab_idx              4
S:num_be_lto           0                lto_count_reset_intvl
    0
S:lr_count_reset_intvl 0                num_be_lr

```

```

      0
S:num_fault_qsfp          0          check_lto
      0
S:credit_loaded          0          num_credit_overrun
      0
S:fec_enabled            0x0          fec_los_to_flag          0x0
S:phy_stats_clear_ts    1725611419    pcs_err_online
      0
S:pcs_err_light_det      0          pcs_err_ignore
      0
S:pcs_blk_err            0          pcs_hiber          0
S:phy_port_status        0          ecb_enc_lr_count
      0
S:dport_mode             0          avoid_lto_det          0
S:sn_debounced          0x0          sn_started_kr_reqd      0
S:major_timer_started    0x0          ready_bm          0x0
S:parln_1_bm            0x0          parln_0_bm          0x0
S:be_los_of_sync_event_intvl 0
be_los_of_sync_event      0
S:errataPtenable_cntr    0          errataPoll_cntr
      0
S:jda_rx_sig_loss_det    0          jda_rx_sig_loss_cnt
      0
S:encrypt_blk_error      0
S:
S:      c4_trunk
S:=====
S:mark_ts                0x0          deskew          0x0
S:master_phyp            0x0
S:
S:adelay[00]: 0x00000000 0x00000000 0x00000000 0x00000000
S:adelay[04]: 0x00000000 0x00000000 0x00000000 0x00000000
S:
S:      c4_buf
S:=====
S:tx_csc                  0          rx_csc
      0
S:ld_vc_credits          0          tx_flag          0x0
S:alloc_buffers          0          req_buffers          0
S:est_buffers            20          ld_use_est          0
S:bb_sc_n                 0          rx_bb_sc_n
      0
S:data_cr                  5          nondata_cr
      6
S:cr_enable              0
S:ld_nondata_cr          6          tnodep
0xbb82c0e0
S:tx_credits[0] 0 0 0 0 0 0 0 0
S:tx_credits[8] 0 0 0 0 0 0 0 0
S:tx_credits[16] 0 0 0 0 0 0 0 0 0 0
S:tx_credits[24] 0 0 0 0 0 0 0 0 0 0
S:tx_credits[32] 0 0 0 0 0 0 0 0 0 0
S:rx_credits[0] 0 0 0 0 0 0 0 0
S:rx_credits[8] 0 0 0 0 0 0 0 0

```

```

S:rx_credits[16]      0    0    0    0    0    0    0    0    0
S:rx_credits[24]      0    0    0    0    0    0    0    0    0
S:rx_credits[32]      0    0    0    0    0    0    0    0    0
S:tx_mbc[0]          0    0    0    0    0    0    0    0    0
S:tx_mbc[8]          0    0    0    0    0    0    0    0    0
S:tx_mbc[16]         0    0    0    0    0    0    0    0    0
S:tx_mbc[24]         0    0    0    0    0    0    0    0    0
S:tx_mbc[32]         0    0    0    0    0    0    0    0    0
S:rx_mbc[0]          0    0    0    0    0    0    0    0    0
S:rx_mbc[8]          0    0    0    0    0    0    0    0    0
S:rx_mbc[16]         0    0    0    0    0    0    0    0    0
S:rx_mbc[24]         0    0    0    0    0    0    0    0    0
S:rx_mbc[32]         0    0    0    0    0    0    0    0    0

```

S:

S:C4 Chip Variables: c4_phyp->c4_chp = 0x97e28000

S:-----

S:version = 2.1

S:magic_id 0xc4234567 init_state 0x8

S:reset_reg_mem 0x1

S:ch_int0_en_bm 0x0 intr0_cause 0x0

S:ch_int1_en_bm 0x0 intr1_cause 0x0

S:ch_int2_en_bm 0x0 intr2_cause 0x0

S:ch 0x43010080 ch_cfg

0xb7013ba0

S:raslog_hndl.hndl 0x0 obj_halted 0x0

S:c4_chip_regp 0x80000000 c4_fpg_regp

0x81800000

S:num_chip_timer 0x5

S:hi_task_bm 0x0 lo_task_bm 0x0

S:c4_deferq.q_head 0x0 c4_deferq.q_tail 0x0

S:c4_tmrq.q_head 0x0 c4_tmrq.q_tail 0x0

slot_no 0

S:chip_inst 0 chip_idx 0

S:pll_initialized 1

pll_serdes_initialized 1

S:init_tries 0 init_ptEnableBM

0xba01b488

S:tick_polling 0xb980c9c0 sec_polling

0xb980c960

S:bb_fid 129

S:ecb_key_bm[0] 0x0 ecb_key_bm[1] 0x0

S:ecb_key_bm[2] 0x0 ecb_key_bm[3] 0x0

S:is_chip_enc_enabled

is_chip_comp_enabled 0x0

S:ftb_rsrcp->ftb_flags 0x0 act_rsrcp->act_flag 0x1

S:lue_rsrcp->lue_flags[0] 0x0 lue_rsrcp-

>lue_flags[1] 0x0

S:c4_phyp[00]: 0xb6ab0000 0xb6ab2080 0xb6ab4100 0xb6ab6180

S:c4_phyp[04]: 0xb6ab9040 0xb6abb0c0 0xb6abd140 0xb6ac0000

S:c4_phyp[08]: 0xb6ac2080 0xb6ac4100 0xb6ac6180 0xb6ac9040

S:c4_phyp[12]: 0xb6acb0c0 0xb6acd140 0xb6ad0000 0xb6ad2080

S:c4_phyp[16]: 0xb6ad4100 0xb6ad6180 0xb6ad9040 0xb6adb0c0

S:c4_phyp[20]: 0xb6add140 0xb6ae0000 0xb6ae2080 0xb6ae4100

```

S:c4_phyp[24]: 0xb6ae6180 0xb6ae9040 0xb6aeb0c0 0xb6aed140
S:c4_phyp[28]: 0xb6af0000 0xb6af2080 0xb6af4100 0xb6af6180
S:c4_phyp[32]: 0xb6af9040 0xb6afb0c0 0xb6afd140 0xb6b00000
S:c4_phyp[36]: 0xb6b02080 0xb6b04100 0xb6b06180 0xb6b09040
S:c4_phyp[40]: 0xb6b0b0c0 0xb6b0d140 0xb6b10000 0xb6b12080
S:c4_phyp[44]: 0xb6b14100 0xb6b16180 0xb6b19040 0xb6b1b0c0
S:c4_phyp[48]: 0xb6b1d140 0xb6b20000 0xb6b22080 0xb6b24100
S:c4_phyp[52]: 0xb6b26180 0xb6b29040 0xb6b2b0c0 0xb6b2d140
S:c4_phyp[56]: 0xb6b30000 0xb6b32080 0xb6b34100 0xb6b36180
S:c4_phyp[60]: 0xb6b39040 0xb6b3b0c0 0xb6b3d140 0xb6b40000
S:c4_lgcp[00]: 0x97f48000 0x97f4c000 0x97f50000 0x97f54000
S:c4_lgcp[04]: 0x97f58000 0x97f5c000 0x97f60000 0x97f64000
S:c4_lgcp[08]: 0x97f68000 0x97f6c000 0x97f70000 0x97f74000
S:c4_lgcp[12]: 0x97f78000 0x97f7c000 0x97f80000 0x97f84000
S:c4_lgcp[16]: 0x97f88000 0x97f8c000 0x97f90000 0x97f94000
S:c4_lgcp[20]: 0x97f98000 0x97f9c000 0x97fa0000 0x97fa4000
S:c4_lgcp[24]: 0x97fa8000 0x97fac000 0x97fb0000 0x97fb4000
S:c4_lgcp[28]: 0x97fb8000 0x97fbc000 0x97fc0000 0x97fc4000
S:c4_lgcp[32]: 0x97fc8000 0x97fcc000 0x97fd0000 0x97fd4000
S:c4_lgcp[36]: 0x97fd8000 0x97fdc000 0x97fe0000 0x97fe4000
S:c4_lgcp[40]: 0x97fe8000 0x97fec000 0x97ff0000 0x97ff4000
S:c4_lgcp[44]: 0x97ff8000 0x97ffc000 0x8e000000 0x8e004000
S:c4_lgcp[48]: 0x8e008000 0x8e00c000 0x8e010000 0x8e014000
S:c4_lgcp[52]: 0x8e018000 0x8e01c000 0x8e020000 0x8e024000
S:c4_lgcp[56]: 0x8e028000 0x8e02c000 0x8e030000 0x8e034000
S:c4_lgcp[60]: 0x8e038000 0x8e03c000 0x8e040000 0x8e044000
S:chip_timers[00]: 0xb980c720 0xb980c780 0xb980c7e0 0xb980c840
S:chip_timers[04]: 0xb980c8a0 0xb980c900
S:disc_trap_enable_required      0x0          rxlp_disc_log_stop
      0x0
S:curr_rxlp_frm_cnt      0x0          curr_rxlp_disc_frm_cnt  0x0
S:sw_disc_frm_cnt      0x0          last_disc_frm_cnt      0x0
S:txq_nopop_pr_cnt      0x0          pollErrataDfe_ptBM
0xba01b4b0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][0]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][1] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][2]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][0] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][1]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][2] 0x0
S:
S:C4 Logical Port Variables
S:-----
-----
S:c4_lgc_regp      0x81c08000
S:c4_phyp:
S:      0xb6ab2080      0x0          0x0          0x0

S:      0x0          0x0          0x0          0x0

S:master_phyp      0xb6ab2080      if_id
0x43020001
S:min_phyp      0x0          max_phyp      0x0
S:num_phy_ports      1          lgc_num      1

```

```

S:num_iu_to          0          sw_txq_bm
  0
S:port_fid          129          unused          0
S:port_group        0          lgc_stats_clear_ts
          1725611419
S:domain_tbl_sel    0          area_tbl_sel
  0
S:egid_tbl_sel      0
S:serv_lo_bm        0x0
S:
S:Proto Phy Variables:
S:-----
-----
S:magic_id          0xc4123456    asic_phyp
0xb6ab2080
S:port_id           0x43028001    phy_cfg
          0xb6ab30c0
S:upsm_hdl          0xb800f3c0    physm_hdl
0xb800f140
S:ov_snsn_hdl       0xb800f000    sw_snsn_hdl
0xb800f0a0
S:ov_lksm_hdl       0xb800f1e0    sw_lksm_hdl
0xb800f280
S:trksm_hdl         0xb800f320    lr_flag          0x0
S:lr_active         0x0          qsfp_txrx_rate_sel
          0x0
S:
S:UPSM             UP00: UPST_PORT_DISABLED    --> UP00: UPST_PORT_DISABLED
S:SNSM(OV)         SN00: OV_SNST_STOPPED        --> SN00: OV_SNST_STOPPED
S:SNSM(SW)         SW00: SW_SNST_STAGE_WS    --> SW00: SW_SNST_STAGE_WS
S:PHYSM           PP00: PHYST_STOPPED        --> PP00: PHYST_STOPPED
S:LKSM(OV)         LK00: OV_LKST_INACTIVE    --> LK00: OV_LKST_INACTIVE
S:LKSM(SW)         SW13: INACTIVE          --> SW13: INACTIVE
S:TRKSM           TRK0: TRKST_INIT          --> TRK0: TRKST_INIT
S:
S:physm variables:
S:-----
-----
S:proto_phyp        0xb8804c60    physm_hdl
0xb800f140
S:force_offline     0          copper          0
S:fault_reason      0: UNKNOWN
S:phy_media_present 0
S:
S:snsn variables:
S:-----
-----
S:speed             0xff          proto_phyp
0xb8804c60
S:hw_sn_tries_left  0x0          sw_sn_tries_left    0x0
S:curr_txsp_count   0x0
S:tx_max            0x0          curr_tx_indx
          0x0
S:curr_tx           0x0          curr_rxsp_count

```

```

    0x0
S:rx_max                0x0                curr_rx_indx
    0x0
S:curr_rx               0x0                rx_mem
    0x0
S:rxsp_rec_count       0x0
S:nc_start              0x0                tx_start                0x0
S:sync_start           0x0                sync_present            0x0
S:diag_auto            0x0                diag_speed              0xff
S:striped_wd_tov       3000                hw_wd_tov
    3000
S:step                  0x0                qsfp28_speed_mode
    0x0
S:qsfp_mode0_hw_sn_tries_left  0x0
S:qsfp_mode1_hw_sn_tries_left  0x0
S:
S:lksm variables:
S:-----
-----
S:proto_phyph          0xb8804c60        ov_lksm_hdl
0xb800f1e0
sw_lksm_hdl            0xb800f280
num_lf1                0
S:hw_link_tries_left   0                sw_link_tries_left     0
S:buf_ptype            0x0                stored_entry_state      0x6
S:handshake_owner      0x0                mark_unsent
    0x0
S:busybuf_stuck        0x0                lr_wait                0x0
S:
S:trksm variables:
S:-----
-----
S:Not a trunk port
S:
S:upsm variables:
S:-----
-----
S:proto_phyph          0xb8804c60        upsm_hdl
0xb800f3c0
S:bb_credits           0                port_beacon             0
S:port_diag_flag       0                force_offline
    0
S:port_fault_rsn       0: PORT_NO_FAULT
S:retry_init_rsn       0: UNKNOWN
S:linit_reason         0                linit_result           0
S:ie_fctl_mode         0                fec_in_sync_tries_left 0
S:retry_sn_fail_init   0
retry_link_fail_init   0
S:excess_lr_count      0
S:
S:c4_ch_cfg
S:-----
-----
S:c4_desc_ring_size    256                292                256                256                292

```



```

292      2      292      292
S:thresh_def          0      16      1      0
S:intr_tries          500      cmem_pattern
0xdeadbeef
S:cmem_pattern_upwd   2      cmem_init_time      16
S:cmem_init_tries    5
S:ctrl_par_thresh    2      data_par_thresh
4
S:cam_par_thresh     4      buf_loss_thresh
12
S:crit_par_thresh    2      non_crit_par_thresh
6
S:pci_abort_thresh   10      pci_err_thresh      5
S:excess_chintr_thresh 8      sw_err_thresh      20
S:err_sample_period  300      intr_sleep
20000
S:frame_timeout      2500      proxy_dev      16384
S:vf_route           81920      qos      2048
S:stats 2048      f_redirect      2048
S:rsp_trap           2048      lun_zoning      20480
S:area_mode          0      ftb_max_loop[0]    0
S:ftb_max_loop[1]    6      ftb_max_loop[2]    9
S:ftb_max_loop[3]    10      ftb_max_loop[4]    10
S:ftb_max_loop[5]    5      ftb_max_loop[6]    6
S:ftb_seg_size[0]    0      ftb_seg_size[1]
16384
S:ftb_seg_size[2]    65536      ftb_seg_size[3]
16384
S:ftb_seg_size[4]    16384      ftb_seg_size[5]
65536
S:ftb_seg_size[6]    16384      ftb_seg_base[0]    0
S:ftb_seg_base[1]    0      ftb_seg_base[2]
65536
S:ftb_seg_base[3]    16384      ftb_seg_base[4]
32768
S:ftb_seg_base[5]    131072      ftb_seg_base[6]
49152
asic_err_monitor_period1 300
asic_err_monitor_period2 86400
zone_chk_to_poll_period 25
zone_chk_class2_reject_tov 220

```

S:

S:c4_phy_cfg

S:-----

S:version = 2.1

S:pt 0x43028001 fab_ptr

0x9a800000

S:fabattr 0x9a8000d4 fab_iop

0x9a800050

S:cfgbm 0xbb82be04 port_ctrl

0xb6ab30d8

S:pcap.pcap_bm 0x8d215547 pcap.pcap2_bm

0x2588289

```

S:pcap.pcap3_bm          0x1bebe0c
ui_idx                   59
    0
is_icl                   0
S:neg_speed              0 0 0 0 0
S:my_domain              0x1
S:hw_sn_maxtries        100
    0
S:hw_link_maxtries      10
S:rx_cyc_tov            28
S:bufrdy_tov            300
S:mark_tov              300
S:buf_dealloc_wait      4
S:hw_lk_train_tov       540
    150
S:syswait_tx_12_lips    1
S:al_time_tov           15
S:intr_tries_port       500
    250
S:intr_lsrflt_debounce  500
S:port_no_fid           3
S:port_fault1_thresh    100
S:port_fault1_disc_thresh 500
port_fault1_disc_spur_thresh 1000
S:port_fault2_thresh    5
S:port_sw_link_to       15
    1
frc_hw_sn_mode           0x1
S:enc_poll_thresh       0
S:fec_in_sync_to        50
    4
S:port_be_lto_threshold 100
    2
S:be_cr_in_sync_to      5
port_credit_overrun_thresh 10
S:jda_sfp_losig_tov     400
jda_sfp_losig_try_max   30
S:striped_wd_tov        3000
no_sync_debounce        1200
S:
S:    fab_iop
S:=====
S:fab_iop->interop_mode  0x0
S:fab_iop->fl_bbc        0x0
    0x0
S:fab_iop->fl_cls        0x4
    0x0
S:fab_iop->domain_id_offset 0x60
>mcdt_fabric_mode       0x0
S:fab_iop->mcdt_default_zone 0x0
>mcdt_safe_zone         0x0
S:
S:    port_ctrl
S:slot_no
S:sw_usr_ports          400
port_mode               0x0
    sw_sn_maxtries
sw_link_maxtries        5
rttov                   300
busybuf_tov             286
lksm_tov                3000
hw_wd_tov               3000
    hw_lk_test_tov
lip_rx_tov              55
lp_tov                  2000
    intr_mod_debounce
intr_efifo_debounce     100
excess_ptintr_thresh    8
port_fault1_spur_thresh 250
losync_tov              100
    en_8g_scramble
fec_enable
fec_in_sync_try_max
port_be_lr_threshold

```

```

S:=====
S:port_ctrl.port_type 1 port_ctrl.port_grp 0
S:port_ctrl.port_number 59 port_ctrl.vc_mode 1
S:
S: port_ctrl.lcap
S:=====
S:has_serdes 0 has_media 1
S:topology 1 skip_nego 0
S:skip_pnego 0 skip_init_event 0
S:en_shim 0 speed_neg 1
S:loop_back 0 num_speeds 5
S:fec_enable 0
S:
S: port_ctrl.speed_list array
S:=====
S:speed_list[0].auto_neg 1 speed_list[0].lnk_speed 0x0000000a
S:speed_list[1].auto_neg 1 speed_list[1].lnk_speed 0x00000008
S:speed_list[2].auto_neg 1 speed_list[2].lnk_speed 0x00000006
S:speed_list[3].auto_neg 1 speed_list[3].lnk_speed 0x00000005
S:speed_list[4].auto_neg 1 speed_list[4].lnk_speed 0x00000003
S:speed_list[5].auto_neg 0 speed_list[5].lnk_speed 0x00000000
S:
S: port_ctrl.cm
S:=====
S:port_ctrl.cm.num_vcs 8
S:port_ctrl.cm.min_bufs 8
S:port_ctrl.cm.cr_shar_bufs 0
S:port_ctrl.vc_alloc
S:port_ctrl.vc_alloc 2 0 1 1 1 1 1 1
S:port_ctrl.vc_alloc 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.norm_vc_alloc
S:port_ctrl.norm_vc_alloc 4 0 5 5 5 5 1 1
S:port_ctrl.norm_vc_alloc 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.cm.skip_bb_credit 0
S:port_ctrl.cm.use_shim_based_sublist 0
S:
S: port_ctrl.serdes_set
S:=====
S:serdes_type 0x8
S:serdes_data_t.ibm_hss_serdes.tx_drive_power 0x1
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b_sign 0x1
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b 0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_a 0x0
S:serdes_data_t.ibm_hss_serdes.rxeq 0x0
S:
S: cfgbm
S:=====
S:old_distance 0x0 gport_lockdown 0x0
S:tport 0x1 speed 0x0
S:disable_eport 0x0 fcacc 0x0
S:lport_lockdown 0x0 priv_lport_lockdown

```

```

    0x0
S:vcxlt_linit          0x0          delay_flogi          0x0
S:isl_interop         0x0          distance             0x0
S:BufStarvFlag       0x0          credit_sharing       0x0
S:lport_halfduplex   0x0          lport_fairness       0x0
S:soft_neg           0x0          asn_frc_hwretry      0x0
S:cr_recov           0x0          fport_buffers        0x0
S:export              0x0          export_mode          0x0
    0x0
S:csctl_en           0x0          mirror_port          0x0
S:fault_delay        0x0          non_dfe              0x0
S:fec_configured*(0=ENAB) 0          fec_tts              0
    0
S:port_persistently_disabled (permanently) 0 (0)
S:
S:    cfg property
S:=====
S:priv_pcfg_bm        0x00000000    lgcl_pcfg_bm
0xbb82be44
S:fport_buffer        0x00000000
S:
S:
S:C4 Discard Cntrs: rxlp_stats = 0xb6ab2430
S:-----
-----
S:disc_mcast_wka      0x0          disc_inv_did         0x0
S:disc_cl1_cl4        0x0          disc_sid_chk_fail    0x0
S:disc_inv_dom_egid_txpt 0x0          disc_vft_hop_cnt_1
0x0
S:disc_classf         0x0          disc_fcp_cdb_inv     0x0
S:disc_vfid_trap_enabled 0x0
disc_vfid_hdr_chk_fail 0x0
S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err 0x0
S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err 0x0
S:disc_ftb_vm_mode    0x0          disc_ftb_agnt2_miss  0x0
S:disc_ecb_de_pad_err 0x0          disc_ecb_de_tag_err   0x0
S:disc_ecb_de_seq_err 0x0          disc_ecb_err          0x0
S:disc_ftb_type4_match 0x0          disc_fcp_rsp_ftb_type4 0x0
S:disc_fcp_rsp_ftb_type4 0x0          disc_ftb_type5_match
0x0
S:disc_ftb_type3_match 0x0          disc_els_ftb_type3   0x0
S:disc_ftb_type1_match 0x0          disc_els_rsp_ex_port  0x0
S:disc_inv_drp_dps    0x0          disc_did_lookup_miss 0x0
S:disc_ftb_type2_match 0x0          disc_trpd_plogi_pdisc 0x0
S:disc_type2_lookup_miss 0x0          disc_ftb_type6_match
0x0
S:disc_els_rep_ex_port 0x0          disc_els_sid_lkup_bit1 0x0
S:disc_els_sid_lkup_bit0 0x0
disc_bls_frm_trap_bit1 0x0
S:disc_ftb_token_err  0x0          disc_asic_internal_err 0x0
S:disc_hard_zone_miss 0x0          disc_lun_zone_miss    0x0
S:discflt_frame_disc  0x0          discflt_parity_err    0x0
S:disc_frame_marked_du 0x0          disc_frame_marked_to  0x0
E:Connection type: FE

```

```

E:Port type: E_port
E:Trunk port: No
E:Configured Speed: AUTO_SPEED_NEGO
E:Max Capable Speed: 32G
E:Current SNSM Speed: UNDEFINED
E:Hardware TX Speed: 32G (0x00000004)
E:Hardware RX Speed: 32G (0x00000040)
E:
E:Interrupts:      0          Link_failure:      0
Loss_of_sync:     0          Loss_of_sig:       0
E:Lli:            0          Invalid_word:      0
E:trapped_frm:    0          fwd_status_ok:     0
E:fwd_timeout:    0          fwd_tx_unavail:    0
E:fwd_unroutable: 0          fwd_zone_out:      0
E:fwd_other_err:  0          frm_err_discard:   0
E:Fltr listA:     0          Fltr listB:        0
E:Zone trap fwd:  0          Zone trap disc:    0
E:shim_csum:      0          RTE_perr:          0
E:Invalid_crc:    0          Delim_err:         0
E:Protocol_err:   0
E:Lr_in:          0          Lr_out:            0
E:Ols_in:         0          Ols_out:           0

```

filterportshow 59

FILTER DATA

```

-----
Shadow settings:
  Filter Enable: 0x00000000
  Redir RAM[0]: 0x00000000
  Redir RAM[1]: 0x00000000
  Redir RAM[2]: 0x00000000
  Redir RAM[3]: 0x00000000
  Redir RAM[4]: 0x00000000
  Redir RAM[5]: 0x00000000
  Redir RAM[6]: 0x00000000
  Redir RAM[7]: 0x00000000
  Redir RAM[8]: 0x00000000
  Redir RAM[9]: 0x00000000
  Redir RAM[10]: 0x00000000
  Redir RAM[11]: 0x00000000
  Redir RAM[12]: 0x00000000
  Redir RAM[13]: 0x00000000
  Redir RAM[14]: 0x00000000
  Redir RAM[15]: 0x00000000
  Redir RAM[16]: 0x00000000
  Redir RAM[17]: 0x00000000
  Redir RAM[18]: 0x00000000
  Redir RAM[19]: 0x00000000
  Redir RAM[20]: 0x00000000
  Redir RAM[21]: 0x00000000
  Redir RAM[22]: 0x00000000
  Redir RAM[23]: 0x00000000

```

Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass: 0x00000000

Real settings:

Enable RAM: 0x00000000, 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass RAM: 0x00000000

Shadowed filters:

Filter 0: Not Installed (MIRROR1)(LISTA)

c4_fldenable[0] = 0x00000000 0x00000000 0x00000000
0x00000000

c4_fldnegate[0] = 0x00000000, c4_fltr_config[0] = 0x00000000

Filter 1: Not Installed (MIRROR2)(LISTA)

c4_fldenable[1] = 0x00000000 0x00000000 0x00000000
0x00000000

```
    c4_fldnegate[1] = 0x00000000,c4_fltr_config[1] = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
    c4_fldenable[2] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[2] = 0x00000000,c4_fltr_config[2] = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
    c4_fldenable[3] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[3] = 0x00000000,c4_fltr_config[3] = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
    c4_fldenable[4] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[4] = 0x00000000,c4_fltr_config[4] = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
    c4_fldenable[5] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[5] = 0x00000000,c4_fltr_config[5] = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
    c4_fldenable[6] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[6] = 0x00000000,c4_fltr_config[6] = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
    c4_fldenable[7] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[7] = 0x00000000,c4_fltr_config[7] = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
    c4_fldenable[8] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[8] = 0x00000000,c4_fltr_config[8] = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
    c4_fldenable[9] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[9] = 0x00000000,c4_fltr_config[9] = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
    c4_fldenable[10] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[10] = 0x00000000,c4_fltr_config[10] =
0x00000000
Filter 11: Not Installed (SIM)(LISTA)
    c4_fldenable[11] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[11] = 0x00000000,c4_fltr_config[11] =
0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
    c4_fldenable[12] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[12] = 0x00000000,c4_fltr_config[12] =
0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
    c4_fldenable[13] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[13] = 0x00000000,c4_fltr_config[13] =
0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
```

```
    c4_fldenable[14] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[14] = 0x00000000,c4_fltr_config[14] =
0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
    c4_fldenable[15] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[15] = 0x00000000,c4_fltr_config[15] =
0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
    c4_fldenable[16] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[16] = 0x00000000,c4_fltr_config[16] =
0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
    c4_fldenable[17] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[17] = 0x00000000,c4_fltr_config[17] =
0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
    c4_fldenable[18] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[18] = 0x00000000,c4_fltr_config[18] =
0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
    c4_fldenable[19] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[19] = 0x00000000,c4_fltr_config[19] =
0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
    c4_fldenable[20] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[20] = 0x00000000,c4_fltr_config[20] =
0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
    c4_fldenable[21] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[21] = 0x00000000,c4_fltr_config[21] =
0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
    c4_fldenable[22] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[22] = 0x00000000,c4_fltr_config[22] =
0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
    c4_fldenable[23] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[23] = 0x00000000,c4_fltr_config[23] =
0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
    c4_fldenable[24] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[24] = 0x00000000,c4_fltr_config[24] =
0x00000000
```


Filter 25: Not Installed (PERF10)(LISTA)
c4_fldenable[25] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[25] = 0x00000000,c4_fltr_config[25] =
0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
c4_fldenable[26] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[26] = 0x00000000,c4_fltr_config[26] =
0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
c4_fldenable[27] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[27] = 0x00000000,c4_fltr_config[27] =
0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
c4_fldenable[28] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[28] = 0x00000000,c4_fltr_config[28] =
0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
c4_fldenable[29] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[29] = 0x00000000,c4_fltr_config[29] =
0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
c4_fldenable[30] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[30] = 0x00000000,c4_fltr_config[30] =
0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
c4_fldenable[31] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[31] = 0x00000000,c4_fltr_config[31] =
0x00000000

Real filters:

Filter 0: Not Installed (MIRROR1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,

```
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 11: Not Installed (SIM)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
```

fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,

fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter dirty indicator: 0x00000000
Performance filters: 0
Port Mirror filters: 0 (0x0)

FIELD DATA

Shadowed fields:

fldoffset[0] = 0x00, fldmask[0] = 0x00, fldvalue_dyna[0]: 0x00 0x00
0x00 0x00
fldcontrol[0].inuse = 0x0 fldcontrol[0].refcnt = 0x00 0x00 0x00
0x00
fldoffset[1] = 0x00, fldmask[1] = 0x00, fldvalue_dyna[1]: 0x00 0x00
0x00 0x00
fldcontrol[1].inuse = 0x0 fldcontrol[1].refcnt = 0x00 0x00 0x00
0x00
fldoffset[2] = 0x00, fldmask[2] = 0x00, fldvalue_dyna[2]: 0x00 0x00
0x00 0x00
fldcontrol[2].inuse = 0x0 fldcontrol[2].refcnt = 0x00 0x00 0x00
0x00
fldoffset[3] = 0x00, fldmask[3] = 0x00, fldvalue_dyna[3]: 0x00 0x00
0x00 0x00
fldcontrol[3].inuse = 0x0 fldcontrol[3].refcnt = 0x00 0x00 0x00
0x00
fldoffset[4] = 0x00, fldmask[4] = 0x00, fldvalue_dyna[4]: 0x00 0x00
0x00 0x00
fldcontrol[4].inuse = 0x0 fldcontrol[4].refcnt = 0x00 0x00 0x00
0x00
fldoffset[5] = 0x00, fldmask[5] = 0x00, fldvalue_dyna[5]: 0x00 0x00
0x00 0x00
fldcontrol[5].inuse = 0x0 fldcontrol[5].refcnt = 0x00 0x00 0x00
0x00
fldoffset[6] = 0x00, fldmask[6] = 0x00, fldvalue_dyna[6]: 0x00 0x00
0x00 0x00
fldcontrol[6].inuse = 0x0 fldcontrol[6].refcnt = 0x00 0x00 0x00
0x00
fldoffset[7] = 0x00, fldmask[7] = 0x00, fldvalue_dyna[7]: 0x00 0x00
0x00 0x00
fldcontrol[7].inuse = 0x0 fldcontrol[7].refcnt = 0x00 0x00 0x00
0x00
fldoffset[8] = 0x00, fldmask[8] = 0x00, fldvalue_dyna[8]: 0x00 0x00
0x00 0x00
fldcontrol[8].inuse = 0x0 fldcontrol[8].refcnt = 0x00 0x00 0x00
0x00
fldoffset[9] = 0x00, fldmask[9] = 0x00, fldvalue_dyna[9]: 0x00 0x00
0x00 0x00

```
fldcontrol[9].inuse = 0x0 fldcontrol[9].refcnt = 0x00 0x00 0x00
0x00
fldoffset[10] = 0x00, fldmask[10] = 0x00, fldvalue_dyna[10]:0x00 0x00
0x00 0x00
fldcontrol[10].inuse = 0x0 fldcontrol[10].refcnt = 0x00 0x00 0x00
0x00
fldoffset[11] = 0x00, fldmask[11] = 0x00, fldvalue_dyna[11]:0x00 0x00
0x00 0x00
fldcontrol[11].inuse = 0x0 fldcontrol[11].refcnt = 0x00 0x00 0x00
0x00
fldoffset[12] = 0x00, fldmask[12] = 0x00, fldvalue_dyna[12]:0x00 0x00
0x00 0x00
fldcontrol[12].inuse = 0x0 fldcontrol[12].refcnt = 0x00 0x00 0x00
0x00
fldoffset[13] = 0x00, fldmask[13] = 0x00, fldvalue_dyna[13]:0x00 0x00
0x00 0x00
fldcontrol[13].inuse = 0x0 fldcontrol[13].refcnt = 0x00 0x00 0x00
0x00
fldoffset[14] = 0x00, fldmask[14] = 0x00, fldvalue_dyna[14]:0x00 0x00
0x00 0x00
fldcontrol[14].inuse = 0x0 fldcontrol[14].refcnt = 0x00 0x00 0x00
0x00
fldoffset[15] = 0x00, fldmask[15] = 0x00, fldvalue_dyna[15]:0x00 0x00
0x00 0x00
fldcontrol[15].inuse = 0x0 fldcontrol[15].refcnt = 0x00 0x00 0x00
0x00
fldoffset[16] = 0x00, fldmask[16] = 0x00, fldvalue_dyna[16]:0x00 0x00
0x00 0x00
fldcontrol[16].inuse = 0x0 fldcontrol[16].refcnt = 0x00 0x00 0x00
0x00
fldoffset[17] = 0x00, fldmask[17] = 0x00, fldvalue_dyna[17]:0x00 0x00
0x00 0x00
fldcontrol[17].inuse = 0x0 fldcontrol[17].refcnt = 0x00 0x00 0x00
0x00
fldoffset[18] = 0x00, fldmask[18] = 0x00, fldvalue_dyna[18]:0x00 0x00
0x00 0x00
fldcontrol[18].inuse = 0x0 fldcontrol[18].refcnt = 0x00 0x00 0x00
0x00
fldoffset[19] = 0x00, fldmask[19] = 0x00, fldvalue_dyna[19]:0x00 0x00
0x00 0x00
fldcontrol[19].inuse = 0x0 fldcontrol[19].refcnt = 0x00 0x00 0x00
0x00
```

Real fields:

```
fldoffset RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000
fldmask RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000
fld value4 RAM:
0x00000000
0x00000000
0x00000000
0x00000000
```

0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000

Field dirty indicator: 0x00000000

FDB reference count fdb: 0 [0 0 0 0]
FDB reference count fdb: 1 [0 0 0 0]
FDB reference count fdb: 2 [0 0 0 0]
FDB reference count fdb: 3 [0 0 0 0]
FDB reference count fdb: 4 [0 0 0 0]
FDB reference count fdb: 5 [0 0 0 0]
FDB reference count fdb: 6 [0 0 0 0]
FDB reference count fdb: 7 [0 0 0 0]
FDB reference count fdb: 8 [0 0 0 0]
FDB reference count fdb: 9 [0 0 0 0]
FDB reference count fdb: 10 [0 0 0 0]
FDB reference count fdb: 11 [0 0 0 0]
FDB reference count fdb: 12 [0 0 0 0]
FDB reference count fdb: 13 [0 0 0 0]
FDB reference count fdb: 14 [0 0 0 0]
FDB reference count fdb: 15 [0 0 0 0]
FDB reference count fdb: 16 [0 0 0 0]
FDB reference count fdb: 17 [0 0 0 0]
FDB reference count fdb: 18 [0 0 0 0]
FDB reference count fdb: 19 [0 0 0 0]

Filter counters:

Filter counter 0: 0 (MIRROR1)
Filter counter 1: 0 (MIRROR2)
Filter counter 2: 0 (MIRROR3)
Filter counter 3: 0 (MIRROR4)
Filter counter 4: 0 (AEPORT_NON_MIRR_DROP)
Filter counter 5: 0 (ZONING TRAP)
Filter counter 6: 0 (FCR_EXPORT_DC)
Filter counter 7: 0 (TIN TRAP)
Filter counter 8: 0 (FICON CUP)
Filter counter 9: 0 (FICON CUP DST)
Filter counter 10: 0 (WELL KNOWN ADDR)
Filter counter 11: 0 (SIM)
Filter counter 12: 0 (UNUSED)
Filter counter 13: 0 (UNUSED)

Filter counter 14: 0 (UNUSED)
Filter counter 15: 0 (UNUSED)
Filter counter 16: 0 (PERF1)
Filter counter 17: 0 (PERF2)
Filter counter 18: 0 (PERF3)
Filter counter 19: 0 (PERF4)
Filter counter 20: 0 (PERF5)
Filter counter 21: 0 (PERF6)
Filter counter 22: 0 (PERF7)
Filter counter 23: 0 (PERF8)
Filter counter 24: 0 (PERF9)
Filter counter 25: 0 (PERF10)
Filter counter 26: 0 (PERF11)
Filter counter 27: 0 (PERF12)
Filter counter 28: 0 (OPM1)
Filter counter 29: 0 (OPM2)
Filter counter 30: 0 (IPM1)
Filter counter 31: 0 (IPM2)

ACL DATA

Logical port 1: Hard Zoning disabled, Soft Zoning disabled
Zone type: WWN Zoning
Frames with hard zone miss: 0

*** Please use filterportshow on user port 56 to display ACL hash tables and Mirroring resources of thischip.
***We show this data only for the first physical port which is an external port.

portFcPortCmdShow --slot 0 60 3
doing portFcPortCmdShow: arg1 = 3, arg2 = -2

portshow 60
portDisableReason: None
portCFlags: 0x0
portFlags: 0x4021 PRESENT U_PORT DISABLED LED
LocalSwcFlags: 0x0
portType: 26.0
POD Port: Need license to enable the port
portState: 2 Offline
Protocol: FC
portPhys: 2 No_Module portScn: 2 Offline
port generation number: 0
state transition count: 0

portId: 013c00
portIfId: 43020004
portWwn: 20:3c:d8:1f:cc:2c:99:90
portWwn of device(s) connected:
16b Area list:
Distance: normal
portSpeed: N32Gbps

```

FEC: Inactive
Credit Recovery: Inactive
LE domain: 0
Peer beacon: Off
FC Fastwrite: OFF
Interrupts:      0          Link_failure: 0          Frjt:
0
Unknown:        0          Loss_of_sync: 0          Fbsy:
0
Lli:            0          Loss_of_sig: 0
Proc_rqrd:     0          Protocol_err: 0
Timed_out:     0          Invalid_word: 0
Tx_unavail:    0          Invalid_crc: 0
Delim_err:     0          Address_err: 0
Lr_in:         0          0ls_in:      0
Lr_out:        0          0ls_out:    0

```

portloginshow 60

```

Type  PID      World Wide Name      credit df_sz cos
=====

```

portloginshow 60 -history

```

Type  PID      World Wide Name      logout time
=====

```

portregshow 60

LED registers

```

=====
0x81c22000: c4_led_status      00000000      0x81c22004:
c4_led_ctl      00000000

```

FPL registers

```

=====
0x81c20200: fpl_port_config      23490000
0x81c2020c: fpl_port_id_ctl      00000000      0x81c20210:
fpl_port_id_addr      00013c00
0x81c20214: fpl_port_speed      00000004      0x81c2021c:
fpl_lli_ctl      00000903
0x81c20228: fpl_lli_os_ctl      bc95b5b5      0x81c2022c:
fpl_lli_send_word      bc95b5b5
0x81c20230: fpl_lli_mark_rx      00000000      0x81c20234:
fpl_lli_rnd_trip_time      00000000
0x81c20238: fpl_lli_ns_status      00070007      0x81c2023c:
fpl_lli_intr_status      80070007
0x81c20244: fpl_lli_def      00000000      0x81c20254:
fpl_lli_intr_enable_clr      00100000
0x81c20258: fpl_err_intr_status      00000000      0x81c20260:
fpl_err_intr_enable_clr      00000000
0x81c20268: fpl_err_first_error      00000000      0x81c2026c:
fpl_speed_neg_ctl      00000000

```


| | | | |
|-------------|--------------------|----------|-------------|
| 0x81c20270: | fpl_speed_neg_stat | 00000000 | 0x81c20274: |
| | fpl_softasn_ctl | 0000000f | |
| 0x81c20278: | fpl_link_init_ctl | 00000000 | 0x81c2027c: |
| | fpl_link_init_stat | 00000000 | |
| 0x81c20280: | fpl_aec_ctl | 00051060 | 0x81c20284: |
| | fpl_aec_ctl2 | 04009f60 | |
| 0x81c20288: | fpl_pcs_ctl | 00000160 | 0x81c2028c: |
| | fpl_fec_ctl | 00000441 | |
| 0x81c20290: | fpl_fec_cor | 00000000 | 0x81c20294: |
| | fpl_fec_uncor | 00000000 | |
| 0x81c20298: | fpl_hss_link_ctl | 0031f040 | 0x81c2029c: |
| | fpl_afifo_link_ctl | 00000a86 | |
| 0x81c202a0: | fpl_echo_lb_ctl | 0000028c | 0x81c202a4: |
| | fpl_scratch | 00000121 | |
| 0x81c202a8: | fpl_debug | 00030005 | 0x81c202ac: |
| | fpl_misc_debug | 00001800 | |
| 0x00000000: | SW_shadow_reg | 00000000 | 0x00000000: |
| | SW_c4_phyp->cfgptr | 00030000 | |

per-fpg (per octet) registers

=====

| | | | |
|-------------|-------------------------|----------|-------------|
| 0x8180382c: | fpg_serdes_ctla0 | 81a37be7 | 0x81803830: |
| | fpg_serdes_ctla1 | 81a37be7 | |
| 0x81803834: | fpg_serdes_ctlb0 | 81a1c3c3 | 0x81803838: |
| | fpg_serdes_ctlb1 | 81a1c3c3 | |
| 0x8180383c: | fpg_serdes_xgmii_1ms | 00067c28 | 0x81803840: |
| | fpg_serdes_regtimctl | 40e47946 | |
| 0x81803844: | fpg_serdes_asnrsttimctl | 00000102 | |

HSS PLL registers

=====

| | | | |
|-------------|----------------------------|----------|-------------|
| 0x81803400: | 00_hssplla_vco_coarse_cal0 | 00000000 | 0x81803404: |
| | 01_hssplla_vco_coarse_cal1 | 00000014 | |
| 0x81803408: | 02_hssplla_vco_coarse_cal2 | 00000000 | 0x8180340c: |
| | 03_hssplla_vco_coarse_cal3 | 00000000 | |
| 0x81803410: | 04_hssplla_vco_coarse_cal4 | 00000000 | 0x81803424: |
| | 09_hssplla_power_ctl | 00000000 | |
| 0x81803428: | 0A_hssplla_charge_pump_ctl | 00000004 | 0x81803438: |
| | 0E_hssplla_pll_misc_ctl | 00000000 | |
| 0x8180343c: | 0F_hssplla_pclk_ctl | 000000f8 | 0x81803440: |
| | 10_hssplla_eyem_intv_ctl | 00000000 | |
| 0x81803444: | 11_hssplla_eyem_intv_lim1 | 00000000 | 0x81803448: |
| | 12_hssplla_eyem_intv_lim2 | 00000000 | |
| 0x8180344c: | 13_hssplla_eyem_intv_lim3 | 00000000 | 0x81803450: |
| | 14_hssplla_eyem_intv_lim4 | 00000000 | |
| 0x818034f0: | 3C_hssplla_macro_tst_ctl4 | 00000000 | 0x818034f4: |
| | 3D_hssplla_macro_tst_ctl3 | 00000000 | |
| 0x818034f8: | 3E_hssplla_macro_tst_ctl2 | 00000000 | 0x818034fc: |
| | 3F_hssplla_macro_tst_ctl1 | 00000000 | |
| 0x81803500: | 00_hssppll_vco_coarse_cal0 | 0000000a | 0x81803504: |
| | 01_hssppll_vco_coarse_cal1 | 00000014 | |
| 0x81803508: | 02_hssppll_vco_coarse_cal2 | 00000000 | 0x8180350c: |
| | 03_hssppll_vco_coarse_cal3 | 00000000 | |
| 0x81803510: | 04_hssppll_vco_coarse_cal4 | 00000000 | 0x81803524: |

| | | |
|---|----------|-------------|
| 09_hsspll_b_power_ctl | 00000000 | |
| 0x81803528: 0A_hsspll_b_charge_pump_ctl | 00000004 | 0x81803538: |
| 0E_hsspll_b_pll_misc_ctl | 00000000 | |
| 0x8180353c: 0F_hsspll_b_pclk_ctl | 000000f8 | 0x81803540: |
| 10_hsspll_b_eyem_intv_ctl | 00000000 | |
| 0x81803544: 11_hsspll_b_eyem_intv_lim1 | 00000000 | 0x81803548: |
| 12_hsspll_b_eyem_intv_lim2 | 00000000 | |
| 0x8180354c: 13_hsspll_b_eyem_intv_lim3 | 00000000 | 0x81803550: |
| 14_hsspll_b_eyem_intv_lim4 | 00000000 | |
| 0x818035f0: 3C_hsspll_b_macro_tst_ctl4 | 00000000 | 0x818035f4: |
| 3D_hsspll_b_macro_tst_ctl3 | 00000000 | |
| 0x818035f8: 3E_hsspll_b_macro_tst_ctl2 | 00000000 | 0x818035fc: |
| 3F_hsspll_b_macro_tst_ctl1 | 00000000 | |

HSS TX registers

=====

| | | |
|--|----------|-------------|
| 0x81802000: 00_hsstx_cfg_mode_PHY | 00009f48 | 0x81802004: |
| 01_hsstx_test_ctl | 00000000 | |
| 0x81802008: 02_hsstx_coeff_ctl_INV | 00000000 | 0x8180200c: |
| 03_hsstx_drv_mode_ctl | 00000000 | |
| 0x81802010: 04_hsstx_drv_ovrd_ctl | 00000010 | 0x81802014: |
| 05_hsstx_dclk_align_ovrd | 00000080 | |
| 0x81802018: 06_hsstx_imp_cal_ovrd | 00000c0c | 0x8180201c: |
| 07_hsstx_dclk_drift_tol | 00000004 | |
| 0x81802020: 08_hsstx_tap0_coeff_TUNE | 00000000 | 0x81802024: |
| 09_hsstx_tap1_coeff_TUNE | 00000003 | |
| 0x81802028: 0A_hsstx_tap2_coeff_TUNE | 00000018 | 0x8180202c: |
| 0B_hsstx_tap3_coeff_TUNE | 0000000d | |
| 0x81802034: 0D_hsstx_pol_INV | 00000004 | 0x81802038: |
| 0E_hsstx_ae_cmd | 00000000 | |
| 0x8180203c: 0F_hsstx_ae_stat | 00000000 | 0x81802040: |
| 10_hsstx_ae_tap0_TUNE | 00000000 | |
| 0x81802044: 11_hsstx_ae_tap1_TUNE | 00000000 | 0x81802048: |
| 12_hsstx_ae_tap2_TUNE | 00000028 | |
| 0x8180204c: 13_hsstx_ae_tap3_TUNE | 00000000 | 0x81802054: |
| 15_hsstx_app_tune | 0000120e | |
| 0x81802058: 16_hsstx_analog_diag | 00000000 | 0x81802060: |
| 18_hsstx_4x_seg_app | 0000aafa | |
| 0x81802064: 19_hsstx_2x_seg_app | 00000000 | 0x81802068: |
| 1A_hsstx_1x_seg_app | 0000ff5d | |
| 0x8180206c: 1B_hsstx_seg_4x_term_app | 00000000 | 0x81802070: |
| 1C_hsstx_seg_2x1x_term_app | 00000f00 | |
| 0x81802074: 1D_hsstx_tap_sign_app | 00000004 | 0x81802078: |
| 1E_hsstx_ext_addr_data | 00000001 | |
| 0x8180207c: 1F_hsstx_ext_addr_addr | 00000000 | 0x81802080: |
| 20_hsstx_pat_buf_bytes_1_0 | 00000000 | |
| 0x81802084: 21_hsstx_pat_buf_bytes_3_2 | 00000000 | 0x81802088: |
| 22_hsstx_pat_buf_bytes_5_4 | 00000000 | |
| 0x8180208c: 23_hsstx_pat_buf_bytes_7_6 | 00000000 | 0x8180209c: |
| 27_hsstx_8023az_ctl | 00000000 | |
| 0x818020a0: 28_hsstx_dcc_ctl | 000060c0 | 0x818020a4: |
| 29_hsstx_dcc_ovrd | 00000000 | |
| 0x818020a8: 2A_hsstx_dcc_app | 00000086 | 0x818020ac: |
| 2B_hsstx_dcc_timeout | 0000ffff | |

| | | |
|---|----------|-------------|
| 0x818020c0: 30_hsstx_tap_sign_ovrd | 00000000 | 0x818020c8: |
| 32_hsstx_seg_4x_ovrd | 00000000 | |
| 0x818020cc: 33_hsstx_seg_2x_ovrd | 00000000 | 0x818020d0: |
| 34_hsstx_seg_1x_ovrd | 00000000 | |
| 0x818020d8: 36_hsstx_tap_seg_4x_term_ovrd | 00000000 | 0x818020dc: |
| 37_hsstx_tap_seg_2x_term_ovrd | 00000000 | |
| 0x818020e0: 38_hsstx_tap_seg_1x_term_ovrd | 00000000 | 0x818020ec: |
| 3B_hsstx_mac_test_ctl5 | 00000000 | |
| 0x818020f0: 3C_hsstx_mac_test_ctl4 | 00000000 | 0x818020f4: |
| 3D_hsstx_mac_test_ctl3 | 00000000 | |
| 0x818020f8: 3E_hsstx_mac_test_ctl2 | 00000000 | 0x818020fc: |
| 3F_hsstx_mac_test_ctl1 | 000000c6 | |

HSS RX registers

=====

| | | |
|---|----------|-------------|
| 0x81802200: 00_hssrx_cfg_mode_PHY | 00009e78 | 0x81802204: |
| 01_hssrx_test_ctl | 00000000 | |
| 0x81802208: 02_hssrx_phs_rot_ctl | 0000cb80 | 0x8180220c: |
| 03_hssrx_phs_rot_ofs_ctl | 00001610 | |
| 0x81802210: 04_hssrx_phs_rot_posn1 | 00001a18 | 0x81802214: |
| 05_hssrx_phs_rot_posn2 | 00000008 | |
| 0x81802218: 06_hssrx_phs_rot_sta_ofs1 | 00000101 | 0x8180221c: |
| 07_hssrx_phs_rot_sta_ofs2 | 0000001f | |
| 0x81802220: 08_hssrx_dfe_ctl_PHY | 00002002 | 0x81802224: |
| 09_hssrx_dfe_smpl_snap1 | 00000000 | |
| 0x81802228: 0A_hssrx_dfe_smpl_snap2 | 00008000 | 0x8180222c: |
| 0B_hssrx_vga_ctl1 | 00004002 | |
| 0x81802230: 0C_hssrx_vga_ctl2 | 00007aa0 | 0x81802234: |
| 0D_hssrx_vga_ctl3 | 000009e4 | |
| 0x81802238: 0E_hssrx_pwr_mgmt_ctl | 0000001f | 0x8180223c: |
| 0F_hssrx_iqamp_ctl1 | 0000001b | |
| 0x81802240: 10_hssrx_iqamp_ctl2 | 00000007 | 0x81802244: |
| 11_hssrx_dacap_dacan_sel | 00000003 | |
| 0x81802248: 12_hssrx_dacap_dacan | 0000ffff | 0x8180224c: |
| 13_hssrx_daca_min | 00000000 | |
| 0x81802250: 14_hssrx_adac_ctl | 00000000 | 0x81802254: |
| 15_hssrx_ac_cp_ctl | 000031c3 | |
| 0x81802258: 16_hssrx_ac_cp_val | 00008054 | 0x8180225c: |
| 17_hssrx_dfe_h1h2h3_lcl_off_ch | 00000014 | |
| 0x81802260: 18_hssrx_dfe_h1h2h3_lcl_off_val | 00000000 | 0x81802264: |
| 19_hssrx_peaked_intg | 000000ff | |
| 0x81802268: 1A_hssrx_cdr_analog_sw | 0000ce00 | 0x8180226c: |
| 1B_hssrx_peaking_amp_init_c_PHY | 00000000 | |
| 0x81802270: 1C_hssrx_dac_dpc | 00000040 | 0x81802274: |
| 1D_hssrx_ddc | 00000000 | |
| 0x81802278: 1E_hssrx_int_stat_PHY | 00001c0f | 0x8180227c: |
| 1F_hssrx_dfe_func_ctl1_PHY | 0000ffff | |
| 0x81802280: 20_hssrx_dfe_func_ctl2_INV | 00007ebf | 0x81802284: |
| 21_hssrx_ofs_ch_dcc_qcc_idx | 00002000 | |
| 0x81802288: 22_hssrx_dfe_ofs_val | 00007e03 | 0x8180228c: |
| 23_hssrx_h_coeff_bist | 00000405 | |
| 0x81802290: 24_hssrx_ac_cap_bist | 00000000 | 0x81802294: |
| 25_hssrx_max_gain_path_idx_res | 00007800 | |
| 0x81802298: 26_hssrx_loff_ctl | 00000040 | 0x8180229c: |

| | | | |
|--|----------------|-------------|------|
| 27_hssrx_sigdet_ctl | 00002380 | | |
| 0x818022a0: 28_hssrx_ana_ctl_sw | 00000000 | 0x818022a4: | |
| 29_hssrx_intg_dac_ofs | 0000dfe2 | | |
| 0x818022a8: 2A_hssrx_eye_ctl | 00000000 | 0x818022ac: | |
| 2B_hssrx_eye_met | 00000004 | | |
| 0x818022b0: 2C_hssrx_eye_met_err_cnt | 00000000 | 0x818022b4: | |
| 2D_hssrx_eye_met_pdf_eyec | 00000000 | | |
| 0x818022b8: 2E_hssrx_eye_met_pat_len | 0000007f | 0x818022bc: | |
| 2F_hssrx_dfe_func_ctl3 | 0000dfff | | |
| 0x818022c0: 30_hssrx_dfe_tap_ctl_idx_ptr | 00000008 | 0x818022c4: | |
| 31_hssrx_dfe_tap | 00003030 | | |
| 0x818022c8: 32_hssrx_lte_ctl_TUNE | 00001601 | 0x818022e4: | |
| 39_hssrx_int_stat2 | 0000c1ff | | |
| 0x818022e8: 3A_hssrx_ac_cpl_cur_src_adj | 00000042 | 0x818022ec: | |
| 3B_hssrx_dcd_ctl | 00007c41 | | |
| 0x818022f0: 3C_hssrx_dcc_ctl | 00000d00 | 0x818022f4: | |
| 3D_hssrx_qcc_ctl | 00006941 | | |
| 0x818022f8: 3E_hssrx_mac_test_ctl2 | 00000000 | 0x818022fc: | |
| 3F_hssrx_mac_test_ctl1 | 00000000 | | |
| 0x81802248: 12_hssrx_dacap_dacan[02] | | 00fe fffe | |
| 0x81802260: 18_hssrx_dfe_h1h2h3_lcl_off_va[00] | 0000 0000 0000 | 0000 0000 | 0000 |
| 0000 0000 0000 0000 0000 | | | |
| 0x81802260: 18_hssrx_dfe_h1h2h3_lcl_off_va[08] | | 0000 0000 | 0000 |
| 0000 0000 0000 0000 0000 | | | |
| 0x81802260: 18_hssrx_dfe_h1h2h3_lcl_off_va[16] | | 0000 0000 | 0000 |
| 0000 0000 | | | |
| 0x81802288: 22_hssrx_dfe_ofs_val[00][00] | | 7e03 007f | 0b04 |
| 7f7f 0003 007f | | | |
| 0x81802288: 22_hssrx_dfe_ofs_val[03][00] | | 7f7d 0000 | 027d |
| 7f00 017b 7f00 | | | |
| 0x81802288: 22_hssrx_dfe_ofs_val[06][00] | | 0476 0001 | 7d05 |
| 007f 7c7f 0000 | | | |
| 0x81802288: 22_hssrx_dfe_ofs_val[09][00] | | 7d0b 007f | 7d79 |
| 0000 037d 0000 | | | |
| 0x81802288: 22_hssrx_dfe_ofs_val[12][00] | | 0305 007f | 7d7d |
| 0000 0206 007f | | | |
| 0x81802288: 22_hssrx_dfe_ofs_val[15][00] | | 7b04 0000 | 7c08 |
| 0000 7b04 007f | | | |
| 0x81802288: 22_hssrx_dfe_ofs_val[18][00] | | 7805 007f | 7d00 |
| 0000 007e 0000 | | | |
| 0x81802288: 22_hssrx_dfe_ofs_val[21][00] | | 007e 0000 | 007e |
| 0000 007e 0000 | | | |
| 0x81802288: 22_hssrx_dfe_ofs_val[24][00] | | 0778 0000 | 7e05 |
| 0000 7f00 0000 | | | |
| 0x81802294: 25_hssrx_max_gain_path_idx_res[00] | | 005d 084e | 1001 |
| 1898 2100 28ba 30a0 3800 | | | |
| 0x81802294: 25_hssrx_max_gain_path_idx_res[08] | | 40d0 48a0 | 508d |
| 5800 6044 6800 70fc 7800 | | | |
| 0x818022c4: 31_hssrx_dfe_tap[00] | | fffef 8080 | 0000 |
| 0000 0030 0030 3030 3030 | | | |
| 0x818022c4: 31_hssrx_dfe_tap[08] | | 3030 3030 | 3030 |
| 0000 | | | |
| 0x818022e8: 3A_hssrx_ac_cpl_cur_src_adj[00] | | 0042 0042 | 0042 |
| 0042 | | | |

```

0x818022ec: 3B_hssrx_dcd_ctl[00]          7c41 5c00   7c85
5c00   7c82
0x818022f0: 3C_hssrx_dcc_ctl[00]          0d00 0d81   0d83
0d00
0x818022f4: 3D_hssrx_qcc_ctl[00]          6987 6941

```

xfipcs, fec, aec, & aet registers

=====

```

0x81c20400: xfipcs_reg          [00] 00002040 00000080 00000000
00000000 00000001 00000008 00000000 00000000
0x81c20420: xfipcs_reg          [08] 00008c01 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c20440: xfipcs_reg          [16] 00000000 00000000 00000000
00000000 00000040 00000000 00000000 00000000
0x81c20460: xfipcs_reg          [24] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c20480: xfipcs_reg          [32] 00000004 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c20620: fec_32g_128g_reg   [08] 00000000 00000000 00000000
00000000 00000000 00000000 00000000
0x81c20648: fec_32g_128g_reg   [18] 00000000 00000000 00000000
00000000 00000000 00000000 00000000
0x81c20a00: aec_reg            [00] 00000000 00000000 00000000
00000000 00000000 00000000 00000000
0x81c20c00: aet_reg            [00] 00000000 00000000 00000000
00000000 00000000

```

bbc registers

=====

```

0x81c21800: bbc_trc            0 0 0 0 0 0 0
0
0x81c21840: bbc_trc            0 0 0 0 0 0 0
0
0x81c21880: bbc_trc            0 0 0 0 0 0 0
0
0x81c218c0: bbc_trc            0 0 0 0 0 0 0
0
0x81c21900: bbc_trc            0 0 0 0 0 0 0
0
0x81c21804: bbc_mbc            0 0 0 0 0 0 0
0
0x81c21844: bbc_mbc            0 0 0 0 0 0 0
0
0x81c21884: bbc_mbc            0 0 0 0 0 0 0
0
0x81c218c4: bbc_mbc            0 0 0 0 0 0 0
0
0x81c21904: bbc_mbc            0 0 0 0 0 0 0
0
0x81c21a00: bbc_rcc            0 0 0 0 0 0 0
0
0x81c21a20: bbc_rcc            0 0 0 0 0 0 0
0
0x81c21a40: bbc_rcc            0 0 0 0 0 0 0

```

```

0
0x81c21a60: bbc_rcc          0  0  0  0  0  0  0
0
0x81c21a80: bbc_rcc          0  0  0  0  0  0  0
0
0x81c21c00: bbc_rqc          0  0  0  0  0  0  0
0
0x81c21c20: bbc_rqc          0  0  0  0  0  0  0
0
0x81c21c40: bbc_rqc          0  0  0  0  0  0  0
0
0x81c21c60: bbc_rqc          0  0  0  0  0  0  0
0
0x81c21c80: bbc_rqc          0  0  0  0  0  0  0
0
0x81c21d00: bbc_fbpc        00000000  0x81c21d04: bbc_csc
00000000
0x81c21d08: bbc_rcc_inc     00000000  0x81c21d0c:
bbc_rqc_inc       00000000
0x81c21d10: bbc_fbpc_inc    00000000  0x81c21d14:
bbc_tmc_inc       00000000
0x81c21d18: bbc_threshold   00080100  0x81c21d1c:
bbc_counter_clr   00000000
0x81c21d20: bbc_debug_en    00000000  0x81c21d24: bbc_ctrl
00200020
0x81c21d28: bbc_rqc_rcc_thresh 00000055  0x81c21d34:
bbc_bb_sc_n       00000000
0x81c21d38: bbc_crd_reco_debug 00000000  0x81c21d3c:
bbc_crd_reco_debug_data 00000000
0x81c21d40: bbc_multi_frm_loss_cnt 00000000  0x81c21d44:
bbc_multi_rdy_loss_cnt 00000000
0x81c21d48: bbc_1frm_loss_recov_cnt 00000000  0x81c21d4c:
bbc_1rdy_loss_recov_cnt 00000000
0x81c21d58: bbc_int_status  00000000  0x81c21d5c:
bbc_int_set       00000000
0x81c21d60: bbc_int_first   00000000  0x81c21d64:
bbc_frm_rdy_rx_err_addr 00000000
0x81c21d68: bbc_frm_rdy_tx_err_addr 00000000  0x81c21d6c:
bbc_trc_mbc_err_addr 00000000
0x81c21d70: bbc_frm_rdy_rx_dbl_ecc 00000000  0x81c21d74:
bbc_frm_rdy_tx_dbl_ecc 00000000
0x81c21d78: bbc_trc_mbc_dbl_ecc 00000000
0x81c21d7c: bbc_fsm_status  00001011  0x81c21d80:
bbc_force_err     00000000
0x81c21d84: bbc_crdr_avail0  ffffffff  0x81c21d88:
bbc_crdr_avail1   000000ff
0x81c21d8c: bbc_scratch     00000000

FPS registers
=====
0x81c20004: fps_er_enc_in   00000000  0x81c20008:
fps_er_crc        00000000
0x81c2000c: fps_er_trunc    00000000  0x81c20010:
fps_er_toolong    00000000

```

```

0x81c20014: fps_er_bad_eof          00000000    0x81c20018:
fps_er_enc_out          00000000
0x81c2001c: fps_er_bad_os            00000000    0x81c20020:
fps_er_flush           00000000
0x81c20024: fps_er_ifg              00000000    0x81c20038:
fps_er_crc_good_eof    00000000
0x81c2003c: fps_inv_arb            00000000    0x81c20040:
fps_slow_sts_status    00000000
0x81c20044: fps_tx_frm_cnt        00000000    0x81c20048:
fps_rx_frm_cnt         00000000
0x81c20050: fps_tx_word_cnt_hi    00000000    0x81c2004c:
fps_tx_word_cnt_lo     00000000
0x81c20058: fps_rx_word_cnt_hi    00000000    0x81c20054:
fps_rx_word_cnt_lo     00000000

```

BAL registers

=====

```

0x81c27000: bal_desired_buf        00000000    0x81c27004:
bal_alloc_buf          00000000
0x81c27008: bal_busy_buf           00000000    0x81c2700c:
bal_usable_buf         00000000
0x81c27010: bal_max_bor_buf       00000000
0x81c27014: bal_busy_buf_thresh   00000002

```

TXQ registers

=====

```

0x81c23004: txq_phys_port_ctl     00440000
0x81c23050: txq_link_skew         00000000
0x81c23068: txq_cr_lk_dttm_intr_sts [00] 00000000 00000000
0x81c23070: txq_cr_lk_dttm_intr_en [00] 00000000 00000000
0x81c23024: txq_disc_frm_trap_cnt 00000014

```

FDS registers

=====

```

0x81c24000: fds_rxf_ctl           00000002    0x81c24004:
fds_rxf_wait_thresh    00000909
0x81c24018: fds_rxf_first_error    00000000    0x81c2401c:
fds_rxf_first_error_info 00000000
0x81c24020: fds_rxf_inout_pkt_cnt  00000000
0x81c24008: fds_rxf_err_int_status 00000000    0x81c24024:
fds_rxf_fifo_status    00888888
0x81c25000: fds_txf_ctl           0000003a    0x81c25004:
fds_txf_wait_ifg_thresh 00a00106
0x81c25008: fds_txf_err_int_status 00000000    0x81c25024:
fds_txf_fifo_status    00088888
0x81c2502c: fds_txf_bbc_scs       00000000

```

Logical TXQ registers

=====

```

0x81c23000: txq_log_port_ctl     00000002    0x81c23008:
txq_port_status        00000000
0x81c2300c: txq_todo_flags        [00] 00000000 00000000
0x81c23014: txq_spd_match_desc    [00] 00000000 00000000 00000000
00000000

```

```

0x81c23024: txq_spd_match_desc      [04] 00000014
0x81c23028: txq_vc_weight            [00] 01010101 01010101 01010101
01010101
0x81c23038: txq_vc_weight            [04] 01010101 01010101 01010101
01010101
0x81c23048: txq_vc_weight            [08] 01010101 00010101
0x81c23054: txq_cong_dttm_ctrl      00000000
0x81c23058: txq_cong_dttm_intr_sts      [00] 00000000 00000000
0x81c23060: txq_cong_dttm_intr_en      [00] 00000000 00000000
0x81c23078: txq_bw_limit_en_reg      [00] 00000000 00000000
0x81c23080: txq_bw_gua_en_reg            [00] 00000000 00000000
0x81c23088: txq_vc_group                [00] 03030300 03030303 03030303
03030303
0x81c23098: txq_vc_group                [04] 03030303 03030303 03030303
03030303
0x81c230a8: txq_vc_group                [08] 03030303 03030303 00000000
00000000
0x81c230b0: txq_bw_thresh_group      [00] 00000000 00000000 00000000
00000000
0x81c230c0: txq_bw_thresh_group      [04] 00000000 00000000 00000000
00000000
0x81c230d0: txq_bw_thresh_group      [08] 00000000 00000000 00000000
00000000
0x81c230e0: txq_bw_thresh_group      [12] 00000000 00000000 00000000
00000000
0x81c230f0: txq_bw_thresh_group      [16] 00000000 00000000 00000000
00000000
0x81c23100: txq_bw_thresh_group      [20] 00000000 00000000 00000000
00000000
0x81c23110: txq_bw_thresh_group      [24] 00000000 00000000 00000000
00000000
0x81c23120: txq_bw_thresh_group      [28] 00000000 00000000 00000000
00000000
0x81c23130: txq_bw_thresh_group      [32] 00000000 00000000 00000000
00000000
0x81c23140: txq_bw_thresh_group      [36] 00000000 00000000 00000000
00000000

```

txq Congestion detection Statistics RAM

=====

```

0x81090280: vc[0]          00000000      0x81090284: vc[1]
00000000
0x81090288: vc[2]          00000000      0x8109028c: vc[3]
00000000
0x81090290: vc[4]          00000000      0x81090294: vc[5]
00000000
0x81090298: vc[6]          00000000      0x8109029c: vc[7]
00000000
0x810902a0: vc[8]          00000000      0x810902a4: vc[9]
00000000
0x810902a8: vc[10]         00000000     0x810902ac: vc[11]
00000000
0x810902b0: vc[12]         00000000     0x810902b4: vc[13]
00000000

```


| | | |
|--------------------|----------|--------------------|
| 0x810902b8: vc[14] | 00000000 | 0x810902bc: vc[15] |
| 00000000 | | |
| 0x810902c0: vc[16] | 00000000 | 0x810902c4: vc[17] |
| 00000000 | | |
| 0x810902c8: vc[18] | 00000000 | 0x810902cc: vc[19] |
| 00000000 | | |
| 0x810902d0: vc[20] | 00000000 | 0x810902d4: vc[21] |
| 00000000 | | |
| 0x810902d8: vc[22] | 00000000 | 0x810902dc: vc[23] |
| 00000000 | | |
| 0x810902e0: vc[24] | 00000000 | 0x810902e4: vc[25] |
| 00000000 | | |
| 0x810902e8: vc[26] | 00000000 | 0x810902ec: vc[27] |
| 00000000 | | |
| 0x810902f0: vc[28] | 00000000 | 0x810902f4: vc[29] |
| 00000000 | | |
| 0x810902f8: vc[30] | 00000000 | 0x810902fc: vc[31] |
| 00000000 | | |
| 0x81090300: vc[32] | 00000000 | 0x81090304: vc[33] |
| 00000000 | | |
| 0x81090308: vc[34] | 00000000 | 0x8109030c: vc[35] |
| 00000000 | | |
| 0x81090310: vc[36] | 00000000 | 0x81090314: vc[37] |
| 00000000 | | |
| 0x81090318: vc[38] | 00000000 | 0x8109031c: vc[39] |
| 00000000 | | |

Logical STS registers

=====

| | | |
|----------------------------------|----------------------------|------------------------------|
| 0x81584384: sts_ftb_type1_miss | 00000000 | |
| 0x81584388: sts_ftb_type2_miss | 00000000 | |
| 0x8158438c: sts_ftb_type6_miss | 00000000 | |
| 0x81584390: sts_hard_zoning_miss | 00000000 | |
| 0x81584394: sts_lun_zoning_miss | 00000000 | |
| 0x8158439c: sts_unroutable | 00000000 | |
| 0x815813b4: sts_rte_cl2 | 00000000 | 0x815813b8: |
| sts_rte_cl3 | 00000000 | 0x815813bc: sts_rte_link_ctl |
| 00000000 | 0x815843a8: sts_tx_timeout | 00000000 |

Logical STS filter registers

=====

| | | | | |
|-------------------------|------|----------|----------|----------|
| 0x81584300: stsflt_trig | [00] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584310: stsflt_trig | [04] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584320: stsflt_trig | [08] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584330: stsflt_trig | [12] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584340: stsflt_trig | [16] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584350: stsflt_trig | [20] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |

```

0x81584360: sts_flt_trig      [24] 00000000 00000000 00000000
00000000
0x81584370: sts_flt_trig      [28] 00000000 00000000 00000000
00000000
0x81584380: sts_flt_trig      [32]

```

Logical STS discard registers

=====

```

0x815815d0: disc_mcast_wka      00000000      0x815815d4:
disc_inv_did      00000000
0x815815d8: disc_cl1_cl4      00000000      0x815815dc:
disc_sid_chk_fail 00000000
0x815815e0: disc_inv_dom_egid_txpt 00000000      0x815815e4:
disc_vft_hop_cnt_1 00000000
0x815815e8: disc_classf      00000000      0x815815ec:
disc_fcp_cdb_inv  00000000
0x815815f0: disc_vfid_trap_enabled 00000000      0x815815f4:
disc_vfid_hdr_chk_fail 00000000
0x815815f8: disc_shim_cksum_fail 00000000      0x815815fc:
disc_fed_edit_cmd_err 00000000
0x81581600: disc_ftb_vm_mode 00000000      0x81581604:
disc_ftb_agnt2_miss 00000000
0x81581608: disc_ecb_reserved 00000000      0x8158160c:
disc_ecb_de_pad_err 00000000
0x81581610: disc_ecb_de_tag_err 00000000      0x81581614:
disc_ecb_de_seq_err 00000000
0x81581618: disc_ecb_err      00000000      0x8158161c:
disc_ftb_type4_match 00000000
0x81581620: disc_fcp_rsp_ftb_type4 00000000      0x81581624:
disc_ftb_type5_match 00000000
0x81581628: disc_ftb_type3_match 00000000      0x8158162c:
disc_els_ftb_type3 00000000
0x81581630: disc_ftb_type1_match 00000000      0x81581634:
disc_els_rsp_ex_port 00000000
0x81581638: disc_inv_drp_dps  00000000      0x8158163c:
disc_did_lookup_miss 00000000
0x81581640: disc_ftb_type2_match 00000000      0x81581644:
disc_trpd_plogi_pdisc 00000000
0x81581648: disc_type2_lookup_miss 00000000      0x8158164c:
disc_ftb_type6_match 00000000
0x81581650: disc_els_rep_ex_port 00000000      0x81581654:
disc_els_sid_lkup_bit1 00000000
0x81581658: disc_els_sid_lkup_bit0 00000000      0x8158165c:
disc_bls_frm_trap_bit1 00000000
0x81581660: disc_ftb_token_err 00000000      0x81581664:
disc_asic_internal_err 00000000
0x81581668: disc_hard_zone_miss 00000000      0x8158166c:
disc_lun_zone_miss 00000000
0x81581670: disc_flt_frame_disc 00000000      0x81581674:
disc_flt_parity_err 00000000
0x81581678: disc_frame_marked_du 00000000      0x8158167c:
disc_frame_marked_to 00000000
0x81581680: disc_lkup_rte_prty_err 00000000

```

```

portstatsshow 60
stat_wtx          0          4-byte words transmitted
stat_wrx          0          4-byte words received
stat_ftx          0          Frames transmitted
stat_frx          0          Frames received
stat_c2_frx       0          Class 2 frames received
stat_c3_frx       0          Class 3 frames received
stat_lc_rx        0          Link control frames
received
stat_mc_rx        0          Multicast frames
received
stat_mc_to        0          Multicast timeouts
stat_mc_tx        0          Multicast frames
transmitted
tim_txcrd_z       0          Time TX Credit Zero
(2.5Us ticks)
tim_txcrd_z_vc   0- 3: 0          0          0          0
tim_txcrd_z_vc   4- 7: 0          0          0          0
tim_txcrd_z_vc   8-11: 0         0          0          0
tim_txcrd_z_vc  12-15: 0         0          0          0
lat_tot_pkt_vc   0- 3: 1          1          1          1
lat_tot_pkt_vc   4- 7: 1          1          1          1
lat_tot_pkt_vc   8-11: 1          1          1          1
lat_tot_pkt_vc  12-15: 1          1          1          1
lat_hi_time_vc   0- 3: 0          0          0          0
lat_hi_time_vc   4- 7: 0          0          0          0
lat_hi_time_vc   8-11: 0          0          0          0
lat_hi_time_vc  12-15: 0          0          0          0
lat_lo_time_vc   0- 3: 1          1          1          1
lat_lo_time_vc   4- 7: 1          1          1          1
lat_lo_time_vc   8-11: 1          1          1          1
lat_lo_time_vc  12-15: 1          1          1          1
max_latency_vc   0- 3: 1          1          1          1
max_latency_vc   4- 7: 1          1          1          1
max_latency_vc   8-11: 1          1          1          1
max_latency_vc  12-15: 1          1          1          1
latency_dma_ts   09-09-2024 UTC Mon 08:47:26          TXQ
Latency DMA TimeStamp
fec_cor_detected  0          Count of blocks that
were corrected by FEC
fec_uncor_detected 0          Count of blocks that
were left uncorrected by FEC
er_enc_in        0          Encoding errors inside
of frames
er_crc           0          Frames with CRC errors
er_trunc         0          Frames shorter than
minimum
er_toolong       0          Frames longer than
maximum
er_bad_eof       0          Frames with bad end-of-
frame
er_enc_out       0          Encoding error outside
of frames

```

| | | |
|--------------------------|-----------------------------|--------------------------|
| er_bad_os | 0 | Invalid ordered set |
| er_pcs_blk | 0 | PCS block errors |
| er_rx_c3_timeout | 0 | Class 3 receive frames |
| discarded due to timeout | | |
| er_tx_c3_timeout | 0 | Class 3 transmit frames |
| discarded due to timeout | | |
| er_unroutable | 0 | Frames that are |
| unroutable | | |
| er_unreachable | 0 | Frame with unreachable |
| destination | | |
| er_other_discard | 0 | Other discards |
| er_type1_miss | 0 | frames with FTB type 1 |
| miss | | |
| er_type2_miss | 0 | frames with FTB type 2 |
| miss | | |
| er_type6_miss | 0 | frames with FTB type 6 |
| miss | | |
| er_zone_miss | 0 | frames with hard zoning |
| miss | | |
| er_lun_zone_miss | 0 | frames with LUN zoning |
| miss | | |
| er_crc_good_eof | 0 | Crc error with good eof |
| er_inv_arb | 0 | Invalid ARB |
| er_single_credit_loss | 0 | Single vcrdy/frame loss |
| on link | | |
| er_multi_credit_loss | 0 | Multiple vcrdy/frame |
| loss on link | | |
| other_credit_loss | 0 | Link timeout/complete |
| credit loss | | |
| phy_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | Timestamp of |
| phy_port stats clear | | |
| lgc_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | Timestamp of |
| lgc_port stats clear | | |
| fec_corrected_rate | 0 | FEC Corrected blocks per |
| second | | |

portstats64show 60

| | | |
|---------------|---|--|
| stat64_wtx | 0 | top_int : 4-byte words transmitted |
| | 0 | bottom_int : 4-byte words transmitted |
| stat64_wrx | 0 | top_int : 4-byte words received |
| | 0 | bottom_int : 4-byte words received |
| stat64_ftx | 0 | top_int : Frames transmitted |
| | 0 | bottom_int : Frames transmitted |
| stat64_frx | 0 | top_int : Frames received |
| | 0 | bottom_int : Frames received |
| stat64_c2_frx | 0 | top_int : Class 2 frames received |
| | 0 | bottom_int : Class 2 frames received |
| stat64_c3_frx | 0 | top_int : Class 3 frames received |
| | 0 | bottom_int : Class 3 frames received |
| stat64_lc_rx | 0 | top_int : Link control frames received |
| | 0 | bottom_int : Link control frames |
| received | | |
| stat64_mc_rx | 0 | top_int : Multicast frames received |
| | 0 | bottom_int : Multicast frames received |

| | | |
|---|---|--|
| stat64_mc_to | 0 | top_int : Multicast timeouts |
| | 0 | bottom_int : Multicast timeouts |
| stat64_mc_tx | 0 | top_int : Multicast frames transmitted |
| | 0 | bottom_int : Multicast frames |
| transmitted | | |
| tim64_rdy_pri | 0 | top_int : Time R_RDY high priority |
| | 0 | bottom_int : Time R_RDY high priority |
| tim64_txcrd_z | 0 | top_int : Time BB_credit zero |
| | 0 | bottom_int : Time BB_credit zero |
| er64_enc_in | 0 | top_int : Encoding errors inside of |
| frames | | |
| | 0 | bottom_int : Encoding errors inside of |
| frames | | |
| er64_crc | 0 | top_int : Frames with CRC errors |
| | 0 | bottom_int : Frames with CRC errors |
| er64_trunc | 0 | top_int : Frames shorter than minimum |
| | 0 | bottom_int : Frames shorter than minimum |
| er64_toolong | 0 | top_int : Frames longer than maximum |
| | 0 | bottom_int : Frames longer than maximum |
| er64_bad_eof | 0 | top_int : Frames with bad end-of-frame |
| | 0 | bottom_int : Frames with bad end-of- |
| frame | | |
| er64_enc_out | 0 | top_int : Encoding error outside of |
| frames | | |
| | 0 | bottom_int : Encoding error outside of |
| frames | | |
| er64_disc_c3 | 0 | top_int : Class 3 frames discarded |
| | 0 | bottom_int : Class 3 frames discarded |
| er64_pcs_blk | 0 | top_int : PCS block errors |
| | 0 | bottom_int : PCS block errors |
| stat64_rateTxFrame | 0 | Tx frame rate (fr/sec) |
| stat64_rateRxFrame | 0 | Rx frame rate (fr/sec) |
| stat64_rateTxPeakFrame | 0 | Tx peak frame rate (fr/sec) |
| stat64_rateRxPeakFrame | 0 | Rx peak frame rate (fr/sec) |
| stat64_rateTxWord | 0 | Tx Word rate (words/sec) |
| stat64_rateRxWord | 0 | Rx Word rate (words/sec) |
| stat64_rateTxPeakWord | 0 | Tx peak Word rate (words/sec) |
| stat64_rateRxPeakWord | 0 | Rx peak Word rate (words/sec) |
| stat64_PRJTFrames | 0 | top_int : Number of PRJT frames |
| returned to this port | | |
| | 0 | bottom_int : Number of PRJT |
| frames returned to this port | | |
| stat64_PBSYFrames | 0 | top_int : Number of PBSY frames |
| returned to this port | | |
| | 0 | bottom_int : Number of PBSY |
| frames returned to this port | | |
| stat64_inputBuffersFull | 0 | top_int : Number of occurrences |
| when all input buffers full | | |
| | 0 | bottom_int : Number of |
| occurrences when all input buffers full | | |
| stat64_rxClass1Frames | 0 | top_int : Number of class 1 |
| frames received | | |
| | 0 | bottom_int : Number of class 1 |
| frames received | | |

```

stat64_aveTxFrameSize  0          Average Tx Frame size
stat64_aveRxFrameSize  0          Average Rx Frame size
Lr_in                  0          top_int
                        0          bottom_int
Ols_in                 0          top_int
                        0          bottom_int
Lr_out                 0          top_int
                        0          bottom_int
Ols_out                0          top_int
                        0          bottom_int
Link_failure           0          top_int
                        0          bottom_int
Invalid_CRC            0          top_int
                        0          bottom_int
Invalid_word           0          top_int
                        0          bottom_int
Protocol_err           0          top_int
                        0          bottom_int
Loss_of_sig            0          top_int
                        0          bottom_int
Loss_of_sync           0          top_int
                        0          bottom_int
er_bad_os              0          top_int : Invalid ordered set
                        0          bottom_int: Invalid ordered set

```

```

portrouteshow 60
port address ID: 0x013c00
external unicast routing table:
  0: Embedded
 255: Embedded
internal unicast routing table:
  0: Embedded

```

```
portcamshow 60
```

```

-----
Port  SID used  DID used  SID entries  DID entries
60    0          0          000000      000000
-----

```

```
ptbufshow, ptcreditshow, ptdatashow, ptstatsshow 60
```

```

S:
S:VF Enable:          1
S:
S:C4 Global Variable:
S:-----
-----
S:trace_stop:        0
S:
S:C4 Phy Data Pointers: c4_phyp = 0xb6ab9040
S:-----
-----
S:tnodep              0xbb82f7e0      pt
      0x43028004

```

```

S:proto_phyph          0xb88066c0      phy_cfg
0xb6aba080
S:c4_chp                0x97e28000      c4_lgcp
0x97f58000
S:c4_phy_regp          0x81c20000      proc_dir
0xb85138c0
S:-----
-----
S:magic_id              0xc4345678      num_port_timer    12
S:prev_if_id           0x43020004      S:ftx              0
    tov              0
S:initialized          0                port_idx           4
S:ui_idx               60              slot_no
    0
S:blade_idx            4                sw_usr_ports       400
S:unused               0                intr_debounced
    0
S:aec_status           0x0              reason_code
    0
S:debug                0x00000004      debug_trc_line     0
S:rxbuf_list_head     0xffffffff      rxbuf_list_tail
0xffffffff
S:isAePort             0                port_misc_data
    0
S:num_fault1_rx_disc   0                num_fault2_rx_disc 0
S:p_ll_i_cause0        0                p_sig_regained     0
S:p_sync_regained      0                enc_out
    0x0
S:cached_fps_status    0                cached_sts_status  0
S:cached_er_crc_good_eof 0
S:cached_er_bad_os     0                cached_er_too_long 0
S:cached_er_trunc      0
cached_tot_er_crc_good_eof 0
S:num_pt_excess_intr   0                num_no_fid         0
S:num_fault1_cnt       0                num_fault2_cnt
    0
S:num_fault_lip        0                num_fault_ll_i     0
S:num_fault_rx_fifo    0                num_fault_hss      0
S:num_fault_bwait      0                lli_intr_prim
    0
S:num_sw_link_to       0
be_link_err_mon_count 0
S:ecb_enc_enabled      0                ecb_comp_enabled
    0
S:ecb_rsv_enc          0                ecb_rsv_comp       0
S:ecb_enc_bm           0x0              ecb_key_index
0xffffffff
S:fab_idx              4
S:num_be_lto           0                lto_count_reset_intvl
    0
S:lr_count_reset_intvl 0                num_be_lr
    0
S:num_fault_qsfp       0                check_lto
    0

```

```

S:credit_loaded          0          num_credit_overrun
   0
S:fec_enabled            0x0          fec_los_to_flag          0x0
S:phy_stats_clear_ts    1725611419      pcs_err_online
   0
S:pcs_err_light_det     0          pcs_err_ignore
   0
S:pcs_blk_err           0          pcs_hiber                0
S:phy_port_status       0          ecb_enc_lr_count
   0
S:dport_mode            0          avoid_lto_det           0
S:sn_debounced          0x0          sn_started_kr_reqd      0
S:major_timer_started   0x0          ready_bm                0x0
S:parln_1_bm            0x0          parln_0_bm              0x0
S:be_los_of_sync_event_intvl
be_los_of_sync_event    0
S:errataPtenable_cntr   0          errataPoll_cntr
   0
S:jda_rx_sig_loss_det   0          jda_rx_sig_loss_cnt
   0
S:encrypt_blk_error     0
S:
S:      c4_trunk
S:=====
S:mark_ts                0x0          deskew                  0x0
S:master_phyp            0x0
S:
S:adelay[00]: 0x00000000 0x00000000 0x00000000 0x00000000
S:adelay[04]: 0x00000000 0x00000000 0x00000000 0x00000000
S:
S:      c4_buf
S:=====
S:tx_csc                  0          rx_csc
   0
S:ld_vc_credits          0          tx_flag                  0x0
S:alloc_buffers          0          req_buffers              0
S:est_buffers            20          ld_use_est               0
S:bb_sc_n                 0          rx_bb_sc_n
   0
S:data_cr                 5          nondata_cr
   6
S:cr_enable              0
S:ld_nondata_cr          6          tnodep
0xbb82f8c0
S:tx_credits[0] 0      0      0      0      0      0      0      0
S:tx_credits[8] 0      0      0      0      0      0      0      0
S:tx_credits[16]      0      0      0      0      0      0      0      0
S:tx_credits[24]      0      0      0      0      0      0      0      0
S:tx_credits[32]      0      0      0      0      0      0      0      0
S:rx_credits[0] 0      0      0      0      0      0      0
S:rx_credits[8] 0      0      0      0      0      0
S:rx_credits[16]      0      0      0      0      0      0      0      0
S:rx_credits[24]      0      0      0      0      0      0      0      0
S:rx_credits[32]      0      0      0      0      0      0      0      0

```



```

S:tx_mbc[0]      0      0      0      0      0      0      0      0
S:tx_mbc[8]     0      0      0      0      0      0      0      0
S:tx_mbc[16]    0      0      0      0      0      0      0      0
S:tx_mbc[24]    0      0      0      0      0      0      0      0
S:tx_mbc[32]    0      0      0      0      0      0      0      0
S:rx_mbc[0]     0      0      0      0      0      0      0      0
S:rx_mbc[8]     0      0      0      0      0      0      0      0
S:rx_mbc[16]    0      0      0      0      0      0      0      0
S:rx_mbc[24]    0      0      0      0      0      0      0      0
S:rx_mbc[32]    0      0      0      0      0      0      0      0

```

S:

S:C4 Chip Variables: c4_phyp->c4_chp = 0x97e28000

S:-----

S:version = 2.1

S:magic_id 0xc4234567 init_state 0x8

S:reset_reg_mem 0x1

S:ch_int0_en_bm 0x0 intr0_cause 0x0

S:ch_int1_en_bm 0x0 intr1_cause 0x0

S:ch_int2_en_bm 0x0 intr2_cause 0x0

S:ch 0x43010080 ch_cfg

0xb7013ba0

S:raslog_hdl.hndl 0x0 obj_halted 0x0

S:c4_chip_regp 0x80000000 c4_fpg_regp

0x81800000

S:num_chip_timer 0x5

S:hi_task_bm 0x0 lo_task_bm 0x0

S:c4_deferq.q_head 0x0 c4_deferq.q_tail 0x0

S:c4_tmrq.q_head 0x0 c4_tmrq.q_tail 0x0

slot_no 0

S:chip_inst 0 chip_idx 0

S:pll_initialized 1

pll_serdes_initialized 1

S:init_tries 0 init_ptEnableBM

0xba01b488

S:tick_polling 0xb980c9c0 sec_polling

0xb980c960

S:bb_fid 129

S:ecb_key_bm[0] 0x0 ecb_key_bm[1] 0x0

S:ecb_key_bm[2] 0x0 ecb_key_bm[3] 0x0

S:is_chip_enc_enabled 0

is_chip_comp_enabled 0x0

S:ftb_rsrcp->ftb_flags 0x0 act_rsrcp->act_flag 0x1

S:lue_rsrcp->lue_flags[0] 0x0 lue_rsrcp-

>lue_flags[1] 0x0

S:c4_phyp[00]: 0xb6ab0000 0xb6ab2080 0xb6ab4100 0xb6ab6180

S:c4_phyp[04]: 0xb6ab9040 0xb6abb0c0 0xb6abd140 0xb6ac0000

S:c4_phyp[08]: 0xb6ac2080 0xb6ac4100 0xb6ac6180 0xb6ac9040

S:c4_phyp[12]: 0xb6acb0c0 0xb6acd140 0xb6ad0000 0xb6ad2080

S:c4_phyp[16]: 0xb6ad4100 0xb6ad6180 0xb6ad9040 0xb6adb0c0

S:c4_phyp[20]: 0xb6add140 0xb6ae0000 0xb6ae2080 0xb6ae4100

S:c4_phyp[24]: 0xb6ae6180 0xb6ae9040 0xb6aeb0c0 0xb6aed140

S:c4_phyp[28]: 0xb6af0000 0xb6af2080 0xb6af4100 0xb6af6180

S:c4_phyp[32]: 0xb6af9040 0xb6afb0c0 0xb6afd140 0xb6b00000

```

S:c4_phyp[36]: 0xb6b02080 0xb6b04100 0xb6b06180 0xb6b09040
S:c4_phyp[40]: 0xb6b0b0c0 0xb6b0d140 0xb6b10000 0xb6b12080
S:c4_phyp[44]: 0xb6b14100 0xb6b16180 0xb6b19040 0xb6b1b0c0
S:c4_phyp[48]: 0xb6b1d140 0xb6b20000 0xb6b22080 0xb6b24100
S:c4_phyp[52]: 0xb6b26180 0xb6b29040 0xb6b2b0c0 0xb6b2d140
S:c4_phyp[56]: 0xb6b30000 0xb6b32080 0xb6b34100 0xb6b36180
S:c4_phyp[60]: 0xb6b39040 0xb6b3b0c0 0xb6b3d140 0xb6b40000
S:c4_lgcp[00]: 0x97f48000 0x97f4c000 0x97f50000 0x97f54000
S:c4_lgcp[04]: 0x97f58000 0x97f5c000 0x97f60000 0x97f64000
S:c4_lgcp[08]: 0x97f68000 0x97f6c000 0x97f70000 0x97f74000
S:c4_lgcp[12]: 0x97f78000 0x97f7c000 0x97f80000 0x97f84000
S:c4_lgcp[16]: 0x97f88000 0x97f8c000 0x97f90000 0x97f94000
S:c4_lgcp[20]: 0x97f98000 0x97f9c000 0x97fa0000 0x97fa4000
S:c4_lgcp[24]: 0x97fa8000 0x97fac000 0x97fb0000 0x97fb4000
S:c4_lgcp[28]: 0x97fb8000 0x97fbc000 0x97fc0000 0x97fc4000
S:c4_lgcp[32]: 0x97fc8000 0x97fcc000 0x97fd0000 0x97fd4000
S:c4_lgcp[36]: 0x97fd8000 0x97fdc000 0x97fe0000 0x97fe4000
S:c4_lgcp[40]: 0x97fe8000 0x97fec000 0x97ff0000 0x97ff4000
S:c4_lgcp[44]: 0x97ff8000 0x97ffc000 0x8e000000 0x8e004000
S:c4_lgcp[48]: 0x8e008000 0x8e00c000 0x8e010000 0x8e014000
S:c4_lgcp[52]: 0x8e018000 0x8e01c000 0x8e020000 0x8e024000
S:c4_lgcp[56]: 0x8e028000 0x8e02c000 0x8e030000 0x8e034000
S:c4_lgcp[60]: 0x8e038000 0x8e03c000 0x8e040000 0x8e044000
S:chip_timers[00]: 0xb980c720 0xb980c780 0xb980c7e0 0xb980c840
S:chip_timers[04]: 0xb980c8a0 0xb980c900
S:disc_trap_enable_required      0x0                rxlp_disc_log_stop
                                0x0
S:curr_rxlp_frm_cnt              0x0                curr_rxlp_disc_frm_cnt  0x0
S:sw_disc_frm_cnt                0x0                last_disc_frm_cnt       0x0
S:txq_nopop_pr_cnt              0x0                pollErrataDfe_ptBM
0xba01b4b0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][0]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][1] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][2]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][0] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][1]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][2] 0x0
S:
S:C4 Logical Port Variables
S:-----
-----
S:c4_lgc_regp                    0x81c20000
S:c4_phyp:
S:      0xb6ab9040              0x0                0x0                0x0

S:      0x0                    0x0                0x0                0x0

S:master_phyp                   0xb6ab9040        if_id
0x43020004
S:min_phyp                      0x0                max_phyp           0x0
S:num_phy_ports                 1                  lgc_num            4
S:num_iu_to                     0                  sw_txq_bm
0
S:port_fid                      129                unused             0

```

```

S:port_group          0          lgc_stats_clear_ts
                    1725611419
S:domain_tbl_sel     0          area_tbl_sel
                    0
S:egid_tbl_sel       0
S:serv_lo_bm         0x0
S:
S:Proto Phy Variables:
S:-----
-----
S:magic_id           0xc4123456   asic_phyp
0xb6ab9040
S:port_id            0x43028004   phy_cfg
                    0xb6aba080
S:upsm_hdl           0xb8010500   physm_hdl
0xb8010280
S:ov_snsn_hdl        0xb8010140   sw_snsn_hdl
0xb80101e0
S:ov_lksm_hdl        0xb8010320   sw_lksm_hdl
0xb80103c0
S:trksm_hdl          0xb8010460   lr_flag          0x0
S:lr_active          0x0          qsfp_txxrx_rate_sel
                    0x0
S:
S:UPSM              UP00: UPST_PORT_DISABLED   --> UP00: UPST_PORT_DISABLED
S:SNSM(OV)          SN00: OV_SNST_STOPPED       --> SN00: OV_SNST_STOPPED
S:SNSM(SW)          SW00: SW_SNST_STAGE_WS   --> SW00: SW_SNST_STAGE_WS
S:PHYSM             PP00: PHYST_STOPPED      --> PP00: PHYST_STOPPED
S:LKSM(OV)          LK00: OV_LKST_INACTIVE   --> LK00: OV_LKST_INACTIVE
S:LKSM(SW)          SW13: INACTIVE          --> SW13: INACTIVE
S:TRKSM             TRK0: TRKST_INIT        --> TRK0: TRKST_INIT
S:
S:physm variables:
S:-----
-----
S:proto_phyp         0xb88066c0   physm_hdl
0xb8010280
S:force_offline     0          copper          0
S:fault_reason       0: UNKNOWN
S:phy_media_present  0
S:
S:snsn variables:
S:-----
-----
S:speed              0xff          proto_phyp
0xb88066c0
S:hw_sn_tries_left  0x0          sw_sn_tries_left  0x0
S:curr_txsp_count    0x0
S:tx_max             0x0          curr_tx_indx
                    0x0
S:curr_tx            0x0          curr_rxsp_count
                    0x0
S:rx_max             0x0          curr_rx_indx
                    0x0

```

```

S:curr_rx          0x0          rx_mem
   0x0
S:rxsp_rec_count  0x0
S:nc_start        0x0          tx_start          0x0
S:sync_start      0x0          sync_present      0x0
S:diag_auto       0x0          diag_speed        0xff
S:striped_wd_tov  3000          hw_wd_tov
   3000
S:step            0x0          qsfp28_speed_mode
   0x0
S:qsfp_mode0_hw_sn_tries_left  0x0
S:qsfp_mode1_hw_sn_tries_left  0x0
S:
S:lksm variables:
S:-----
-----
S:proto_phyp      0xb88066c0    ov_lksm_hdl
0xb8010320
sw_lksm_hdl       0xb80103c0
num_lf1           0
S:hw_link_tries_left  0          sw_link_tries_left  0
S:buf_ptype       0x0          stored_entry_state  0x6
S:handshake_owner 0x0          0x0          mark_unsent
   0x0
S:busybuf_stuck   0x0          lr_wait           0x0
S:
S:trksm variables:
S:-----
-----
S:Not a trunk port
S:
S:upsm variables:
S:-----
-----
S:proto_phyp      0xb88066c0    upsm_hdl
0xb8010500
S:bb_credits      0          port_beacon        0
S:port_diag_flag  0          0          force_offline
   0
S:port_fault_rsn          0: PORT_NO_FAULT
S:retry_init_rsn          0: UNKNOWN
S:linit_reason          0          linit_result        0
S:ie_fctl_mode          0          fec_in_sync_tries_left  0
S:retry_sn_fail_init    0
retry_link_fail_init    0
S:excess_lr_count      0
S:
S:c4_ch_cfg
S:-----
-----
S:c4_desc_ring_size  256          292          256          256          292
292          2          292          292
S:thresh_def        0          16          1          0
S:intr_tries        500          cmem_pattern

```

```

0xdeadbeef
S:cmem_pattern_upwd      2          cmem_init_time      16
S:cmem_init_tries      5
S:ctrl_par_thresh      2          data_par_thresh
4
S:cam_par_thresh      4          buf_loss_thresh
12
S:crit_par_thresh      2          non_crit_par_thresh
6
S:pci_abort_thresh     10         pci_err_thresh      5
S:excess_chintr_thresh 8          sw_err_thresh       20
S:err_sample_period    300       intr_sleep
20000
S:frame_timeout        2500      proxy_dev           16384
S:vf_route             81920     qos                 2048
S:stats                2048      f_redirect          2048
S:rsp_trap             2048      lun_zoning          20480
S:area_mode            0         ftb_max_loop[0]    0
S:ftb_max_loop[1]      6         ftb_max_loop[2]    9
S:ftb_max_loop[3]      10        ftb_max_loop[4]    10
S:ftb_max_loop[5]      5         ftb_max_loop[6]    6
S:ftb_seg_size[0]      0         ftb_seg_size[1]
16384
S:ftb_seg_size[2]      65536    ftb_seg_size[3]
16384
S:ftb_seg_size[4]      16384    ftb_seg_size[5]
65536
S:ftb_seg_size[6]      16384    ftb_seg_base[0]    0
S:ftb_seg_base[1]      0         ftb_seg_base[2]
65536
S:ftb_seg_base[3]      16384    ftb_seg_base[4]
32768
S:ftb_seg_base[5]      131072   ftb_seg_base[6]
49152
asic_err_monitor_period1 300
asic_err_monitor_period2 86400
zone_chk_to_poll_period 25
zone_chk_class2_reject_tov 220
S:
S:c4_phy_cfg
S:-----
-----

```

```

S:version = 2.1
S:pt                   0x43028004      fab_ptr
0x9a800000
S:fabattr              0x9a8000d4      fab_iop
0x9a800050
S:cfgbm                0xbb82f624      port_ctrl
0xb6aba098
S:pcap.pcap_bm         0x8d215547      pcap.pcap2_bm
0x2588289
S:pcap.pcap3_bm        0x1bebe0c
ui_idx                 60              S:slot_no
0

```

```

is_icl 0 S:sw_usr_ports 400
S:neg_speed 0 0 0 0 0 0
S:my_domain 0x1 port_mode 0x0
S:hw_sn_maxtries 100 sw_sn_maxtries
0
S:hw_link_maxtries 10 sw_link_maxtries 5
S:rx_cyc_tov 28 rttov 300
S:bufrdy_tov 300 busybuf_tov 286
S:mark_tov 300 lksm_tov 3000
S:buf_dealloc_wait 4 hw_wd_tov 3000
S:hw_lk_train_tov 540 hw_lk_test_tov
150
S:syswait_tx_12_lips 1 lip_rx_tov 55
S:al_time_tov 15 lp_tov 2000
S:intr_tries_port 500 intr_mod_debounce
250
S:intr_lsrflt_debounce 500 intr_efifo_debounce 100
S:port_no_fid 3 excess_ptintr_thresh 8
S:port_fault1_thresh 100 port_fault1_spur_thresh 250
S:port_fault1_disc_thresh 500
port_fault1_disc_spur_thresh 1000
S:port_fault2_thresh 5 losync_tov 100
S:port_sw_link_to 15 en_8g_scramble
1
frc_hw_sn_mode 0x1
S:enc_poll_thresh 0 fec_enable
0
S:fec_in_sync_to 50 fec_in_sync_try_max
4
S:port_be_lto_threshold 100 port_be_lr_threshold
2
S:be_cr_in_sync_to 5
port_credit_overrun_thresh 10
S:jda_sfp_losig_tov 400
jda_sfp_losig_try_max 30
S:striped_wd_tov 3000
no_sync_debounce 1200
S:
S: fab_iop
S:=====
S:fab_iop->interop_mode 0x0 fab_iop->lab_mode 0x0
S:fab_iop->fl_bbc 0x0 fab_iop->fl_fan
0x0
S:fab_iop->fl_cls 0x4 fab_iop->fl_rscn
0x0
S:fab_iop->domain_id_offset 0x60 fab_iop-
>mcdt_fabric_mode 0x0
S:fab_iop->mcdt_default_zone 0x0 fab_iop-
>mcdt_safe_zone 0x0
S:
S: port_ctrl
S:=====
S:port_ctrl.port_type 1 port_ctrl.port_grp 0
S:port_ctrl.port_number 60 port_ctrl.vc_mode 1

```

```

S:
S:      port_ctrl.lcap
S:=====
S:has_serdes          0          has_media          1
S:topology            1          skip_nego         0
S:skip_pnego         0          skip_init_event  0
S:en_shim            0          speed_neg        0
S:      1
S:loop_back          0          num_speeds       5
S:fec_enable         0
S:
S:      port_ctrl.speed_list array
S:=====
S:speed_list[0].auto_neg  1    speed_list[0].lnk_speed  0x0000000a
S:speed_list[1].auto_neg  1    speed_list[1].lnk_speed  0x00000008
S:speed_list[2].auto_neg  1    speed_list[2].lnk_speed  0x00000006
S:speed_list[3].auto_neg  1    speed_list[3].lnk_speed  0x00000005
S:speed_list[4].auto_neg  1    speed_list[4].lnk_speed  0x00000003
S:speed_list[5].auto_neg  0    speed_list[5].lnk_speed  0x00000000
S:
S:      port_ctrl.cm
S:=====
S:port_ctrl.cm.num_vcs          8
S:port_ctrl.cm.min_bufs        8
S:port_ctrl.cm.cr_shar_bufs    0
S:port_ctrl.vc_alloc
S:port_ctrl.vc_alloc          2 0 1 1 1 1 1 1
S:port_ctrl.vc_alloc          0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.norm_vc_alloc
S:port_ctrl.norm_vc_alloc     4 0 5 5 5 5 1 1
S:port_ctrl.norm_vc_alloc     0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.cm.skip_bb_credit          0
S:port_ctrl.cm.use_shim_based_sublist          0
S:
S:      port_ctrl.serdes_set
S:=====
S:serdes_type          0x8
S:serdes_data_t.ibm_hss_serdes.tx_drive_power          0x1
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b_sign     0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b         0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_a         0x0
S:serdes_data_t.ibm_hss_serdes.rxeq                   0x0
S:
S:      cfgbm
S:=====
S:old_distance          0x0          gport_lockdown          0x0
S:tport                0x1          speed                    0x0
S:disable_eport        0x0          fcacc                    0x0
S:lport_lockdown       0x0          priv_lport_lockdown     0x0
S:      0x0
S:vcxlt_linit          0x0          delay_flogi             0x0
S:isl_interop          0x0          distance                 0x0

```

```

S:BufStarvFlag          0x0          credit_sharing          0x0
S:lport_halfduplex     0x0          lport_fairness         0x0
S:soft_neg              0x0          asn_frc_hwretry        0x0
S:cr_recov              0x0          fport_buffers          0x0
S:export                0x0          export_mode            0x0
S:csctl_en              0x0          mirror_port            0x0
S:fault_delay           0x0          non_dfe                 0x0
S:fec_configured*(0=ENAB) 0          fec_tts                 0
S:port_persistently_disabled (permanently) 0 (0)
S:
S:      cfg property
S:=====
S:priv_pcfg_bm          0x00000000      lgcl_pcfg_bm
0xbb82f664
S:fport_buffer          0x00000000
S:
S:
S:C4 Discard Cntrs: rxlp_stats = 0xb6ab93f0
S:-----
-----
S:disc_mcast_wka        0x0          disc_inv_did           0x0
S:disc_cl1_cl4          0x0          disc_sid_chk_fail      0x0
S:disc_inv_dom_egid_txpt 0x0          disc_vft_hop_cnt_1
0x0
S:disc_classf           0x0          disc_fcp_cdb_inv       0x0
S:disc_vfid_trap_enabled 0x0          0x0
disc_vfid_hdr_chk_fail 0x0
S:disc_shim_cksum_fail  0x0          disc_fed_edit_cmd_err  0x0
S:disc_shim_cksum_fail  0x0          disc_fed_edit_cmd_err  0x0
S:disc_ftb_vm_mode      0x0          disc_ftb_agn_t2_miss   0x0
S:disc_ecb_de_pad_err   0x0          disc_ecb_de_tag_err    0x0
S:disc_ecb_de_seq_err   0x0          disc_ecb_err            0x0
S:disc_ftb_type4_match  0x0          disc_fcp_rsp_ftb_type4 0x0
S:disc_fcp_rsp_ftb_type4 0x0          disc_ftb_type5_match
0x0
S:disc_ftb_type3_match  0x0          disc_els_ftb_type3     0x0
S:disc_ftb_type1_match  0x0          disc_els_rsp_ex_port   0x0
S:disc_inv_drp_dps      0x0          disc_did_lookup_miss   0x0
S:disc_ftb_type2_match  0x0          disc_trpd_plogi_pdisc  0x0
S:disc_type2_lookup_miss 0x0          disc_ftb_type6_match
0x0
S:disc_els_rep_ex_port  0x0          disc_els_sid_lkup_bit1 0x0
S:disc_els_sid_lkup_bit0 0x0          0x0
disc_bls_frm_trap_bit1 0x0
S:disc_ftb_token_err    0x0          disc_asic_internal_err 0x0
S:disc_hard_zone_miss   0x0          disc_lun_zone_miss     0x0
S:disc_flt_frame_disc   0x0          disc_flt_parity_err    0x0
S:disc_frame_marked_du  0x0          disc_frame_marked_to   0x0
E:Connection type: FE
E:Port type: E_port
E:Trunk port: No
E:Configured Speed: AUTO_SPEED_NEGO

```


E:Max Capable Speed: 32G
E:Current SNSM Speed: UNDEFINED
E:Hardware TX Speed: 32G (0x00000004)
E:Hardware RX Speed: 32G (0x00000040)

E:

| | | | |
|-------------------|---|------------------|---|
| E:Interrupts: | 0 | Link_failure: | 0 |
| Loss_of_sync: | 0 | Loss_of_sig: | 0 |
| E:Lli: | 0 | Invalid_word: | 0 |
| E:trapped_frm: | 0 | fwd_status_ok: | 0 |
| E:fwd_timeout: | 0 | fwd_tx_unavail: | 0 |
| E:fwd_unroutable: | 0 | fwd_zone_out: | 0 |
| E:fwd_other_err: | 0 | frm_err_discard: | 0 |
| E:Fltr listA: | 0 | Fltr listB: | 0 |
| E:Zone trap fwd: | 0 | Zone trap disc: | 0 |
| E:shim_csum: | 0 | RTE_perr: | 0 |
| E:Invalid_crc: | 0 | Delim_err: | 0 |
| E:Protocol_err: | 0 | | |
| E:Lr_in: | 0 | Lr_out: | 0 |
| E:Ols_in: | 0 | Ols_out: | 0 |

filterportshow 60

FILTER DATA

Shadow settings:

Filter Enable: 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000

Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass: 0x00000000

Real settings:

Enable RAM: 0x00000000, 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass RAM: 0x00000000

Shadowed filters:

Filter 0: Not Installed (MIRROR1)(LISTA)

c4_fldenable[0] = 0x00000000 0x00000000 0x00000000
0x00000000

c4_fldnegate[0] = 0x00000000, c4_fltr_config[0] = 0x00000000

Filter 1: Not Installed (MIRROR2)(LISTA)

c4_fldenable[1] = 0x00000000 0x00000000 0x00000000
0x00000000

c4_fldnegate[1] = 0x00000000, c4_fltr_config[1] = 0x00000000

Filter 2: Not Installed (MIRROR3)(LISTA)

c4_fldenable[2] = 0x00000000 0x00000000 0x00000000

```
0x00000000
    c4_fldnegate[2] = 0x00000000,c4_fltr_config[2] = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
    c4_fldenable[3] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[3] = 0x00000000,c4_fltr_config[3] = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
    c4_fldenable[4] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[4] = 0x00000000,c4_fltr_config[4] = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
    c4_fldenable[5] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[5] = 0x00000000,c4_fltr_config[5] = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
    c4_fldenable[6] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[6] = 0x00000000,c4_fltr_config[6] = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
    c4_fldenable[7] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[7] = 0x00000000,c4_fltr_config[7] = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
    c4_fldenable[8] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[8] = 0x00000000,c4_fltr_config[8] = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
    c4_fldenable[9] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[9] = 0x00000000,c4_fltr_config[9] = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
    c4_fldenable[10] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[10] = 0x00000000,c4_fltr_config[10] =
0x00000000
Filter 11: Not Installed (SIM)(LISTA)
    c4_fldenable[11] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[11] = 0x00000000,c4_fltr_config[11] =
0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
    c4_fldenable[12] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[12] = 0x00000000,c4_fltr_config[12] =
0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
    c4_fldenable[13] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[13] = 0x00000000,c4_fltr_config[13] =
0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
    c4_fldenable[14] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[14] = 0x00000000,c4_fltr_config[14] =
```

```
0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
    c4_fldenable[15] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[15] = 0x00000000,c4_fltr_config[15] =
0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
    c4_fldenable[16] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[16] = 0x00000000,c4_fltr_config[16] =
0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
    c4_fldenable[17] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[17] = 0x00000000,c4_fltr_config[17] =
0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
    c4_fldenable[18] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[18] = 0x00000000,c4_fltr_config[18] =
0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
    c4_fldenable[19] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[19] = 0x00000000,c4_fltr_config[19] =
0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
    c4_fldenable[20] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[20] = 0x00000000,c4_fltr_config[20] =
0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
    c4_fldenable[21] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[21] = 0x00000000,c4_fltr_config[21] =
0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
    c4_fldenable[22] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[22] = 0x00000000,c4_fltr_config[22] =
0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
    c4_fldenable[23] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[23] = 0x00000000,c4_fltr_config[23] =
0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
    c4_fldenable[24] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[24] = 0x00000000,c4_fltr_config[24] =
0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
    c4_fldenable[25] = 0x00000000 0x00000000 0x00000000
0x00000000
```

```
    c4_fldnegate[25] = 0x00000000,c4_fltr_config[25] =
0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
    c4_fldenable[26] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[26] = 0x00000000,c4_fltr_config[26] =
0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
    c4_fldenable[27] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[27] = 0x00000000,c4_fltr_config[27] =
0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
    c4_fldenable[28] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[28] = 0x00000000,c4_fltr_config[28] =
0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
    c4_fldenable[29] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[29] = 0x00000000,c4_fltr_config[29] =
0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    c4_fldenable[30] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[30] = 0x00000000,c4_fltr_config[30] =
0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    c4_fldenable[31] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[31] = 0x00000000,c4_fltr_config[31] =
0x00000000
```

Real filters:

```
Filter 0: Not Installed (MIRROR1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
```

0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 11: Not Installed (SIM)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 18: Not Installed (PERF3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 19: Not Installed (PERF4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 20: Not Installed (PERF5)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 21: Not Installed (PERF6)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 22: Not Installed (PERF7)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 23: Not Installed (PERF8)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 24: Not Installed (PERF9)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 25: Not Installed (PERF10)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 26: Not Installed (PERF11)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 27: Not Installed (PERF12)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 28: Not Installed (OPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 29: Not Installed (OPM2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 30: Not Installed (IPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 31: Not Installed (IPM2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,

0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter dirty indicator: 0x00000000
Performance filters: 0
Port Mirror filters: 0 (0x0)

FIELD DATA

Shadowed fields:

fldoffset[0] = 0x00, fldmask[0] = 0x00, fldvalue_dyna[0]: 0x00 0x00
0x00 0x00
fldcontrol[0].inuse = 0x0 fldcontrol[0].refcnt = 0x00 0x00 0x00
0x00
fldoffset[1] = 0x00, fldmask[1] = 0x00, fldvalue_dyna[1]: 0x00 0x00
0x00 0x00
fldcontrol[1].inuse = 0x0 fldcontrol[1].refcnt = 0x00 0x00 0x00
0x00
fldoffset[2] = 0x00, fldmask[2] = 0x00, fldvalue_dyna[2]: 0x00 0x00
0x00 0x00
fldcontrol[2].inuse = 0x0 fldcontrol[2].refcnt = 0x00 0x00 0x00
0x00
fldoffset[3] = 0x00, fldmask[3] = 0x00, fldvalue_dyna[3]: 0x00 0x00
0x00 0x00
fldcontrol[3].inuse = 0x0 fldcontrol[3].refcnt = 0x00 0x00 0x00
0x00
fldoffset[4] = 0x00, fldmask[4] = 0x00, fldvalue_dyna[4]: 0x00 0x00
0x00 0x00
fldcontrol[4].inuse = 0x0 fldcontrol[4].refcnt = 0x00 0x00 0x00
0x00
fldoffset[5] = 0x00, fldmask[5] = 0x00, fldvalue_dyna[5]: 0x00 0x00
0x00 0x00
fldcontrol[5].inuse = 0x0 fldcontrol[5].refcnt = 0x00 0x00 0x00
0x00
fldoffset[6] = 0x00, fldmask[6] = 0x00, fldvalue_dyna[6]: 0x00 0x00
0x00 0x00
fldcontrol[6].inuse = 0x0 fldcontrol[6].refcnt = 0x00 0x00 0x00
0x00
fldoffset[7] = 0x00, fldmask[7] = 0x00, fldvalue_dyna[7]: 0x00 0x00
0x00 0x00
fldcontrol[7].inuse = 0x0 fldcontrol[7].refcnt = 0x00 0x00 0x00
0x00
fldoffset[8] = 0x00, fldmask[8] = 0x00, fldvalue_dyna[8]: 0x00 0x00
0x00 0x00
fldcontrol[8].inuse = 0x0 fldcontrol[8].refcnt = 0x00 0x00 0x00
0x00
fldoffset[9] = 0x00, fldmask[9] = 0x00, fldvalue_dyna[9]: 0x00 0x00
0x00 0x00
fldcontrol[9].inuse = 0x0 fldcontrol[9].refcnt = 0x00 0x00 0x00
0x00
fldoffset[10] = 0x00, fldmask[10] = 0x00, fldvalue_dyna[10]: 0x00 0x00


```
0x00 0x00
fldcontrol[10].inuse = 0x0 fldcontrol[10].refcnt = 0x00 0x00 0x00
0x00
fldoffset[11] = 0x00,fldmask[11] = 0x00,fldvalue_dyna[11]:0x00 0x00
0x00 0x00
fldcontrol[11].inuse = 0x0 fldcontrol[11].refcnt = 0x00 0x00 0x00
0x00
fldoffset[12] = 0x00,fldmask[12] = 0x00,fldvalue_dyna[12]:0x00 0x00
0x00 0x00
fldcontrol[12].inuse = 0x0 fldcontrol[12].refcnt = 0x00 0x00 0x00
0x00
fldoffset[13] = 0x00,fldmask[13] = 0x00,fldvalue_dyna[13]:0x00 0x00
0x00 0x00
fldcontrol[13].inuse = 0x0 fldcontrol[13].refcnt = 0x00 0x00 0x00
0x00
fldoffset[14] = 0x00,fldmask[14] = 0x00,fldvalue_dyna[14]:0x00 0x00
0x00 0x00
fldcontrol[14].inuse = 0x0 fldcontrol[14].refcnt = 0x00 0x00 0x00
0x00
fldoffset[15] = 0x00,fldmask[15] = 0x00,fldvalue_dyna[15]:0x00 0x00
0x00 0x00
fldcontrol[15].inuse = 0x0 fldcontrol[15].refcnt = 0x00 0x00 0x00
0x00
fldoffset[16] = 0x00,fldmask[16] = 0x00,fldvalue_dyna[16]:0x00 0x00
0x00 0x00
fldcontrol[16].inuse = 0x0 fldcontrol[16].refcnt = 0x00 0x00 0x00
0x00
fldoffset[17] = 0x00,fldmask[17] = 0x00,fldvalue_dyna[17]:0x00 0x00
0x00 0x00
fldcontrol[17].inuse = 0x0 fldcontrol[17].refcnt = 0x00 0x00 0x00
0x00
fldoffset[18] = 0x00,fldmask[18] = 0x00,fldvalue_dyna[18]:0x00 0x00
0x00 0x00
fldcontrol[18].inuse = 0x0 fldcontrol[18].refcnt = 0x00 0x00 0x00
0x00
fldoffset[19] = 0x00,fldmask[19] = 0x00,fldvalue_dyna[19]:0x00 0x00
0x00 0x00
fldcontrol[19].inuse = 0x0 fldcontrol[19].refcnt = 0x00 0x00 0x00
0x00
```

Real fields:

```
fldoffset RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000
fldmask RAM: 0x00000000, 0x00000000, 0x00000000, 0x00000000,
0x00000000
fld value4 RAM:
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
```

0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000

Field dirty indicator: 0x00000000

FDB reference count fdb: 0 [0 0 0 0]
FDB reference count fdb: 1 [0 0 0 0]
FDB reference count fdb: 2 [0 0 0 0]
FDB reference count fdb: 3 [0 0 0 0]
FDB reference count fdb: 4 [0 0 0 0]
FDB reference count fdb: 5 [0 0 0 0]
FDB reference count fdb: 6 [0 0 0 0]
FDB reference count fdb: 7 [0 0 0 0]
FDB reference count fdb: 8 [0 0 0 0]
FDB reference count fdb: 9 [0 0 0 0]
FDB reference count fdb: 10 [0 0 0 0]
FDB reference count fdb: 11 [0 0 0 0]
FDB reference count fdb: 12 [0 0 0 0]
FDB reference count fdb: 13 [0 0 0 0]
FDB reference count fdb: 14 [0 0 0 0]
FDB reference count fdb: 15 [0 0 0 0]
FDB reference count fdb: 16 [0 0 0 0]
FDB reference count fdb: 17 [0 0 0 0]
FDB reference count fdb: 18 [0 0 0 0]
FDB reference count fdb: 19 [0 0 0 0]

Filter counters:

Filter counter 0: 0 (MIRROR1)
Filter counter 1: 0 (MIRROR2)
Filter counter 2: 0 (MIRROR3)
Filter counter 3: 0 (MIRROR4)
Filter counter 4: 0 (AEPORT_NON_MIRR_DROP)
Filter counter 5: 0 (ZONING TRAP)
Filter counter 6: 0 (FCR_EXPORT_DC)
Filter counter 7: 0 (TIN TRAP)
Filter counter 8: 0 (FICON CUP)
Filter counter 9: 0 (FICON CUP DST)
Filter counter 10: 0 (WELL KNOWN ADDR)
Filter counter 11: 0 (SIM)
Filter counter 12: 0 (UNUSED)
Filter counter 13: 0 (UNUSED)
Filter counter 14: 0 (UNUSED)
Filter counter 15: 0 (UNUSED)
Filter counter 16: 0 (PERF1)

Filter counter 17: 0 (PERF2)
Filter counter 18: 0 (PERF3)
Filter counter 19: 0 (PERF4)
Filter counter 20: 0 (PERF5)
Filter counter 21: 0 (PERF6)
Filter counter 22: 0 (PERF7)
Filter counter 23: 0 (PERF8)
Filter counter 24: 0 (PERF9)
Filter counter 25: 0 (PERF10)
Filter counter 26: 0 (PERF11)
Filter counter 27: 0 (PERF12)
Filter counter 28: 0 (OPM1)
Filter counter 29: 0 (OPM2)
Filter counter 30: 0 (IPM1)
Filter counter 31: 0 (IPM2)

ACL DATA

Logical port 4: Hard Zoning disabled, Soft Zoning disabled
Zone type: WWN Zoning
Frames with hard zone miss: 0

*** Please use filterportshow on user port 56 to display ACL hash
tables and Mirroring resources of thischip.
***We show this data only for the first physical port which is an
external port.

portFcPortCmdShow --slot 0 61 3
doing portFcPortCmdShow: arg1 = 3, arg2 = -2

portshow 61
portDisableReason: None
portCFlags: 0x0
portFlags: 0x4021 PRESENT U_PORT DISABLED LED
LocalSwcFlags: 0x0
portType: 26.0
POD Port: Need license to enable the port
portState: 2 Offline
Protocol: FC
portPhys: 2 No_Module portScn: 2 Offline
port generation number: 0
state transition count: 0

portId: 013d00
portIfId: 43020006
portWwn: 20:3d:d8:1f:cc:2c:99:90
portWwn of device(s) connected:
16b Area list:
Distance: normal
portSpeed: N32Gbps

FEC: Inactive
Credit Recovery: Inactive
LE domain: 0

```

Peer beacon: Off
FC Fastwrite: OFF
Interrupts:      0          Link_failure: 0          Frjt:
0
Unknown:        0          Loss_of_sync: 0         Fbsy:
0
Lli:           0          Loss_of_sig: 0
Proc_rqrd:     0          Protocol_err: 0
Timed_out:     0          Invalid_word: 0
Tx_unavail:    0          Invalid_crc: 0
Delim_err:     0          Address_err: 0
Lr_in:         0          Ols_in:      0
Lr_out:        0          Ols_out:     0

```

portloginshow 61

```

Type  PID      World Wide Name      credit df_sz cos
=====

```

portloginshow 61 -history

```

Type  PID      World Wide Name      logout time
=====

```

portregshow 61

LED registers

=====

```

0x81c32000: c4_led_status      00000000      0x81c32004:
c4_led_ctl      00000000

```

FPL registers

=====

```

0x81c30200: fpl_port_config    23490000
0x81c3020c: fpl_port_id_ctl    00000000      0x81c30210:
fpl_port_id_addr      00013d00
0x81c30214: fpl_port_speed     00000004      0x81c3021c:
fpl_lli_ctl           00000903
0x81c30228: fpl_lli_os_ctl     bc95b5b5      0x81c3022c:
fpl_lli_send_word     bc95b5b5
0x81c30230: fpl_lli_mark_rx    00000000      0x81c30234:
fpl_lli_rnd_trip_time 00000000
0x81c30238: fpl_lli_ns_status  80070007      0x81c3023c:
fpl_lli_intr_status   80070007
0x81c30244: fpl_lli_def        00000000      0x81c30254:
fpl_lli_intr_enable_clr 00100000
0x81c30258: fpl_err_intr_status 00000000      0x81c30260:
fpl_err_intr_enable_clr 00000000
0x81c30268: fpl_err_first_error 00000000      0x81c3026c:
fpl_speed_neg_ctl     00000000
0x81c30270: fpl_speed_neg_stat 00000000      0x81c30274:
fpl_softasn_ctl       0000000f
0x81c30278: fpl_link_init_ctl  00000000      0x81c3027c:

```

```

fpl_link_init_stat      00000000
0x81c30280: fpl_aec_ctl      00051060      0x81c30284:
fpl_aec_ctl2           04009f60
0x81c30288: fpl_pcs_ctl      00000160      0x81c3028c:
fpl_fec_ctl            00000441
0x81c30290: fpl_fec_cor      00000000      0x81c30294:
fpl_fec_uncor          00000000
0x81c30298: fpl_hss_link_ctl      0031f040      0x81c3029c:
fpl_afifo_link_ctl     00000a86
0x81c302a0: fpl_echo_lb_ctl      0000028c      0x81c302a4:
fpl_scratch            00000121
0x81c302a8: fpl_debug          00030005      0x81c302ac:
fpl_misc_debug         00001800
0x00000000: SW_shadow_reg      00000000      0x00000000:
SW_c4_phyp->cfgptr     00030000

```

per-fpg (per octet) registers

```

=====
0x8180382c: fpg_serdes_ctla0      81a37be7      0x81803830:
fpg_serdes_ctla1      81a37be7
0x81803834: fpg_serdes_ctlb0      81a1c3c3      0x81803838:
fpg_serdes_ctlb1      81a1c3c3
0x8180383c: fpg_serdes_xgmii_1ms  00067c28      0x81803840:
fpg_serdes_regtimctl  40e47946
0x81803844: fpg_serdes_asnrsttimctl 00000102

```

HSS PLL registers

```

=====
0x81803400: 00_hssplla_vco_coarse_cal0  00000000      0x81803404:
01_hssplla_vco_coarse_cal1  00000014
0x81803408: 02_hssplla_vco_coarse_cal2  00000000      0x8180340c:
03_hssplla_vco_coarse_cal3  00000000
0x81803410: 04_hssplla_vco_coarse_cal4  00000000      0x81803424:
09_hssplla_power_ctl        00000000
0x81803428: 0A_hssplla_charge_pump_ctl  00000004      0x81803438:
0E_hssplla_pll_misc_ctl     00000000
0x8180343c: 0F_hssplla_pclk_ctl        000000f8      0x81803440:
10_hssplla_eyem_intv_ctl    00000000
0x81803444: 11_hssplla_eyem_intv_lim1    00000000      0x81803448:
12_hssplla_eyem_intv_lim2    00000000
0x8180344c: 13_hssplla_eyem_intv_lim3    00000000      0x81803450:
14_hssplla_eyem_intv_lim4    00000000
0x818034f0: 3C_hssplla_macro_tst_ctl4    00000000      0x818034f4:
3D_hssplla_macro_tst_ctl3    00000000
0x818034f8: 3E_hssplla_macro_tst_ctl2    00000000      0x818034fc:
3F_hssplla_macro_tst_ctl1    00000000
0x81803500: 00_hsspllb_vco_coarse_cal0  0000000a      0x81803504:
01_hsspllb_vco_coarse_cal1  00000014
0x81803508: 02_hsspllb_vco_coarse_cal2  00000000      0x8180350c:
03_hsspllb_vco_coarse_cal3  00000000
0x81803510: 04_hsspllb_vco_coarse_cal4  00000000      0x81803524:
09_hsspllb_power_ctl        00000000
0x81803528: 0A_hsspllb_charge_pump_ctl  00000004      0x81803538:
0E_hsspllb_pll_misc_ctl     00000000

```

| | | |
|--|----------|-------------|
| 0x8180353c: 0F_hsspll_b_pclk_ctl | 000000f8 | 0x81803540: |
| 10_hsspll_b_eyem_intv_ctl | 00000000 | |
| 0x81803544: 11_hsspll_b_eyem_intv_lim1 | 00000000 | 0x81803548: |
| 12_hsspll_b_eyem_intv_lim2 | 00000000 | |
| 0x8180354c: 13_hsspll_b_eyem_intv_lim3 | 00000000 | 0x81803550: |
| 14_hsspll_b_eyem_intv_lim4 | 00000000 | |
| 0x818035f0: 3C_hsspll_b_macro_tst_ctl4 | 00000000 | 0x818035f4: |
| 3D_hsspll_b_macro_tst_ctl3 | 00000000 | |
| 0x818035f8: 3E_hsspll_b_macro_tst_ctl2 | 00000000 | 0x818035fc: |
| 3F_hsspll_b_macro_tst_ctl1 | 00000000 | |

HSS TX registers

=====

| | | |
|--|----------|-------------|
| 0x81802400: 00_hsstx_cfg_mode_PHY | 00009f48 | 0x81802404: |
| 01_hsstx_test_ctl | 00000000 | |
| 0x81802408: 02_hsstx_coeff_ctl_INV | 00000000 | 0x8180240c: |
| 03_hsstx_drv_mode_ctl | 00000000 | |
| 0x81802410: 04_hsstx_drv_ovrd_ctl | 00000010 | 0x81802414: |
| 05_hsstx_dclk_align_ovrd | 00000080 | |
| 0x81802418: 06_hsstx_imp_cal_ovrd | 00000c0c | 0x8180241c: |
| 07_hsstx_dclk_drift_tol | 00000004 | |
| 0x81802420: 08_hsstx_tap0_coeff_TUNE | 00000000 | 0x81802424: |
| 09_hsstx_tap1_coeff_TUNE | 00000003 | |
| 0x81802428: 0A_hsstx_tap2_coeff_TUNE | 00000018 | 0x8180242c: |
| 0B_hsstx_tap3_coeff_TUNE | 0000000d | |
| 0x81802434: 0D_hsstx_pol_INV | 0000000a | 0x81802438: |
| 0E_hsstx_ae_cmd | 00000000 | |
| 0x8180243c: 0F_hsstx_ae_stat | 00000000 | 0x81802440: |
| 10_hsstx_ae_tap0_TUNE | 00000000 | |
| 0x81802444: 11_hsstx_ae_tap1_TUNE | 00000000 | 0x81802448: |
| 12_hsstx_ae_tap2_TUNE | 00000028 | |
| 0x8180244c: 13_hsstx_ae_tap3_TUNE | 00000000 | 0x81802454: |
| 15_hsstx_app_tune | 0000120e | |
| 0x81802458: 16_hsstx_analog_diag | 00000000 | 0x81802460: |
| 18_hsstx_4x_seg_app | 0000aafa | |
| 0x81802464: 19_hsstx_2x_seg_app | 00000000 | 0x81802468: |
| 1A_hsstx_1x_seg_app | 0000ff5d | |
| 0x8180246c: 1B_hsstx_seg_4x_term_app | 00000000 | 0x81802470: |
| 1C_hsstx_seg_2x1x_term_app | 00000f00 | |
| 0x81802474: 1D_hsstx_tap_sign_app | 0000000a | 0x81802478: |
| 1E_hsstx_ext_addr_data | 00000001 | |
| 0x8180247c: 1F_hsstx_ext_addr_addr | 00000000 | 0x81802480: |
| 20_hsstx_pat_buf_bytes_1_0 | 00000000 | |
| 0x81802484: 21_hsstx_pat_buf_bytes_3_2 | 00000000 | 0x81802488: |
| 22_hsstx_pat_buf_bytes_5_4 | 00000000 | |
| 0x8180248c: 23_hsstx_pat_buf_bytes_7_6 | 00000000 | 0x8180249c: |
| 27_hsstx_8023az_ctl | 00000000 | |
| 0x818024a0: 28_hsstx_dcc_ctl | 000060c0 | 0x818024a4: |
| 29_hsstx_dcc_ovrd | 00000000 | |
| 0x818024a8: 2A_hsstx_dcc_app | 0000008c | 0x818024ac: |
| 2B_hsstx_dcc_timeout | 0000ffff | |
| 0x818024c0: 30_hsstx_tap_sign_ovrd | 00000000 | 0x818024c8: |
| 32_hsstx_seg_4x_ovrd | 00000000 | |
| 0x818024cc: 33_hsstx_seg_2x_ovrd | 00000000 | 0x818024d0: |

| | | |
|---|----------|-------------|
| 34_hsstx_seg_1x_ovrd | 00000000 | |
| 0x818024d8: 36_hsstx_tap_seg_4x_term_ovrd | 00000000 | 0x818024dc: |
| 37_hsstx_tap_seg_2x_term_ovrd | 00000000 | |
| 0x818024e0: 38_hsstx_tap_seg_1x_term_ovrd | 00000000 | 0x818024ec: |
| 3B_hsstx_mac_test_ctl5 | 00000000 | |
| 0x818024f0: 3C_hsstx_mac_test_ctl4 | 00000000 | 0x818024f4: |
| 3D_hsstx_mac_test_ctl3 | 00000000 | |
| 0x818024f8: 3E_hsstx_mac_test_ctl2 | 00000000 | 0x818024fc: |
| 3F_hsstx_mac_test_ctl1 | 000000c6 | |

HSS RX registers

=====

| | | |
|---|----------|-------------|
| 0x81802600: 00_hssrx_cfg_mode_PHY | 00009e78 | 0x81802604: |
| 01_hssrx_test_ctl | 00000000 | |
| 0x81802608: 02_hssrx_phs_rot_ctl | 0000cb80 | 0x8180260c: |
| 03_hssrx_phs_rot_ofs_ctl | 00004610 | |
| 0x81802610: 04_hssrx_phs_rot_posn1 | 00002a29 | 0x81802614: |
| 05_hssrx_phs_rot_posn2 | 00000015 | |
| 0x81802618: 06_hssrx_phs_rot_sta_ofs1 | 00000001 | 0x8180261c: |
| 07_hssrx_phs_rot_sta_ofs2 | 00000000 | |
| 0x81802620: 08_hssrx_dfe_ctl_PHY | 00002002 | 0x81802624: |
| 09_hssrx_dfe_smpl_snap1 | 00000000 | |
| 0x81802628: 0A_hssrx_dfe_smpl_snap2 | 00008000 | 0x8180262c: |
| 0B_hssrx_vga_ctl1 | 000041ff | |
| 0x81802630: 0C_hssrx_vga_ctl2 | 00007aa0 | 0x81802634: |
| 0D_hssrx_vga_ctl3 | 000009e4 | |
| 0x81802638: 0E_hssrx_pwr_mgmnt_ctl | 0000001f | 0x8180263c: |
| 0F_hssrx_iqamp_ctl1 | 0000001b | |
| 0x81802640: 10_hssrx_iqamp_ctl2 | 00000006 | 0x81802644: |
| 11_hssrx_dacap_dacan_sel | 00000003 | |
| 0x81802648: 12_hssrx_dacap_dacan | 000000ff | 0x8180264c: |
| 13_hssrx_daca_min | 00000000 | |
| 0x81802650: 14_hssrx_adac_ctl | 00000000 | 0x81802654: |
| 15_hssrx_ac_cp_ctl | 000031c3 | |
| 0x81802658: 16_hssrx_ac_cp_val | 0000804d | 0x8180265c: |
| 17_hssrx_dfe_h1h2h3_lcl_off_ch | 00000014 | |
| 0x81802660: 18_hssrx_dfe_h1h2h3_lcl_off_val | 00000000 | 0x81802664: |
| 19_hssrx_peaked_intg | 000000ff | |
| 0x81802668: 1A_hssrx_cdr_analog_sw | 0000ce00 | 0x8180266c: |
| 1B_hssrx_peaking_amp_init_c_PHY | 00000000 | |
| 0x81802670: 1C_hssrx_dac_dpc | 00000040 | 0x81802674: |
| 1D_hssrx_ddc | 00000000 | |
| 0x81802678: 1E_hssrx_int_stat_PHY | 00000c0f | 0x8180267c: |
| 1F_hssrx_dfe_func_ctl1_PHY | 0000ffff | |
| 0x81802680: 20_hssrx_dfe_func_ctl2_INV | 00007ebf | 0x81802684: |
| 21_hssrx_ofs_ch_dcc_qcc_idx | 00002000 | |
| 0x81802688: 22_hssrx_dfe_ofs_val | 0000017f | 0x8180268c: |
| 23_hssrx_h_coeff_bist | 00000401 | |
| 0x81802690: 24_hssrx_ac_cap_bist | 00000000 | 0x81802694: |
| 25_hssrx_max_gain_path_idx_res | 00007800 | |
| 0x81802698: 26_hssrx_loff_ctl | 00000040 | 0x8180269c: |
| 27_hssrx_sigdet_ctl | 00004580 | |
| 0x818026a0: 28_hssrx_ana_ctl_sw | 00000000 | 0x818026a4: |
| 29_hssrx_intg_dac_ofs | 0000dddd | |

| | | |
|--|----------------|-------------|
| 0x818026a8: 2A_hssrx_eye_ctl | 00000000 | 0x818026ac: |
| 2B_hssrx_eye_met | 00000004 | |
| 0x818026b0: 2C_hssrx_eye_met_err_cnt | 00000000 | 0x818026b4: |
| 2D_hssrx_eye_met_pdf_eyec | 00000000 | |
| 0x818026b8: 2E_hssrx_eye_met_pat_len | 0000007f | 0x818026bc: |
| 2F_hssrx_dfe_func_ctl3 | 0000dfff | |
| 0x818026c0: 30_hssrx_dfe_tap_ctl_idx_ptr | 00000008 | 0x818026c4: |
| 31_hssrx_dfe_tap | 00003030 | |
| 0x818026c8: 32_hssrx_lte_ctl_TUNE | 00001601 | 0x818026e4: |
| 39_hssrx_int_stat2 | 0000c1ff | |
| 0x818026e8: 3A_hssrx_ac_cpl_cur_src_adj | 00000040 | 0x818026ec: |
| 3B_hssrx_dcd_ctl | 00007c49 | |
| 0x818026f0: 3C_hssrx_dcc_ctl | 00000d81 | 0x818026f4: |
| 3D_hssrx_qcc_ctl | 00006988 | |
| 0x818026f8: 3E_hssrx_mac_test_ctl2 | 00000000 | 0x818026fc: |
| 3F_hssrx_mac_test_ctl1 | 00000000 | |
| 0x81802648: 12_hssrx_dacap_dacan[02] | 00ff 00ff | |
| 0x81802660: 18_hssrx_dfe_h1h2h3_lcl_off_va[00] | 0000 0000 0000 | |
| 0000 0000 0000 0000 0000 | | |
| 0x81802660: 18_hssrx_dfe_h1h2h3_lcl_off_va[08] | 0000 0000 0000 | |
| 0000 0000 0000 0000 0000 | | |
| 0x81802660: 18_hssrx_dfe_h1h2h3_lcl_off_va[16] | 0000 0000 0000 | |
| 0000 0000 | | |
| 0x81802688: 22_hssrx_dfe_ofs_val[00][00] | 017f 7f00 7d7d | |
| 0000 797b 0000 | | |
| 0x81802688: 22_hssrx_dfe_ofs_val[03][00] | 7b7f 0000 7d7b | |
| 0000 7d7b 0000 | | |
| 0x81802688: 22_hssrx_dfe_ofs_val[06][00] | 0309 7f7f 7a7b | |
| 0000 7e0c 007f | | |
| 0x81802688: 22_hssrx_dfe_ofs_val[09][00] | 797d 0000 7d00 | |
| 0000 037f 0000 | | |
| 0x81802688: 22_hssrx_dfe_ofs_val[12][00] | 7f7b 0000 7d7d | |
| 0001 797b 0000 | | |
| 0x81802688: 22_hssrx_dfe_ofs_val[15][00] | 017b 0000 0902 | |
| 7f00 7f00 0000 | | |
| 0x81802688: 22_hssrx_dfe_ofs_val[18][00] | 7b7d 0000 047b | |
| 0000 000a 007f | | |
| 0x81802688: 22_hssrx_dfe_ofs_val[21][00] | 000a 007f 000a | |
| 007f 000a 007f | | |
| 0x81802688: 22_hssrx_dfe_ofs_val[24][00] | 097a 0000 077d | |
| 7f00 0179 0000 | | |
| 0x81802694: 25_hssrx_max_gain_path_idx_res[00] | 005b 0849 1100 | |
| 189f 20cf 289f 3084 3800 | | |
| 0x81802694: 25_hssrx_max_gain_path_idx_res[08] | 40af 4885 5074 | |
| 5801 6040 6800 70fe 7800 | | |
| 0x818026c4: 31_hssrx_dfe_tap[00] | fffe 8181 0000 | |
| 0000 0030 0030 3030 3030 | | |
| 0x818026c4: 31_hssrx_dfe_tap[08] | 3030 3030 3030 | |
| 0000 | | |
| 0x818026e8: 3A_hssrx_ac_cpl_cur_src_adj[00] | 0040 0040 0040 | |
| 0040 | | |
| 0x818026ec: 3B_hssrx_dcd_ctl[00] | 7c49 5c00 7c43 | |
| 5c00 7c00 | | |
| 0x818026f0: 3C_hssrx_dcc_ctl[00] | 0d81 0d81 0d41 | |

0d81

0x818026f4: 3D_hssrx_qcc_ctl[00]

6900 6988

xfipcs, fec, aec, & aet registers

=====

```

0x81c30400: xfipcs_reg          [00] 00002040 00000080 00000000
00000000 00000001 00000008 00000000 00000000
0x81c30420: xfipcs_reg          [08] 00008c01 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c30440: xfipcs_reg          [16] 00000000 00000000 00000000
00000000 00000040 00000000 00000000 00000000
0x81c30460: xfipcs_reg          [24] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c30480: xfipcs_reg          [32] 00000004 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c30620: fec_32g_128g_reg    [08] 00000000 00000000 00000000
00000000 00000000 00000000 00000000
0x81c30648: fec_32g_128g_reg    [18] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c30a00: aec_reg             [00] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c30c00: aet_reg             [00] 00000000 00000000 00000000
00000000 00000000

```

bbc registers

=====

```

0x81c31800: bbc_trc              0 0 0 0 0 0 0
0
0x81c31840: bbc_trc              0 0 0 0 0 0 0
0
0x81c31880: bbc_trc              0 0 0 0 0 0 0
0
0x81c318c0: bbc_trc              0 0 0 0 0 0 0
0
0x81c31900: bbc_trc              0 0 0 0 0 0 0
0
0x81c31804: bbc_mbc              0 0 0 0 0 0 0
0
0x81c31844: bbc_mbc              0 0 0 0 0 0 0
0
0x81c31884: bbc_mbc              0 0 0 0 0 0 0
0
0x81c318c4: bbc_mbc              0 0 0 0 0 0 0
0
0x81c31904: bbc_mbc              0 0 0 0 0 0 0
0
0x81c31a00: bbc_rcc              0 0 0 0 0 0 0
0
0x81c31a20: bbc_rcc              0 0 0 0 0 0 0
0
0x81c31a40: bbc_rcc              0 0 0 0 0 0 0
0
0x81c31a60: bbc_rcc              0 0 0 0 0 0 0
0

```

| | | | | | | | |
|-------------------------------------|----------|---|---|---|---|----------------------|---|
| 0x81c31a80: bbc_rcc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c31c00: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c31c20: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c31c40: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c31c60: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c31c80: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c31d00: bbc_fbpc | 00000000 | | | | | 0x81c31d04: bbc_csc | |
| 00000000 | | | | | | | |
| 0x81c31d08: bbc_rcc_inc | 00000000 | | | | | 0x81c31d0c: | |
| bbc_rqc_inc | 00000000 | | | | | | |
| 0x81c31d10: bbc_fbpc_inc | 00000000 | | | | | 0x81c31d14: | |
| bbc_tmc_inc | 00000000 | | | | | | |
| 0x81c31d18: bbc_threshold | 00080100 | | | | | 0x81c31d1c: | |
| bbc_counter_clr | 00000000 | | | | | | |
| 0x81c31d20: bbc_debug_en | 00000000 | | | | | 0x81c31d24: bbc_ctrl | |
| 00200020 | | | | | | | |
| 0x81c31d28: bbc_rqc_rcc_thresh | 00000055 | | | | | 0x81c31d34: | |
| bbc_bb_sc_n | 00000000 | | | | | | |
| 0x81c31d38: bbc_crd_reco_debug | 00000000 | | | | | 0x81c31d3c: | |
| bbc_crd_reco_debug_data | 00000000 | | | | | | |
| 0x81c31d40: bbc_multi_frm_loss_cnt | 00000000 | | | | | 0x81c31d44: | |
| bbc_multi_rdy_loss_cnt | 00000000 | | | | | | |
| 0x81c31d48: bbc_1frm_loss_recov_cnt | 00000000 | | | | | 0x81c31d4c: | |
| bbc_1rdy_loss_recov_cnt | 00000000 | | | | | | |
| 0x81c31d58: bbc_int_status | 00000000 | | | | | 0x81c31d5c: | |
| bbc_int_set | 00000000 | | | | | | |
| 0x81c31d60: bbc_int_first | 00000000 | | | | | 0x81c31d64: | |
| bbc_frm_rdy_rx_err_addr | 00000000 | | | | | | |
| 0x81c31d68: bbc_frm_rdy_tx_err_addr | 00000000 | | | | | 0x81c31d6c: | |
| bbc_trc_mbc_err_addr | 00000000 | | | | | | |
| 0x81c31d70: bbc_frm_rdy_rx_dbl_ecc | 00000000 | | | | | 0x81c31d74: | |
| bbc_frm_rdy_tx_dbl_ecc | 00000000 | | | | | | |
| 0x81c31d78: bbc_trc_mbc_dbl_ecc | 00000000 | | | | | | |
| 0x81c31d7c: bbc_fsm_status | 00001011 | | | | | 0x81c31d80: | |
| bbc_force_err | 00000000 | | | | | | |
| 0x81c31d84: bbc_crdt_avail0 | ffffffff | | | | | 0x81c31d88: | |
| bbc_crdt_avail1 | 000000ff | | | | | | |
| 0x81c31d8c: bbc_scratch | 00000000 | | | | | | |

FPS registers

=====

| | | | | | | | |
|----------------------------|----------|--|--|--|--|-------------|--|
| 0x81c30004: fps_er_enc_in | 00000000 | | | | | 0x81c30008: | |
| fps_er_crc | 00000000 | | | | | | |
| 0x81c3000c: fps_er_trunc | 00000000 | | | | | 0x81c30010: | |
| fps_er_toolong | 00000000 | | | | | | |
| 0x81c30014: fps_er_bad_eof | 00000000 | | | | | 0x81c30018: | |
| fps_er_enc_out | 00000000 | | | | | | |
| 0x81c3001c: fps_er_bad_os | 00000000 | | | | | 0x81c30020: | |

```

fps_er_flush          00000000
0x81c30024: fps_er_ifg          00000000    0x81c30038:
fps_er_crc_good_eof  00000000
0x81c3003c: fps_inv_arb          00000000    0x81c30040:
fps_slow_sts_status  00000000
0x81c30044: fps_tx_frm_cnt          00000000    0x81c30048:
fps_rx_frm_cnt        00000000
0x81c30050: fps_tx_word_cnt_hi        00000000    0x81c3004c:
fps_tx_word_cnt_lo    00000000
0x81c30058: fps_rx_word_cnt_hi        00000000    0x81c30054:
fps_rx_word_cnt_lo    00000000

```

BAL registers

=====

```

0x81c37000: bal_desired_buf          00000000    0x81c37004:
bal_alloc_buf          00003fff
0x81c37008: bal_busy_buf            00003fff    0x81c3700c:
bal_usable_buf          00000000
0x81c37010: bal_max_bor_buf          00000000
0x81c37014: bal_busy_buf_thresh        00000002

```

TXQ registers

=====

```

0x81c33004: txq_phys_port_ctl          00460000
0x81c33050: txq_link_skew              00000000
0x81c33068: txq_cr_lk_dttm_intr_sts [00] 00000000 00000000
0x81c33070: txq_cr_lk_dttm_intr_en [00] 00000000 00000000
0x81c33024: txq_disc_frm_trap_cnt      00000014

```

FDS registers

=====

```

0x81c34000: fds_rxf_ctl                00000002    0x81c34004:
fds_rxf_wait_thresh    00000909
0x81c34018: fds_rxf_first_error          00000000    0x81c3401c:
fds_rxf_first_error_info 00000000
0x81c34020: fds_rxf_inout_pkt_cnt        00000000
0x81c34008: fds_rxf_err_int_status        00000000    0x81c34024:
fds_rxf_fifo_status      00888888
0x81c35000: fds_txf_ctl                0000003a    0x81c35004:
fds_txf_wait_ifg_thresh 00a00106
0x81c35008: fds_txf_err_int_status        00000000    0x81c35024:
fds_txf_fifo_status      00088888
0x81c3502c: fds_txf_bbc_scs            00000000

```

Logical TXQ registers

=====

```

0x81c33000: txq_log_port_ctl          00000002    0x81c33008:
txq_port_status          00000000
0x81c3300c: txq_todo_flags              [00] 00000000 00000000
0x81c33014: txq_spd_match_desc          [00] 00000000 00000000 00000000
00000000
0x81c33024: txq_spd_match_desc          [04] 00000014
0x81c33028: txq_vc_weight              [00] 01010101 01010101 01010101
01010101

```

```

0x81c33038: txq_vc_weight      [04] 01010101 01010101 01010101
01010101
0x81c33048: txq_vc_weight      [08] 01010101 00010101
0x81c33054: txq_cong_dttm_ctrl    00000000
0x81c33058: txq_cong_dttm_intr_sts   [00] 00000000 00000000
0x81c33060: txq_cong_dttm_intr_en     [00] 00000000 00000000
0x81c33078: txq_bw_limit_en_reg       [00] 00000000 00000000
0x81c33080: txq_bw_gua_en_reg         [00] 00000000 00000000
0x81c33088: txq_vc_group             [00] 03030300 03030303 03030303
03030303
0x81c33098: txq_vc_group             [04] 03030303 03030303 03030303
03030303
0x81c330a8: txq_vc_group             [08] 03030303 03030303 00000000
00000000
0x81c330b0: txq_bw_thresh_group     [00] 00000000 00000000 00000000
00000000
0x81c330c0: txq_bw_thresh_group     [04] 00000000 00000000 00000000
00000000
0x81c330d0: txq_bw_thresh_group     [08] 00000000 00000000 00000000
00000000
0x81c330e0: txq_bw_thresh_group    [12] 00000000 00000000 00000000
00000000
0x81c330f0: txq_bw_thresh_group    [16] 00000000 00000000 00000000
00000000
0x81c33100: txq_bw_thresh_group    [20] 00000000 00000000 00000000
00000000
0x81c33110: txq_bw_thresh_group    [24] 00000000 00000000 00000000
00000000
0x81c33120: txq_bw_thresh_group    [28] 00000000 00000000 00000000
00000000
0x81c33130: txq_bw_thresh_group    [32] 00000000 00000000 00000000
00000000
0x81c33140: txq_bw_thresh_group    [36] 00000000 00000000 00000000
00000000

```

txq Congestion detection Statistics RAM

=====

```

0x810903c0: vc[0]          00000000      0x810903c4: vc[1]
00000000
0x810903c8: vc[2]          00000000      0x810903cc: vc[3]
00000000
0x810903d0: vc[4]          00000000      0x810903d4: vc[5]
00000000
0x810903d8: vc[6]          00000000      0x810903dc: vc[7]
00000000
0x810903e0: vc[8]          00000000      0x810903e4: vc[9]
00000000
0x810903e8: vc[10]         00000000      0x810903ec: vc[11]
00000000
0x810903f0: vc[12]         00000000      0x810903f4: vc[13]
00000000
0x810903f8: vc[14]         00000000      0x810903fc: vc[15]
00000000
0x81090400: vc[16]         00000000      0x81090404: vc[17]

```

```

00000000
0x81090408: vc[18]      00000000      0x8109040c: vc[19]
00000000
0x81090410: vc[20]      00000000      0x81090414: vc[21]
00000000
0x81090418: vc[22]      00000000      0x8109041c: vc[23]
00000000
0x81090420: vc[24]      00000000      0x81090424: vc[25]
00000000
0x81090428: vc[26]      00000000      0x8109042c: vc[27]
00000000
0x81090430: vc[28]      00000000      0x81090434: vc[29]
00000000
0x81090438: vc[30]      00000000      0x8109043c: vc[31]
00000000
0x81090440: vc[32]      00000000      0x81090444: vc[33]
00000000
0x81090448: vc[34]      00000000      0x8109044c: vc[35]
00000000
0x81090450: vc[36]      00000000      0x81090454: vc[37]
00000000
0x81090458: vc[38]      00000000      0x8109045c: vc[39]
00000000

```

Logical STS registers

=====

```

0x81584504: sts_ftb_type1_miss  00000000
0x81584508: sts_ftb_type2_miss  00000000
0x8158450c: sts_ftb_type6_miss  00000000
0x81584510: sts_hard_zoning_miss 00000000
0x81584514: sts_lun_zoning_miss 00000000
0x8158451c: sts_unroutable      00000000
0x81581534: sts_rte_cl2         00000000      0x81581538:
sts_rte_cl3           00000000      0x8158153c: sts_rte_link_ctl
00000000      0x81584528: sts_tx_timeout      00000000

```

Logical STS filter registers

=====

```

0x81584480: stsflt_trig [00] 00000000 00000000 00000000
00000000
0x81584490: stsflt_trig [04] 00000000 00000000 00000000
00000000
0x815844a0: stsflt_trig [08] 00000000 00000000 00000000
00000000
0x815844b0: stsflt_trig [12] 00000000 00000000 00000000
00000000
0x815844c0: stsflt_trig [16] 00000000 00000000 00000000
00000000
0x815844d0: stsflt_trig [20] 00000000 00000000 00000000
00000000
0x815844e0: stsflt_trig [24] 00000000 00000000 00000000
00000000
0x815844f0: stsflt_trig [28] 00000000 00000000 00000000

```

00000000
0x81584500: sts_flt_trig [32]

Logical STS discard registers

=====

| | | |
|------------------------------------|----------|-------------|
| 0x815818b8: disc_mcast_wka | 00000000 | 0x815818bc: |
| disc_inv_did | 00000000 | |
| 0x815818c0: disc_cl1_cl4 | 00000000 | 0x815818c4: |
| disc_sid_chk_fail | 00000000 | |
| 0x815818c8: disc_inv_dom_egid_txpt | 00000000 | 0x815818cc: |
| disc_vft_hop_cnt_1 | 00000000 | |
| 0x815818d0: disc_classf | 00000000 | 0x815818d4: |
| disc_fcp_cdb_inv | 00000000 | |
| 0x815818d8: disc_vfid_trap_enabled | 00000000 | 0x815818dc: |
| disc_vfid_hdr_chk_fail | 00000000 | |
| 0x815818e0: disc_shim_cksum_fail | 00000000 | 0x815818e4: |
| disc_fed_edit_cmd_err | 00000000 | |
| 0x815818e8: disc_ftb_vm_mode | 00000000 | 0x815818ec: |
| disc_ftb_agnt2_miss | 00000000 | |
| 0x815818f0: disc_ecb_reserved | 00000000 | 0x815818f4: |
| disc_ecb_de_pad_err | 00000000 | |
| 0x815818f8: disc_ecb_de_tag_err | 00000000 | 0x815818fc: |
| disc_ecb_de_seq_err | 00000000 | |
| 0x81581900: disc_ecb_err | 00000000 | 0x81581904: |
| disc_ftb_type4_match | 00000000 | |
| 0x81581908: disc_fcp_rsp_ftb_type4 | 00000000 | 0x8158190c: |
| disc_ftb_type5_match | 00000000 | |
| 0x81581910: disc_ftb_type3_match | 00000000 | 0x81581914: |
| disc_els_ftb_type3 | 00000000 | |
| 0x81581918: disc_ftb_type1_match | 00000000 | 0x8158191c: |
| disc_els_rsp_ex_port | 00000000 | |
| 0x81581920: disc_inv_drp_dps | 00000000 | 0x81581924: |
| disc_did_lookup_miss | 00000000 | |
| 0x81581928: disc_ftb_type2_match | 00000000 | 0x8158192c: |
| disc_trpd_plogi_pdisc | 00000000 | |
| 0x81581930: disc_type2_lookup_miss | 00000000 | 0x81581934: |
| disc_ftb_type6_match | 00000000 | |
| 0x81581938: disc_els_rep_ex_port | 00000000 | 0x8158193c: |
| disc_els_sid_lkup_bit1 | 00000000 | |
| 0x81581940: disc_els_sid_lkup_bit0 | 00000000 | 0x81581944: |
| disc_bls_frm_trap_bit1 | 00000000 | |
| 0x81581948: disc_ftb_token_err | 00000000 | 0x8158194c: |
| disc_asic_internal_err | 00000000 | |
| 0x81581950: disc_hard_zone_miss | 00000000 | 0x81581954: |
| disc_lun_zone_miss | 00000000 | |
| 0x81581958: disc_flt_frame_disc | 00000000 | 0x8158195c: |
| disc_flt_parity_err | 00000000 | |
| 0x81581960: disc_frame_marked_du | 00000000 | 0x81581964: |
| disc_frame_marked_to | 00000000 | |
| 0x81581968: disc_lkup_rte_prty_err | 00000000 | |

portstatsshow 61

stat_wtx

0

4-byte words transmitted

| | | | | |
|------------------------------|------------|-----|-----|-------------------------|
| stat_wrx | 0 | | | 4-byte words received |
| stat_ftx | 0 | | | Frames transmitted |
| stat_frx | 0 | | | Frames received |
| stat_c2_frx | 0 | | | Class 2 frames received |
| stat_c3_frx | 0 | | | Class 3 frames received |
| stat_lc_rx | 0 | | | Link control frames |
| received | | | | |
| stat_mc_rx | 0 | | | Multicast frames |
| received | | | | |
| stat_mc_to | 0 | | | Multicast timeouts |
| stat_mc_tx | 0 | | | Multicast frames |
| transmitted | | | | |
| tim_txcrd_z | 0 | | | Time TX Credit Zero |
| (2.5Us ticks) | | | | |
| tim_txcrd_z_vc 0- 3: | 0 | 0 | 0 | 0 |
| tim_txcrd_z_vc 4- 7: | 0 | 0 | 0 | 0 |
| tim_txcrd_z_vc 8-11: | 0 | 0 | 0 | 0 |
| tim_txcrd_z_vc 12-15: | 0 | 0 | 0 | 0 |
| lat_tot_pkt_vc 0- 3: | 1 | 1 | 1 | 1 |
| lat_tot_pkt_vc 4- 7: | 1 | 1 | 1 | 1 |
| lat_tot_pkt_vc 8-11: | 1 | 1 | 1 | 1 |
| lat_tot_pkt_vc 12-15: | 1 | 1 | 1 | 1 |
| lat_hi_time_vc 0- 3: | 0 | 0 | 0 | 0 |
| lat_hi_time_vc 4- 7: | 0 | 0 | 0 | 0 |
| lat_hi_time_vc 8-11: | 0 | 0 | 0 | 0 |
| lat_hi_time_vc 12-15: | 0 | 0 | 0 | 0 |
| lat_lo_time_vc 0- 3: | 1 | 1 | 1 | 1 |
| lat_lo_time_vc 4- 7: | 1 | 1 | 1 | 1 |
| lat_lo_time_vc 8-11: | 1 | 1 | 1 | 1 |
| lat_lo_time_vc 12-15: | 1 | 1 | 1 | 1 |
| max_latency_vc 0- 3: | 1 | 1 | 1 | 1 |
| max_latency_vc 4- 7: | 1 | 1 | 1 | 1 |
| max_latency_vc 8-11: | 1 | 1 | 1 | 1 |
| max_latency_vc 12-15: | 1 | 1 | 1 | 1 |
| latency_dma_ts | 09-09-2024 | UTC | Mon | 08:47:26 TXQ |
| Latency DMA TimeStamp | | | | |
| fec_cor_detected | 0 | | | Count of blocks that |
| were corrected by FEC | | | | |
| fec_uncor_detected | 0 | | | Count of blocks that |
| were left uncorrected by FEC | | | | |
| er_enc_in | 0 | | | Encoding errors inside |
| of frames | | | | |
| er_crc | 0 | | | Frames with CRC errors |
| er_trunc | 0 | | | Frames shorter than |
| minimum | | | | |
| er_toolong | 0 | | | Frames longer than |
| maximum | | | | |
| er_bad_eof | 0 | | | Frames with bad end-of- |
| frame | | | | |
| er_enc_out | 0 | | | Encoding error outside |
| of frames | | | | |
| er_bad_os | 0 | | | Invalid ordered set |
| er_pcs_blk | 0 | | | PCS block errors |
| er_rx_c3_timeout | 0 | | | Class 3 receive frames |

```

discarded due to timeout
er_tx_c3_timeout      0          Class 3 transmit frames
discarded due to timeout
er_unroutable         0          Frames that are
unroutable
er_unreachable        0          Frame with unreachable
destination
er_other_discard      0          Other discards
er_type1_miss         0          frames with FTB type 1
miss
er_type2_miss         0          frames with FTB type 2
miss
er_type6_miss         0          frames with FTB type 6
miss
er_zone_miss          0          frames with hard zoning
miss
er_lun_zone_miss      0          frames with LUN zoning
miss
er_crc_good_eof       0          Crc error with good eof
er_inv_arb             0          Invalid ARB
er_single_credit_loss 0          Single vcrdy/frame loss
on link
er_multi_credit_loss  0          Multiple vcrdy/frame
loss on link
other_credit_loss     0          Link timeout/complete
credit loss
phy_stats_clear_ts    09-06-2024 UTC Fri 08:30:19   Timestamp of
phy_port stats clear
lgc_stats_clear_ts    09-06-2024 UTC Fri 08:30:19   Timestamp of
lgc_port stats clear
fec_corrected_rate    0          FEC Corrected blocks per
second

```

```
portstats64show 61
```

```

stat64_wtx            0          top_int : 4-byte words transmitted
                                0          bottom_int : 4-byte words transmitted
stat64_wrx            0          top_int : 4-byte words received
                                0          bottom_int : 4-byte words received
stat64_ftx            0          top_int : Frames transmitted
                                0          bottom_int : Frames transmitted
stat64_frx            0          top_int : Frames received
                                0          bottom_int : Frames received
stat64_c2_frx         0          top_int : Class 2 frames received
                                0          bottom_int : Class 2 frames received
stat64_c3_frx         0          top_int : Class 3 frames received
                                0          bottom_int : Class 3 frames received
stat64_lc_rx          0          top_int : Link control frames received
                                0          bottom_int : Link control frames
received
stat64_mc_rx          0          top_int : Multicast frames received
                                0          bottom_int : Multicast frames received
stat64_mc_to          0          top_int : Multicast timeouts
                                0          bottom_int : Multicast timeouts
stat64_mc_tx          0          top_int : Multicast frames transmitted

```


| | | |
|---|---|--|
| | 0 | bottom_int : Multicast frames |
| transmitted | | |
| tim64_rdy_pri | 0 | top_int : Time R_RDY high priority |
| | 0 | bottom_int : Time R_RDY high priority |
| tim64_txcrd_z | 0 | top_int : Time BB_credit zero |
| | 0 | bottom_int : Time BB_credit zero |
| er64_enc_in | 0 | top_int : Encoding errors inside of |
| frames | | |
| | 0 | bottom_int : Encoding errors inside of |
| frames | | |
| er64_crc | 0 | top_int : Frames with CRC errors |
| | 0 | bottom_int : Frames with CRC errors |
| er64_trunc | 0 | top_int : Frames shorter than minimum |
| | 0 | bottom_int : Frames shorter than minimum |
| er64_toolong | 0 | top_int : Frames longer than maximum |
| | 0 | bottom_int : Frames longer than maximum |
| er64_bad_eof | 0 | top_int : Frames with bad end-of-frame |
| | 0 | bottom_int : Frames with bad end-of- |
| frame | | |
| er64_enc_out | 0 | top_int : Encoding error outside of |
| frames | | |
| | 0 | bottom_int : Encoding error outside of |
| frames | | |
| er64_disc_c3 | 0 | top_int : Class 3 frames discarded |
| | 0 | bottom_int : Class 3 frames discarded |
| er64_pcs_blk | 0 | top_int : PCS block errors |
| | 0 | bottom_int : PCS block errors |
| stat64_rateTxFrame | 0 | Tx frame rate (fr/sec) |
| stat64_rateRxFrame | 0 | Rx frame rate (fr/sec) |
| stat64_rateTxPeakFrame | 0 | Tx peak frame rate (fr/sec) |
| stat64_rateRxPeakFrame | 0 | Rx peak frame rate (fr/sec) |
| stat64_rateTxWord | 0 | Tx Word rate (words/sec) |
| stat64_rateRxWord | 0 | Rx Word rate (words/sec) |
| stat64_rateTxPeakWord | 0 | Tx peak Word rate (words/sec) |
| stat64_rateRxPeakWord | 0 | Rx peak Word rate (words/sec) |
| stat64_PRJTFrames | 0 | top_int : Number of PRJT frames |
| returned to this port | | |
| | 0 | bottom_int : Number of PRJT |
| frames returned to this port | | |
| stat64_PBSYFrames | 0 | top_int : Number of PBSY frames |
| returned to this port | | |
| | 0 | bottom_int : Number of PBSY |
| frames returned to this port | | |
| stat64_inputBuffersFull | 0 | top_int : Number of occurrences |
| when all input buffers full | | |
| | 0 | bottom_int : Number of |
| occurrences when all input buffers full | | |
| stat64_rxClass1Frames | 0 | top_int : Number of class 1 |
| frames received | | |
| | 0 | bottom_int : Number of class 1 |
| frames received | | |
| stat64_aveTxFrameSize | 0 | Average Tx Frame size |
| stat64_aveRxFrameSize | 0 | Average Rx Frame size |
| Lr_in | 0 | top_int |

```

Ols_in          0          bottom_int
                0          top_int
                0          bottom_int
Lr_out          0          top_int
                0          bottom_int
Ols_out        0          top_int
                0          bottom_int
Link_failure    0          top_int
                0          bottom_int
Invalid_CRC     0          top_int
                0          bottom_int
Invalid_word    0          top_int
                0          bottom_int
Protocol_err    0          top_int
                0          bottom_int
Loss_of_sig     0          top_int
                0          bottom_int
Loss_of_sync    0          top_int
                0          bottom_int
er_bad_os      0          top_int : Invalid ordered set
                0          bottom_int: Invalid ordered set

```

```

portrouteshow 61
port address ID: 0x013d00
external unicast routing table:
  0: Embedded
 255: Embedded
internal unicast routing table:
  0: Embedded

```

```
portcamshow 61
```

```

-----
Port  SID used  DID used  SID entries  DID entries
61    0         0         000000      000000
-----

```

```
ptbufshow, ptcridtshow, ptdatashow, ptstatsshow 61
```

```

S:
S:VF Enable:          1
S:
S:C4 Global Variable:
S:-----
-----
S:trace_stop:        0
S:
S:C4 Phy Data Pointers: c4_phyp = 0xb6abd140
S:-----
-----
S:tnodep              0xbb831d20      pt
      0x43028006
S:proto_phyp          0xb8806d80      phy_cfg
0xb6abe180
S:c4_chp              0x97e28000      c4_lgcp

```

```

0x97f60000
S:c4_phy_regp          0x81c30000    proc_dir
0xb85146e0
S:-----
-----
S:magic_id             0xc4345678    num_port_timer    12
S:prev_if_id          0x43020006    S:ftx             0
      tov                0
S:initialized          0              port_idx           6
S:ui_idx              61             slot_no
      0
S:blade_idx           6              sw_usr_ports      400
S:unused              0              intr_debounced
      0
S:aec_status          0x0            reason_code
      0
S:debug               0x00000004    debug_trc_line    0
S:rxbuf_list_head    0xffffffff    rxbuf_list_tail
0xffffffff
S:isAePort            0              port_misc_data
      0
S:num_fault1_rx_disc  0              num_fault2_rx_disc 0
S:p_lll_cause0        0              p_sig_regained    0
S:p_sync_regained     0              enc_out
      0x0
S:cached_fps_status  0              cached_sts_status 0
S:cached_er_crc_good_eof  0
S:cached_er_bad_os    0              cached_er_too_long 0
S:cached_er_trunc     0
cached_tot_er_crc_good_eof  0
S:num_pt_excess_intr  0              num_no_fid         0
S:num_fault1_cnt      0              num_fault2_cnt
      0
S:num_fault_lip       0              num_fault_lll      0
S:num_fault_rx_fifo   0              num_fault_hss      0
S:num_fault_bwait     0              lli_intr_prim
      0
S:num_sw_link_to      0
be_link_err_mon_count  0
S:ecb_enc_enabled     0              ecb_comp_enabled
      0
S:ecb_rsv_enc         0              ecb_rsv_comp       0
S:ecb_enc_bm          0x0            ecb_key_index
0xffffffff
S:fab_idx             4
S:num_be_lto          0              lto_count_reset_intvl
      0
S:lr_count_reset_intvl  0              num_be_lr
      0
S:num_fault_qsfp      0              check_lto
      0
S:credit_loaded       0              num_credit_overrun
      0
S:fec_enabled         0x0            fec_los_to_flag    0x0

```

```

S:phy_stats_clear_ts          1725611419      pcs_err_online
    0
S:pcs_err_light_det          0          pcs_err_ignore
    0
S:pcs_blk_err                0          pcs_hiber          0
S:phy_port_status            0          ecb_enc_lr_count
    0
S:dport_mode                 0          avoid_lto_det     0
S:sn_debounced              0x0       sn_started_kr_reqd 0
S:major_timer_started       0x0       ready_bm          0x0
S:parln_1_bm                0x0       parln_0_bm        0x0
S:be_los_of_sync_event_intvl 0
be_los_of_sync_event        0
S:errataPtenable_cntr       0          errataPoll_cntr
    0
S:jda_rx_sig_loss_det        0          jda_rx_sig_loss_cnt
    0
S:encrypt_blk_error          0
S:
S:      c4_trunk
S:=====
S:mark_ts                    0x0       deskew            0x0
S:master_phyp                0x0
S:
S:adelay[00]: 0x00000000 0x00000000 0x00000000 0x00000000
S:adelay[04]: 0x00000000 0x00000000 0x00000000 0x00000000
S:
S:      c4_buf
S:=====
S:tx_csc                      0          rx_csc
    0
S:ld_vc_credits              0          tx_flag           0x0
S:alloc_buffers              0          req_buffers       0
S:est_buffers                20         ld_use_est        0
S:bb_sc_n                    0          rx_bb_sc_n
    0
S:data_cr                     5          nondata_cr
    6
S:cr_enable                  0
S:ld_nondata_cr              6          tnodep
0xbb831e00
S:tx_credits[0] 0 0 0 0 0 0 0 0
S:tx_credits[8] 0 0 0 0 0 0 0 0
S:tx_credits[16] 0 0 0 0 0 0 0 0 0 0
S:tx_credits[24] 0 0 0 0 0 0 0 0 0 0
S:tx_credits[32] 0 0 0 0 0 0 0 0 0 0
S:rx_credits[0] 0 0 0 0 0 0 0 0
S:rx_credits[8] 0 0 0 0 0 0 0 0
S:rx_credits[16] 0 0 0 0 0 0 0 0 0 0
S:rx_credits[24] 0 0 0 0 0 0 0 0 0 0
S:rx_credits[32] 0 0 0 0 0 0 0 0 0 0
S:tx_mbc[0] 0 0 0 0 0 0 0 0
S:tx_mbc[8] 0 0 0 0 0 0 0 0
S:tx_mbc[16] 0 0 0 0 0 0 0 0

```

```

S:tx_mbc[24]    0    0    0    0    0    0    0    0
S:tx_mbc[32]    0    0    0    0    0    0    0    0
S:rx_mbc[0]     0    0    0    0    0    0    0    0
S:rx_mbc[8]     0    0    0    0    0    0    0    0
S:rx_mbc[16]   0    0    0    0    0    0    0    0
S:rx_mbc[24]   0    0    0    0    0    0    0    0
S:rx_mbc[32]   0    0    0    0    0    0    0    0

```

S:

S:C4 Chip Variables: c4_phyp->c4_chp = 0x97e28000

S:-----

S:version = 2.1

S:magic_id 0xc4234567 init_state 0x8

S:reset_reg_mem 0x1

S:ch_int0_en_bm 0x0 intr0_cause 0x0

S:ch_int1_en_bm 0x0 intr1_cause 0x0

S:ch_int2_en_bm 0x0 intr2_cause 0x0

S:ch 0x43010080 ch_cfg

0xb7013ba0

S:raslog_hndl.hndl 0x0 obj_halted 0x0

S:c4_chip_regp 0x80000000 c4_fpg_regp

0x81800000

S:num_chip_timer 0x5

S:hi_task_bm 0x0 lo_task_bm 0x0

S:c4_deferq.q_head 0x0 c4_deferq.q_tail 0x0

S:c4_tmrq.q_head 0x0 c4_tmrq.q_tail 0x0

slot_no 0

S:chip_inst 0 chip_idx 0

S:pll_initialized 1

pll_serdes_initialized 1

S:init_tries 0 init_ptEnableBM

0xba01b488

S:tick_polling 0xb980c9c0 sec_polling

0xb980c960

S:bb_fid 129

S:ecb_key_bm[0] 0x0 ecb_key_bm[1] 0x0

S:ecb_key_bm[2] 0x0 ecb_key_bm[3] 0x0

S:is_chip_enc_enabled 0

is_chip_comp_enabled 0x0

S:ftb_rsrcp->ftb_flags 0x0 act_rsrcp->act_flag 0x1

S:lue_rsrcp->lue_flags[0] 0x0 lue_rsrcp-

>lue_flags[1] 0x0

S:c4_phyp[00]: 0xb6ab0000 0xb6ab2080 0xb6ab4100 0xb6ab6180

S:c4_phyp[04]: 0xb6ab9040 0xb6abb0c0 0xb6abd140 0xb6ac0000

S:c4_phyp[08]: 0xb6ac2080 0xb6ac4100 0xb6ac6180 0xb6ac9040

S:c4_phyp[12]: 0xb6acb0c0 0xb6acd140 0xb6ad0000 0xb6ad2080

S:c4_phyp[16]: 0xb6ad4100 0xb6ad6180 0xb6ad9040 0xb6adb0c0

S:c4_phyp[20]: 0xb6add140 0xb6ae0000 0xb6ae2080 0xb6ae4100

S:c4_phyp[24]: 0xb6ae6180 0xb6ae9040 0xb6aeb0c0 0xb6aed140

S:c4_phyp[28]: 0xb6af0000 0xb6af2080 0xb6af4100 0xb6af6180

S:c4_phyp[32]: 0xb6af9040 0xb6afb0c0 0xb6afd140 0xb6b00000

S:c4_phyp[36]: 0xb6b02080 0xb6b04100 0xb6b06180 0xb6b09040

S:c4_phyp[40]: 0xb6b0b0c0 0xb6b0d140 0xb6b10000 0xb6b12080

S:c4_phyp[44]: 0xb6b14100 0xb6b16180 0xb6b19040 0xb6b1b0c0

```

S:c4_phyp[48]: 0xb6b1d140 0xb6b20000 0xb6b22080 0xb6b24100
S:c4_phyp[52]: 0xb6b26180 0xb6b29040 0xb6b2b0c0 0xb6b2d140
S:c4_phyp[56]: 0xb6b30000 0xb6b32080 0xb6b34100 0xb6b36180
S:c4_phyp[60]: 0xb6b39040 0xb6b3b0c0 0xb6b3d140 0xb6b40000
S:c4_lgcp[00]: 0x97f48000 0x97f4c000 0x97f50000 0x97f54000
S:c4_lgcp[04]: 0x97f58000 0x97f5c000 0x97f60000 0x97f64000
S:c4_lgcp[08]: 0x97f68000 0x97f6c000 0x97f70000 0x97f74000
S:c4_lgcp[12]: 0x97f78000 0x97f7c000 0x97f80000 0x97f84000
S:c4_lgcp[16]: 0x97f88000 0x97f8c000 0x97f90000 0x97f94000
S:c4_lgcp[20]: 0x97f98000 0x97f9c000 0x97fa0000 0x97fa4000
S:c4_lgcp[24]: 0x97fa8000 0x97fac000 0x97fb0000 0x97fb4000
S:c4_lgcp[28]: 0x97fb8000 0x97fbc000 0x97fc0000 0x97fc4000
S:c4_lgcp[32]: 0x97fc8000 0x97fcc000 0x97fd0000 0x97fd4000
S:c4_lgcp[36]: 0x97fd8000 0x97fdc000 0x97fe0000 0x97fe4000
S:c4_lgcp[40]: 0x97fe8000 0x97fec000 0x97ff0000 0x97ff4000
S:c4_lgcp[44]: 0x97ff8000 0x97ffc000 0x8e000000 0x8e004000
S:c4_lgcp[48]: 0x8e008000 0x8e00c000 0x8e010000 0x8e014000
S:c4_lgcp[52]: 0x8e018000 0x8e01c000 0x8e020000 0x8e024000
S:c4_lgcp[56]: 0x8e028000 0x8e02c000 0x8e030000 0x8e034000
S:c4_lgcp[60]: 0x8e038000 0x8e03c000 0x8e040000 0x8e044000
S:chip_timers[00]: 0xb980c720 0xb980c780 0xb980c7e0 0xb980c840
S:chip_timers[04]: 0xb980c8a0 0xb980c900
S:disc_trap_enable_required      0x0                rxlp_disc_log_stop
                                0x0
S:curr_rxlp_frm_cnt              0x0                curr_rxlp_disc_frm_cnt  0x0
S:sw_disc_frm_cnt                0x0                last_disc_frm_cnt       0x0
S:txq_nopop_pr_cnt              0x0                pollErrataDfe_ptBM
0xba01b4b0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][0] 0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][1] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][2] 0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][0] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][1] 0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][2] 0x0
S:
S:C4 Logical Port Variables
S:-----
-----
S:c4_lgc_regp                    0x81c30000
S:c4_phyp:
S:      0xb6abd140              0x0                0x0                0x0

S:      0x0                    0x0                0x0                0x0

S:master_phyp                   0xb6abd140        if_id
0x43020006
S:min_phyp                      0x0                max_phyp            0x0
S:num_phy_ports                 1                  lgc_num             6
S:num_iu_to                     0                  sw_txq_bm
0
S:port_fid                      129                unused              0
S:port_group                   0                  lgc_stats_clear_ts
1725611419
S:domain_tbl_sel                0                  area_tbl_sel

```

```

      0
S:egid_tbl_sel          0
S:serv_lo_bm           0x0
S:
S:Proto Phy Variables:
S:-----
-----
S:magic_id             0xc4123456      asic_phyp
0xb6abd140
S:port_id              0x43028006      phy_cfg
      0xb6abe180
S:upsm_hdl             0xb80110a0      physm_hdl
0xb8010dc0
S:ov_snsn_hdl         0xb8010c80      sw_snsn_hdl
0xb8010d20
S:ov_lksm_hdl         0xb8010e60      sw_lksm_hdl
0xb8010f00
S:trksm_hdl           0xb8011000      lr_flag          0x0
S:lr_active           0x0          qsfp_tsrx_rate_sel
      0x0
S:
S:UPSM      UP00: UPST_PORT_DISABLED    --> UP00: UPST_PORT_DISABLED
S:SNSM(OV)  SN00: OV_SNST_STOPPED       --> SN00: OV_SNST_STOPPED
S:SNSM(SW)  SW00: SW_SNST_STAGE_WS      --> SW00: SW_SNST_STAGE_WS
S:PHYSM     PP00: PHYST_STOPPED         --> PP00: PHYST_STOPPED
S:LKSM(OV)  LK00: OV_LKST_INACTIVE     --> LK00: OV_LKST_INACTIVE
S:LKSM(SW)  SW13: INACTIVE              --> SW13: INACTIVE
S:TRKSM     TRK0: TRKST_INIT            --> TRK0: TRKST_INIT
S:
S:physm variables:
S:-----
-----
S:proto_phyp          0xb8806d80      physm_hdl
0xb8010dc0
S:force_offline      0          copper          0
S:fault_reason       0: UNKNOWN
S:phy_media_present  0
S:
S:snsn variables:
S:-----
-----
S:speed              0xff          proto_phyp
0xb8806d80
S:hw_sn_tries_left   0x0          sw_sn_tries_left  0x0
S:curr_txsp_count    0x0
S:tx_max             0x0          curr_tx_indx
      0x0
S:curr_tx            0x0          curr_rxsp_count
      0x0
S:rx_max             0x0          curr_rx_indx
      0x0
S:curr_rx            0x0          rx_mem
      0x0
S:rxsp_rec_count     0x0

```

```

S:nc_start          0x0          tx_start          0x0
S:sync_start       0x0          sync_present      0x0
S:diag_auto        0x0          diag_speed        0xff
S:striped_wd_tov   3000          hw_wd_tov
      3000
S:step             0x0          qsfp28_speed_mode
      0x0
S:qsfp_mode0_hw_sn_tries_left  0x0
S:qsfp_mode1_hw_sn_tries_left  0x0
S:
S:lksm variables:
S:-----
-----
S:proto_phyph      0xb8806d80    ov_lksm_hdl
0xb8010e60
sw_lksm_hdl        0xb8010f00
num_lf1            0
S:hw_link_tries_left  0          sw_link_tries_left  0
S:buf_ptype        0x0          stored_entry_state  0x6
S:handshake_owner  0x0          mark_unsent
      0x0
S:busybuf_stuck    0x0          lr_wait           0x0
S:
S:trksm variables:
S:-----
-----
S:Not a trunk port
S:
S:upsm variables:
S:-----
-----
S:proto_phyph      0xb8806d80    upsm_hdl
0xb80110a0
S:bb_credits       0          port_beacon        0
S:port_diag_flag   0          force_offline
      0
S:port_fault_rsn   0: PORT_NO_FAULT
S:retry_init_rsn   0: UNKNOWN
S:limit_reason     0          limit_result       0
S:ie_fctl_mode     0          fec_in_sync_tries_left  0
S:retry_sn_fail_init  0
retry_link_fail_init  0
S:excess_lr_count  0
S:
S:c4_ch_cfg
S:-----
-----
S:c4_desc_ring_size 256      292      256      256      292
292      2      292      292
S:thresh_def       0          16          1          0
S:intr_tries       500          cmem_pattern
0xdeadbeef
S:cmem_pattern_upwd 2          cmem_init_time    16
S:cmem_init_tries 5

```



```

S:ctrl_par_thresh          2          data_par_thresh
   4
S:cam_par_thresh          4          buf_loss_thresh
   12
S:crit_par_thresh         2          non_crit_par_thresh
   6
S:pci_abort_thresh       10          pci_err_thresh          5
S:excess_chintr_thresh   8          sw_err_thresh           20
S:err_sample_period     300         intr_sleep
20000
S:frame_timeout 2500          proxy_dev          16384
S:vf_route 81920          qos          2048
S:stats 2048          f_redirect          2048
S:rsp_trap 2048          lun_zoning          20480
S:area_mode 0          ftb_max_loop[0]    0
S:ftb_max_loop[1]      6          ftb_max_loop[2]    9
S:ftb_max_loop[3]     10         ftb_max_loop[4]   10
S:ftb_max_loop[5]      5          ftb_max_loop[6]    6
S:ftb_seg_size[0]      0          ftb_seg_size[1]
16384
S:ftb_seg_size[2]      65536        ftb_seg_size[3]
16384
S:ftb_seg_size[4]      16384        ftb_seg_size[5]
65536
S:ftb_seg_size[6]      16384        ftb_seg_base[0]    0
S:ftb_seg_base[1]      0          ftb_seg_base[2]
65536
S:ftb_seg_base[3]      16384        ftb_seg_base[4]
32768
S:ftb_seg_base[5]      131072       ftb_seg_base[6]
49152
asic_err_monitor_period1 300
asic_err_monitor_period2 86400
zone_chk_to_poll_period 25
zone_chk_class2_reject_tov 220
S:
S:c4_phy_cfg
S:-----
-----

```

```

S:version = 2.1
S:pt          0x43028006          fab_ptr
0x9a800000
S:fabattr          0x9a8000d4          fab_iop
   0x9a800050
S:cfgbm          0xbb831b64          port_ctrl
0xb6abe198
S:pcap.pcap_bm          0x8d215547          pcap.pcap2_bm
0x2588289
S:pcap.pcap3_bm          0x1bebe0c
ui_idx          61          S:slot_no
   0
is_icl          0          S:sw_usr_ports          400
S:neg_speed          0 0 0 0 0 0
S:my_domain          0x1          port_mode          0x0

```

```

S:hw_sn_maxtries          100          sw_sn_maxtries
    0
S:hw_link_maxtries       10          sw_link_maxtries          5
S:rx_cyc_tov             28          rttov                    300
S:bufrdy_tov             300        busybuf_tov              286
S:mark_tov               300        lksm_tov                 3000
S:buf_dealloc_wait       4          hw_wd_tov                3000
S:hw_lk_train_tov        540        hw_lk_test_tov
    150
S:syswait_tx_12_lips     1          lip_rx_tov              55
S:al_time_tov            15        lp_tov                   2000
S:intr_tries_port        500        intr_mod_debounce
    250
S:intr_lsrflt_debounce   500        intr_efifo_debounce     100
S:port_no_fid            3          excess_ptintr_thresh    8
S:port_fault1_thresh     100       port_fault1_spur_thresh 250
S:port_fault1_disc_thresh 500
port_fault1_disc_spur_thresh 1000
S:port_fault2_thresh     5          losync_tov              100
S:port_sw_link_to        15        en_8g_scramble
    1
frc_hw_sn_mode           0x1
S:enc_poll_thresh        0          fec_enable
    0
S:fec_in_sync_to         50        fec_in_sync_try_max
    4
S:port_be_lto_threshold  100       port_be_lr_threshold
    2
S:be_cr_in_sync_to       5
port_credit_overrun_thresh 10
S:jda_sfp_losig_tov     400
jda_sfp_losig_try_max    30
S:striped_wd_tov         3000
no_sync_debounce         1200
S:
S:    fab_iop
S:=====
S:fab_iop->interop_mode  0x0          fab_iop->lab_mode          0x0
S:fab_iop->fl_bbc         0x0          fab_iop->fl_fan
    0x0
S:fab_iop->fl_cls         0x4          fab_iop->fl_rscn
    0x0
S:fab_iop->domain_id_offset 0x60        fab_iop-
>mcmt_fabric_mode        0x0
S:fab_iop->mcmt_default_zone 0x0          fab_iop-
>mcmt_safe_zone          0x0
S:
S:    port_ctrl
S:=====
S:port_ctrl.port_type    1          port_ctrl.port_grp        0
S:port_ctrl.port_number 61          port_ctrl.vc_mode          1
S:
S:    port_ctrl.lcap
S:=====

```

```

S:has_serdes          0          has_media          1
S:topology            1          skip_nego          0
S:skip_pnego         0          skip_init_event   0
S:en_shim             0          speed_neg
  1
S:loop_back           0          num_speeds        5
S:fec_enable          0
S:
S:      port_ctrl.speed_list array
S:=====
S:speed_list[0].auto_neg  1      speed_list[0].lnk_speed  0x0000000a
S:speed_list[1].auto_neg  1      speed_list[1].lnk_speed  0x00000008
S:speed_list[2].auto_neg  1      speed_list[2].lnk_speed  0x00000006
S:speed_list[3].auto_neg  1      speed_list[3].lnk_speed  0x00000005
S:speed_list[4].auto_neg  1      speed_list[4].lnk_speed  0x00000003
S:speed_list[5].auto_neg  0      speed_list[5].lnk_speed  0x00000000
S:
S:      port_ctrl.cm
S:=====
S:port_ctrl.cm.num_vcs      8
S:port_ctrl.cm.min_bufs     8
S:port_ctrl.cm.cr_shar_bufs 0
S:port_ctrl.vc_alloc
S:port_ctrl.vc_alloc        2 0 1 1 1 1 1 1
S:port_ctrl.vc_alloc        0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.norm_vc_alloc
S:port_ctrl.norm_vc_alloc   4 0 5 5 5 5 1 1
S:port_ctrl.norm_vc_alloc   0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.cm.skip_bb_credit 0
S:port_ctrl.cm.use_shim_based_sublist 0
S:
S:      port_ctrl.serdes_set
S:=====
S:serdes_type                0x8
S:serdes_data_t.ibm_hss_serdes.tx_drive_power 0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b_sign 0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b 0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_a 0x0
S:serdes_data_t.ibm_hss_serdes.rxeq 0x0
S:
S:      cfgbm
S:=====
S:old_distance                0x0          gport_lockdown      0x0
S:tpport                      0x1          speed                0x0
S:disable_eport               0x0          fcacc                0x0
S:lport_lockdown              0x0          priv_lport_lockdown
  0x0
S:vcxlt_linit                 0x0          delay_flogi          0x0
S:isl_interop                 0x0          distance              0x0
S:BufStarvFlag                0x0          credit_sharing       0x0
S:lport_halfduplex            0x0          lport_fairness       0x0
S:soft_neg                    0x0          asn_frc_hwretry      0x0

```

```

S:cr_recov          0x0          fport_buffers      0x0
S:export            0x0          export_mode
      0x0
S:csctl_en          0x0          mirror_port        0x0
S:fault_delay       0x0          non_dfe            0x0
S:fec_configured*(0=ENAB)  0          fec_tts
      0
S:port_persistently_disabled (permanently) 0 (0)
S:
S:      cfg property
S:=====
S:priv_pcfg_bm      0x00000000      lgcl_pcfg_bm
0xbb831ba4
S:fport_buffer      0x00000000
S:
S:
S:C4 Discard Cntrs: rxlp_stats = 0xb6abd4f0
S:-----
-----
S:disc_mcast_wka    0x0          disc_inv_did        0x0
S:disc_cl1_cl4      0x0          disc_sid_chk_fail   0x0
S:disc_inv_dom_egid_txpt  0x0          disc_vft_hop_cnt_1
      0x0
S:disc_classf       0x0          disc_fcp_cdb_inv    0x0
S:disc_vfid_trap_enabled  0x0
disc_vfid_hdr_chk_fail 0x0
S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err 0x0
S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err 0x0
S:disc_ftb_vm_mode  0x0          disc_ftb_agn_t2_miss 0x0
S:disc_ecb_de_pad_err 0x0          disc_ecb_de_tag_err  0x0
S:disc_ecb_de_seq_err 0x0          disc_ecb_err          0x0
S:disc_ftb_type4_match 0x0          disc_fcp_rsp_ftb_type4 0x0
S:disc_fcp_rsp_ftb_type4 0x0          disc_ftb_type5_match
      0x0
S:disc_ftb_type3_match 0x0          disc_els_ftb_type3   0x0
S:disc_ftb_type1_match 0x0          disc_els_rsp_ex_port 0x0
S:disc_inv_drp_dps   0x0          disc_did_lookup_miss 0x0
S:disc_ftb_type2_match 0x0          disc_trpd_plogi_pdisc 0x0
S:disc_type2_lookup_miss 0x0          disc_ftb_type6_match
      0x0
S:disc_els_rep_ex_port 0x0          disc_els_sid_lkup_bit1 0x0
S:disc_els_sid_lkup_bit0 0x0
disc_bls_frm_trap_bit1 0x0
S:disc_ftb_token_err 0x0          disc_asic_internal_err 0x0
S:disc_hard_zone_miss 0x0          disc_lun_zone_miss   0x0
S:disc_flt_frame_disc 0x0          disc_flt_parity_err  0x0
S:disc_frame_marked_du 0x0          disc_frame_marked_to  0x0
E:Connection type: FE
E:Port type: E_port
E:Trunk port: No
E:Configured Speed: AUTO_SPEED_NEGO
E:Max Capable Speed: 32G
E:Current SNSM Speed: UNDEFINED
E:Hardware TX Speed: 32G (0x00000004)

```

E:Hardware RX Speed: 32G (0x00000040)

E:

| | | | |
|-------------------|---|------------------|---|
| E:Interrupts: | 0 | Link_failure: | 0 |
| Loss_of_sync: | 0 | Loss_of_sig: | 0 |
| E:Lli: | 0 | Invalid_word: | 0 |
| E:trapped_frm: | 0 | fwd_status_ok: | 0 |
| E:fwd_timeout: | 0 | fwd_tx_unavail: | 0 |
| E:fwd_unroutable: | 0 | fwd_zone_out: | 0 |
| E:fwd_other_err: | 0 | frm_err_discard: | 0 |
| E:Fltr listA: | 0 | Fltr listB: | 0 |
| E:Zone trap fwd: | 0 | Zone trap disc: | 0 |
| E:shim_csum: | 0 | RTE_perr: | 0 |
| E:Invalid_crc: | 0 | Delim_err: | 0 |
| E:Protocol_err: | 0 | | |
| E:Lr_in: | 0 | Lr_out: | 0 |
| E:Ols_in: | 0 | Ols_out: | 0 |

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FILTER DATA

Shadow settings:

Filter Enable: 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000

Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass: 0x00000000
Real settings:
Enable RAM: 0x00000000, 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass RAM: 0x00000000

Shadowed filters:

Filter 0: Not Installed (MIRROR1)(LISTA)
c4_fldenable[0] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[0] = 0x00000000, c4_fltr_config[0] = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
c4_fldenable[1] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[1] = 0x00000000, c4_fltr_config[1] = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
c4_fldenable[2] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[2] = 0x00000000, c4_fltr_config[2] = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)

```
    c4_fldenable[3] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[3] = 0x00000000,c4_fltr_config[3] = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
    c4_fldenable[4] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[4] = 0x00000000,c4_fltr_config[4] = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
    c4_fldenable[5] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[5] = 0x00000000,c4_fltr_config[5] = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
    c4_fldenable[6] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[6] = 0x00000000,c4_fltr_config[6] = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
    c4_fldenable[7] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[7] = 0x00000000,c4_fltr_config[7] = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
    c4_fldenable[8] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[8] = 0x00000000,c4_fltr_config[8] = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
    c4_fldenable[9] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[9] = 0x00000000,c4_fltr_config[9] = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
    c4_fldenable[10] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[10] = 0x00000000,c4_fltr_config[10] =
0x00000000
Filter 11: Not Installed (SIM)(LISTA)
    c4_fldenable[11] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[11] = 0x00000000,c4_fltr_config[11] =
0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
    c4_fldenable[12] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[12] = 0x00000000,c4_fltr_config[12] =
0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
    c4_fldenable[13] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[13] = 0x00000000,c4_fltr_config[13] =
0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
    c4_fldenable[14] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[14] = 0x00000000,c4_fltr_config[14] =
0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
    c4_fldenable[15] = 0x00000000 0x00000000 0x00000000
```

```
0x00000000
    c4_fldnegate[15] = 0x00000000,c4_fltr_config[15] =
0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
    c4_fldenable[16] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[16] = 0x00000000,c4_fltr_config[16] =
0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
    c4_fldenable[17] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[17] = 0x00000000,c4_fltr_config[17] =
0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
    c4_fldenable[18] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[18] = 0x00000000,c4_fltr_config[18] =
0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
    c4_fldenable[19] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[19] = 0x00000000,c4_fltr_config[19] =
0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
    c4_fldenable[20] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[20] = 0x00000000,c4_fltr_config[20] =
0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
    c4_fldenable[21] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[21] = 0x00000000,c4_fltr_config[21] =
0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
    c4_fldenable[22] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[22] = 0x00000000,c4_fltr_config[22] =
0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
    c4_fldenable[23] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[23] = 0x00000000,c4_fltr_config[23] =
0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
    c4_fldenable[24] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[24] = 0x00000000,c4_fltr_config[24] =
0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
    c4_fldenable[25] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[25] = 0x00000000,c4_fltr_config[25] =
0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
```



```
    c4_fldenable[26] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[26] = 0x00000000,c4_fltr_config[26] =
0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
    c4_fldenable[27] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[27] = 0x00000000,c4_fltr_config[27] =
0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
    c4_fldenable[28] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[28] = 0x00000000,c4_fltr_config[28] =
0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
    c4_fldenable[29] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[29] = 0x00000000,c4_fltr_config[29] =
0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    c4_fldenable[30] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[30] = 0x00000000,c4_fltr_config[30] =
0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    c4_fldenable[31] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[31] = 0x00000000,c4_fltr_config[31] =
0x00000000
```

Real filters:

```
Filter 0: Not Installed (MIRROR1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
```

fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 11: Not Installed (SIM)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,

fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter dirty indicator: 0x00000000
Performance filters: 0
Port Mirror filters: 0 (0x0)

FIELD DATA

Shadowed fields:

fldoffset[0] = 0x00, fldmask[0] = 0x00, fldvalue_dyna[0]: 0x00 0x00
0x00 0x00
fldcontrol[0].inuse = 0x0 fldcontrol[0].refcnt = 0x00 0x00 0x00
0x00
fldoffset[1] = 0x00, fldmask[1] = 0x00, fldvalue_dyna[1]: 0x00 0x00
0x00 0x00
fldcontrol[1].inuse = 0x0 fldcontrol[1].refcnt = 0x00 0x00 0x00
0x00
fldoffset[2] = 0x00, fldmask[2] = 0x00, fldvalue_dyna[2]: 0x00 0x00
0x00 0x00
fldcontrol[2].inuse = 0x0 fldcontrol[2].refcnt = 0x00 0x00 0x00
0x00
fldoffset[3] = 0x00, fldmask[3] = 0x00, fldvalue_dyna[3]: 0x00 0x00
0x00 0x00
fldcontrol[3].inuse = 0x0 fldcontrol[3].refcnt = 0x00 0x00 0x00
0x00
fldoffset[4] = 0x00, fldmask[4] = 0x00, fldvalue_dyna[4]: 0x00 0x00
0x00 0x00
fldcontrol[4].inuse = 0x0 fldcontrol[4].refcnt = 0x00 0x00 0x00
0x00
fldoffset[5] = 0x00, fldmask[5] = 0x00, fldvalue_dyna[5]: 0x00 0x00
0x00 0x00
fldcontrol[5].inuse = 0x0 fldcontrol[5].refcnt = 0x00 0x00 0x00
0x00
fldoffset[6] = 0x00, fldmask[6] = 0x00, fldvalue_dyna[6]: 0x00 0x00
0x00 0x00
fldcontrol[6].inuse = 0x0 fldcontrol[6].refcnt = 0x00 0x00 0x00
0x00
fldoffset[7] = 0x00, fldmask[7] = 0x00, fldvalue_dyna[7]: 0x00 0x00
0x00 0x00
fldcontrol[7].inuse = 0x0 fldcontrol[7].refcnt = 0x00 0x00 0x00
0x00
fldoffset[8] = 0x00, fldmask[8] = 0x00, fldvalue_dyna[8]: 0x00 0x00
0x00 0x00
fldcontrol[8].inuse = 0x0 fldcontrol[8].refcnt = 0x00 0x00 0x00
0x00
fldoffset[9] = 0x00, fldmask[9] = 0x00, fldvalue_dyna[9]: 0x00 0x00
0x00 0x00
fldcontrol[9].inuse = 0x0 fldcontrol[9].refcnt = 0x00 0x00 0x00
0x00
fldoffset[10] = 0x00, fldmask[10] = 0x00, fldvalue_dyna[10]: 0x00 0x00
0x00 0x00
fldcontrol[10].inuse = 0x0 fldcontrol[10].refcnt = 0x00 0x00 0x00
0x00

0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000

Field dirty indicator: 0x00000000

FDB reference count fdb: 0 [0 0 0 0]
FDB reference count fdb: 1 [0 0 0 0]
FDB reference count fdb: 2 [0 0 0 0]
FDB reference count fdb: 3 [0 0 0 0]
FDB reference count fdb: 4 [0 0 0 0]
FDB reference count fdb: 5 [0 0 0 0]
FDB reference count fdb: 6 [0 0 0 0]
FDB reference count fdb: 7 [0 0 0 0]
FDB reference count fdb: 8 [0 0 0 0]
FDB reference count fdb: 9 [0 0 0 0]
FDB reference count fdb: 10 [0 0 0 0]
FDB reference count fdb: 11 [0 0 0 0]
FDB reference count fdb: 12 [0 0 0 0]
FDB reference count fdb: 13 [0 0 0 0]
FDB reference count fdb: 14 [0 0 0 0]
FDB reference count fdb: 15 [0 0 0 0]
FDB reference count fdb: 16 [0 0 0 0]
FDB reference count fdb: 17 [0 0 0 0]
FDB reference count fdb: 18 [0 0 0 0]
FDB reference count fdb: 19 [0 0 0 0]

Filter counters:

Filter counter 0: 0 (MIRROR1)
Filter counter 1: 0 (MIRROR2)
Filter counter 2: 0 (MIRROR3)
Filter counter 3: 0 (MIRROR4)
Filter counter 4: 0 (AEPORT_NON_MIRR_DROP)
Filter counter 5: 0 (ZONING TRAP)
Filter counter 6: 0 (FCR_EXPORT_DC)
Filter counter 7: 0 (TIN TRAP)
Filter counter 8: 0 (FICON CUP)
Filter counter 9: 0 (FICON CUP DST)
Filter counter 10: 0 (WELL KNOWN ADDR)
Filter counter 11: 0 (SIM)
Filter counter 12: 0 (UNUSED)
Filter counter 13: 0 (UNUSED)
Filter counter 14: 0 (UNUSED)
Filter counter 15: 0 (UNUSED)
Filter counter 16: 0 (PERF1)
Filter counter 17: 0 (PERF2)
Filter counter 18: 0 (PERF3)
Filter counter 19: 0 (PERF4)

Filter counter 20: 0 (PERF5)
Filter counter 21: 0 (PERF6)
Filter counter 22: 0 (PERF7)
Filter counter 23: 0 (PERF8)
Filter counter 24: 0 (PERF9)
Filter counter 25: 0 (PERF10)
Filter counter 26: 0 (PERF11)
Filter counter 27: 0 (PERF12)
Filter counter 28: 0 (OPM1)
Filter counter 29: 0 (OPM2)
Filter counter 30: 0 (IPM1)
Filter counter 31: 0 (IPM2)

ACL DATA

Logical port 6: Hard Zoning disabled, Soft Zoning disabled
Zone type: WWN Zoning
Frames with hard zone miss: 0

*** Please use filterportshow on user port 56 to display ACL hash tables and Mirroring resources of thischip.
***We show this data only for the first physical port which is an external port.

portFcPortCmdShow --slot 0 62 3
doing portFcPortCmdShow: arg1 = 3, arg2 = -2

portshow 62
portDisableReason: None
portCFlags: 0x0
portFlags: 0x4021 PRESENT U_PORT DISABLED LED
LocalSwcFlags: 0x0
portType: 26.0
POD Port: Need license to enable the port
portState: 2 Offline
Protocol: FC
portPhys: 2 No_Module portScn: 2 Offline
port generation number: 0
state transition count: 0

portId: 013e00
portIfId: 43020005
portWwn: 20:3e:d8:1f:cc:2c:99:90
portWwn of device(s) connected:
16b Area list:
Distance: normal
portSpeed: N32Gbps

FEC: Inactive
Credit Recovery: Inactive
LE domain: 0
Peer beacon: Off
FC Fastwrite: OFF
Interrupts: 0 Link_failure: 0 Frjt:

```

0
Unknown:          0          Loss_of_sync: 0          Fbsy:
0
Lli:             0          Loss_of_sig:  0
Proc_rqrd:      0          Protocol_err: 0
Timed_out:      0          Invalid_word: 0
Tx_unavail:     0          Invalid_crc:  0
Delim_err:      0          Address_err:  0
Lr_in:          0          Ols_in:       0
Lr_out:         0          Ols_out:      0

```

portloginshow 62

```

Type  PID      World Wide Name      credit df_sz cos
=====

```

portloginshow 62 -history

```

Type  PID      World Wide Name      logout time
=====

```

portregshow 62

LED registers

```

=====
0x81c2a000: c4_led_status      00000000      0x81c2a004:
c4_led_ctl      00000000

```

FPL registers

```

=====
0x81c28200: fpl_port_config    23490000
0x81c2820c: fpl_port_id_ctl    00000000      0x81c28210:
fpl_port_id_addr      00013e00
0x81c28214: fpl_port_speed     00000004      0x81c2821c:
fpl_lli_ctl           00000903
0x81c28228: fpl_lli_os_ctl     bc95b5b5      0x81c2822c:
fpl_lli_send_word     bc95b5b5
0x81c28230: fpl_lli_mark_rx    00000000      0x81c28234:
fpl_lli_rnd_trip_time 00000000
0x81c28238: fpl_lli_ns_status  80070007      0x81c2823c:
fpl_lli_intr_status   80070007
0x81c28244: fpl_lli_def        00000000      0x81c28254:
fpl_lli_intr_enable_clr 00100000
0x81c28258: fpl_err_intr_status 00000000      0x81c28260:
fpl_err_intr_enable_clr 00000000
0x81c28268: fpl_err_first_error 00000000      0x81c2826c:
fpl_speed_neg_ctl     00000000
0x81c28270: fpl_speed_neg_stat 00000000      0x81c28274:
fpl_softasn_ctl       0000000f
0x81c28278: fpl_link_init_ctl  00000000      0x81c2827c:
fpl_link_init_stat    00000000
0x81c28280: fpl_aec_ctl        00051060      0x81c28284:
fpl_aec_ctl2          04009f60

```


| | | | |
|-------------|--------------------|----------|-------------|
| 0x81c28288: | fpl_pcs_ctl | 00000160 | 0x81c2828c: |
| | fpl_fec_ctl | 00000441 | |
| 0x81c28290: | fpl_fec_cor | 00000000 | 0x81c28294: |
| | fpl_fec_uncor | 00000000 | |
| 0x81c28298: | fpl_hss_link_ctl | 0031f040 | 0x81c2829c: |
| | fpl_afifo_link_ctl | 00000a86 | |
| 0x81c282a0: | fpl_echo_lb_ctl | 0000028c | 0x81c282a4: |
| | fpl_scratch | 00000121 | |
| 0x81c282a8: | fpl_debug | 00030005 | 0x81c282ac: |
| | fpl_misc_debug | 00001800 | |
| 0x00000000: | SW_shadow_reg | 00000000 | 0x00000000: |
| | SW_c4_phy->cfgptr | 00030000 | |

per-fpg (per octet) registers

=====

| | | | |
|-------------|-------------------------|----------|-------------|
| 0x8180382c: | fpg_serdes_ctla0 | 81a37be7 | 0x81803830: |
| | fpg_serdes_ctla1 | 81a37be7 | |
| 0x81803834: | fpg_serdes_ctlb0 | 81a1c3c3 | 0x81803838: |
| | fpg_serdes_ctlb1 | 81a1c3c3 | |
| 0x8180383c: | fpg_serdes_xgmii_1ms | 00067c28 | 0x81803840: |
| | fpg_serdes_regtimctl | 40e47946 | |
| 0x81803844: | fpg_serdes_asnrsttimctl | 00000102 | |

HSS PLL registers

=====

| | | | |
|-------------|----------------------------|----------|-------------|
| 0x81803400: | 00_hssplla_vco_coarse_cal0 | 00000000 | 0x81803404: |
| | 01_hssplla_vco_coarse_cal1 | 00000014 | |
| 0x81803408: | 02_hssplla_vco_coarse_cal2 | 00000000 | 0x8180340c: |
| | 03_hssplla_vco_coarse_cal3 | 00000000 | |
| 0x81803410: | 04_hssplla_vco_coarse_cal4 | 00000000 | 0x81803424: |
| | 09_hssplla_power_ctl | 00000000 | |
| 0x81803428: | 0A_hssplla_charge_pump_ctl | 00000004 | 0x81803438: |
| | 0E_hssplla_pll_misc_ctl | 00000000 | |
| 0x8180343c: | 0F_hssplla_pclk_ctl | 000000f8 | 0x81803440: |
| | 10_hssplla_eyem_intv_ctl | 00000000 | |
| 0x81803444: | 11_hssplla_eyem_intv_lim1 | 00000000 | 0x81803448: |
| | 12_hssplla_eyem_intv_lim2 | 00000000 | |
| 0x8180344c: | 13_hssplla_eyem_intv_lim3 | 00000000 | 0x81803450: |
| | 14_hssplla_eyem_intv_lim4 | 00000000 | |
| 0x818034f0: | 3C_hssplla_macro_tst_ctl4 | 00000000 | 0x818034f4: |
| | 3D_hssplla_macro_tst_ctl3 | 00000000 | |
| 0x818034f8: | 3E_hssplla_macro_tst_ctl2 | 00000000 | 0x818034fc: |
| | 3F_hssplla_macro_tst_ctl1 | 00000000 | |
| 0x81803500: | 00_hssppll_vco_coarse_cal0 | 0000000a | 0x81803504: |
| | 01_hssppll_vco_coarse_cal1 | 00000014 | |
| 0x81803508: | 02_hssppll_vco_coarse_cal2 | 00000000 | 0x8180350c: |
| | 03_hssppll_vco_coarse_cal3 | 00000000 | |
| 0x81803510: | 04_hssppll_vco_coarse_cal4 | 00000000 | 0x81803524: |
| | 09_hssppll_power_ctl | 00000000 | |
| 0x81803528: | 0A_hssppll_charge_pump_ctl | 00000004 | 0x81803538: |
| | 0E_hssppll_pll_misc_ctl | 00000000 | |
| 0x8180353c: | 0F_hssppll_pclk_ctl | 000000f8 | 0x81803540: |
| | 10_hssppll_eyem_intv_ctl | 00000000 | |
| 0x81803544: | 11_hssppll_eyem_intv_lim1 | 00000000 | 0x81803548: |

| | | |
|---------------------------------------|----------|-------------|
| 12_hsspllb_eyem_intv_lim2 | 00000000 | |
| 0x8180354c: 13_hsspllb_eyem_intv_lim3 | 00000000 | 0x81803550: |
| 14_hsspllb_eyem_intv_lim4 | 00000000 | |
| 0x818035f0: 3C_hsspllb_macro_tst_ctl4 | 00000000 | 0x818035f4: |
| 3D_hsspllb_macro_tst_ctl3 | 00000000 | |
| 0x818035f8: 3E_hsspllb_macro_tst_ctl2 | 00000000 | 0x818035fc: |
| 3F_hsspllb_macro_tst_ctl1 | 00000000 | |

HSS TX registers

=====

| | | |
|---|----------|-------------|
| 0x81802100: 00_hsstx_cfg_mode_PHY | 00009f48 | 0x81802104: |
| 01_hsstx_test_ctl | 00000000 | |
| 0x81802108: 02_hsstx_coeff_ctl_INV | 00000000 | 0x8180210c: |
| 03_hsstx_drv_mode_ctl | 00000000 | |
| 0x81802110: 04_hsstx_drv_ovrd_ctl | 00000010 | 0x81802114: |
| 05_hsstx_dclk_align_ovrd | 00000080 | |
| 0x81802118: 06_hsstx_imp_cal_ovrd | 00000c0c | 0x8180211c: |
| 07_hsstx_dclk_drift_tol | 00000004 | |
| 0x81802120: 08_hsstx_tap0_coeff_TUNE | 00000000 | 0x81802124: |
| 09_hsstx_tap1_coeff_TUNE | 00000003 | |
| 0x81802128: 0A_hsstx_tap2_coeff_TUNE | 00000018 | 0x8180212c: |
| 0B_hsstx_tap3_coeff_TUNE | 0000000d | |
| 0x81802134: 0D_hsstx_pol_INV | 00000004 | 0x81802138: |
| 0E_hsstx_ae_cmd | 00000000 | |
| 0x8180213c: 0F_hsstx_ae_stat | 00000000 | 0x81802140: |
| 10_hsstx_ae_tap0_TUNE | 00000000 | |
| 0x81802144: 11_hsstx_ae_tap1_TUNE | 00000000 | 0x81802148: |
| 12_hsstx_ae_tap2_TUNE | 00000028 | |
| 0x8180214c: 13_hsstx_ae_tap3_TUNE | 00000000 | 0x81802154: |
| 15_hsstx_app_tune | 0000120e | |
| 0x81802158: 16_hsstx_analog_diag | 00000000 | 0x81802160: |
| 18_hsstx_4x_seg_app | 0000aafa | |
| 0x81802164: 19_hsstx_2x_seg_app | 00000000 | 0x81802168: |
| 1A_hsstx_1x_seg_app | 0000ff5d | |
| 0x8180216c: 1B_hsstx_seg_4x_term_app | 00000000 | 0x81802170: |
| 1C_hsstx_seg_2x1x_term_app | 00000f00 | |
| 0x81802174: 1D_hsstx_tap_sign_app | 00000004 | 0x81802178: |
| 1E_hsstx_ext_addr_data | 00000001 | |
| 0x8180217c: 1F_hsstx_ext_addr_addr | 00000000 | 0x81802180: |
| 20_hsstx_pat_buf_bytes_1_0 | 00000000 | |
| 0x81802184: 21_hsstx_pat_buf_bytes_3_2 | 00000000 | 0x81802188: |
| 22_hsstx_pat_buf_bytes_5_4 | 00000000 | |
| 0x8180218c: 23_hsstx_pat_buf_bytes_7_6 | 00000000 | 0x8180219c: |
| 27_hsstx_8023az_ctl | 00000000 | |
| 0x818021a0: 28_hsstx_dcc_ctl | 000060c0 | 0x818021a4: |
| 29_hsstx_dcc_ovrd | 00000000 | |
| 0x818021a8: 2A_hsstx_dcc_app | 00000109 | 0x818021ac: |
| 2B_hsstx_dcc_timeout | 0000ffff | |
| 0x818021c0: 30_hsstx_tap_sign_ovrd | 00000000 | 0x818021c8: |
| 32_hsstx_seg_4x_ovrd | 00000000 | |
| 0x818021cc: 33_hsstx_seg_2x_ovrd | 00000000 | 0x818021d0: |
| 34_hsstx_seg_1x_ovrd | 00000000 | |
| 0x818021d8: 36_hsstx_tap_seg_4x_term_ovrd | 00000000 | 0x818021dc: |
| 37_hsstx_tap_seg_2x_term_ovrd | 00000000 | |

| | | |
|---|----------|-------------|
| 0x818021e0: 38_hsstx_tap_seg_1x_term_ovrd | 00000000 | 0x818021ec: |
| 3B_hsstx_mac_test_ctl5 | 00000000 | |
| 0x818021f0: 3C_hsstx_mac_test_ctl4 | 00000000 | 0x818021f4: |
| 3D_hsstx_mac_test_ctl3 | 00000000 | |
| 0x818021f8: 3E_hsstx_mac_test_ctl2 | 00000000 | 0x818021fc: |
| 3F_hsstx_mac_test_ctl1 | 000000c6 | |

HSS RX registers

=====

| | | |
|---|----------|-------------|
| 0x81802300: 00_hssrx_cfg_mode_PHY | 00009e78 | 0x81802304: |
| 01_hssrx_test_ctl | 00000000 | |
| 0x81802308: 02_hssrx_phs_rot_ctl | 0000cb80 | 0x8180230c: |
| 03_hssrx_phs_rot_ofs_ctl | 00000610 | |
| 0x81802310: 04_hssrx_phs_rot_posn1 | 00001b1a | 0x81802314: |
| 05_hssrx_phs_rot_posn2 | 0000000b | |
| 0x81802318: 06_hssrx_phs_rot_sta_ofs1 | 00000000 | 0x8180231c: |
| 07_hssrx_phs_rot_sta_ofs2 | 0000001f | |
| 0x81802320: 08_hssrx_dfe_ctl_PHY | 00002002 | 0x81802324: |
| 09_hssrx_dfe_smpl_snap1 | 00000000 | |
| 0x81802328: 0A_hssrx_dfe_smpl_snap2 | 00008000 | 0x8180232c: |
| 0B_hssrx_vga_ctl1 | 000041fb | |
| 0x81802330: 0C_hssrx_vga_ctl2 | 00007aa0 | 0x81802334: |
| 0D_hssrx_vga_ctl3 | 000009e4 | |
| 0x81802338: 0E_hssrx_pwr_mgmt_ctl | 0000001f | 0x8180233c: |
| 0F_hssrx_iqamp_ctl1 | 0000001b | |
| 0x81802340: 10_hssrx_iqamp_ctl2 | 00000005 | 0x81802344: |
| 11_hssrx_dacap_dacan_sel | 00000003 | |
| 0x81802348: 12_hssrx_dacap_dacan | 00000201 | 0x8180234c: |
| 13_hssrx_daca_min | 00000000 | |
| 0x81802350: 14_hssrx_adac_ctl | 00000001 | 0x81802354: |
| 15_hssrx_ac_cp_ctl | 000031c3 | |
| 0x81802358: 16_hssrx_ac_cp_val | 0000004a | 0x8180235c: |
| 17_hssrx_dfe_h1h2h3_lcl_off_ch | 00000014 | |
| 0x81802360: 18_hssrx_dfe_h1h2h3_lcl_off_val | 00000000 | 0x81802364: |
| 19_hssrx_peaked_intg | 000000ff | |
| 0x81802368: 1A_hssrx_cdr_analog_sw | 0000ce00 | 0x8180236c: |
| 1B_hssrx_peaking_amp_init_c_PHY | 00000000 | |
| 0x81802370: 1C_hssrx_dac_dpc | 00000040 | 0x81802374: |
| 1D_hssrx_ddc | 00000000 | |
| 0x81802378: 1E_hssrx_int_stat_PHY | 00000c0f | 0x8180237c: |
| 1F_hssrx_dfe_func_ctl1_PHY | 0000ffff | |
| 0x81802380: 20_hssrx_dfe_func_ctl2_INV | 00007ebf | 0x81802384: |
| 21_hssrx_ofs_ch_dcc_qcc_idx | 00002000 | |
| 0x81802388: 22_hssrx_dfe_ofs_val | 00007f02 | 0x8180238c: |
| 23_hssrx_h_coeff_bist | 00000401 | |
| 0x81802390: 24_hssrx_ac_cap_bist | 000020d6 | 0x81802394: |
| 25_hssrx_max_gain_path_idx_res | 00007800 | |
| 0x81802398: 26_hssrx_loff_ctl | 00000054 | 0x8180239c: |
| 27_hssrx_sigdet_ctl | 00002680 | |
| 0x818023a0: 28_hssrx_ana_ctl_sw | 00000000 | 0x818023a4: |
| 29_hssrx_intg_dac_ofs | 0000dbde | |
| 0x818023a8: 2A_hssrx_eye_ctl | 00000000 | 0x818023ac: |
| 2B_hssrx_eye_met | 00000004 | |
| 0x818023b0: 2C_hssrx_eye_met_err_cnt | 00000000 | 0x818023b4: |

| | | | |
|--|----------|-----------|-------------|
| 2D_hssrx_eye_met_pdf_eyec | 00000000 | | |
| 0x818023b8: 2E_hssrx_eye_met_pat_len | | 0000007f | 0x818023bc: |
| 2F_hssrx_dfe_func_ctl3 | 0000dfff | | |
| 0x818023c0: 30_hssrx_dfe_tap_ctl_idx_ptr | | 00000008 | 0x818023c4: |
| 31_hssrx_dfe_tap | 00003030 | | |
| 0x818023c8: 32_hssrx_lte_ctl_TUNE | | 00001601 | 0x818023e4: |
| 39_hssrx_int_stat2 | 000041ff | | |
| 0x818023e8: 3A_hssrx_ac_cpl_cur_src_adj | | 00000042 | 0x818023ec: |
| 3B_hssrx_dcd_ctl | 00007c4a | | |
| 0x818023f0: 3C_hssrx_dcc_ctl | | 00000d81 | 0x818023f4: |
| 3D_hssrx_qcc_ctl | 00006947 | | |
| 0x818023f8: 3E_hssrx_mac_test_ctl2 | | 00000000 | 0x818023fc: |
| 3F_hssrx_mac_test_ctl1 | 00000000 | | |
| 0x81802348: 12_hssrx_dacap_dacan[02] | | 0200 0201 | |
| 0x81802360: 18_hssrx_dfe_h1h2h3_lcl_off_va[00] | | 0000 0000 | 0000 |
| 0000 0000 0000 0000 0000 | | | |
| 0x81802360: 18_hssrx_dfe_h1h2h3_lcl_off_va[08] | | 0000 0000 | 0000 |
| 0000 0000 0000 0000 0000 | | | |
| 0x81802360: 18_hssrx_dfe_h1h2h3_lcl_off_va[16] | | 0000 0000 | 0000 |
| 0000 0000 | | | |
| 0x81802388: 22_hssrx_dfe_ofs_val[00][00] | | 7f02 7f00 | 7d7d |
| 0000 0b7d 7f00 | | | |
| 0x81802388: 22_hssrx_dfe_ofs_val[03][00] | | 7e7b 7f00 | 7d7b |
| 0000 7b05 0000 | | | |
| 0x81802388: 22_hssrx_dfe_ofs_val[06][00] | | 7e7b 0001 | 097d |
| 7f00 7d7f 0000 | | | |
| 0x81802388: 22_hssrx_dfe_ofs_val[09][00] | | 057d 7f00 | 0501 |
| 0000 7f7d 0000 | | | |
| 0x81802388: 22_hssrx_dfe_ofs_val[12][00] | | 0103 0000 | 0703 |
| 7f00 7f06 007f | | | |
| 0x81802388: 22_hssrx_dfe_ofs_val[15][00] | | 7f7f 0000 | 797d |
| 007f 7e03 0000 | | | |
| 0x81802388: 22_hssrx_dfe_ofs_val[18][00] | | 7b05 0000 | 0007 |
| 007f 007b 0000 | | | |
| 0x81802388: 22_hssrx_dfe_ofs_val[21][00] | | 007b 0000 | 007b |
| 0000 007b 0000 | | | |
| 0x81802388: 22_hssrx_dfe_ofs_val[24][00] | | 0306 007f | 7f7e |
| 7f00 7b00 0000 | | | |
| 0x81802394: 25_hssrx_max_gain_path_idx_res[00] | | 0058 0853 | 1007 |
| 1887 2100 28ba 30a2 3800 | | | |
| 0x81802394: 25_hssrx_max_gain_path_idx_res[08] | | 40c0 489a | 5082 |
| 5800 6044 6804 7000 7800 | | | |
| 0x818023c4: 31_hssrx_dfe_tap[00] | | fffe 8080 | 0000 |
| 0000 0030 0030 3030 3030 | | | |
| 0x818023c4: 31_hssrx_dfe_tap[08] | | 3030 3030 | 3030 |
| 0000 | | | |
| 0x818023e8: 3A_hssrx_ac_cpl_cur_src_adj[00] | | 0042 0042 | 0042 |
| 0042 | | | |
| 0x818023ec: 3B_hssrx_dcd_ctl[00] | | 7c4a 5c00 | 7c82 |
| 5c00 7c81 | | | |
| 0x818023f0: 3C_hssrx_dcc_ctl[00] | | 0d81 0d81 | 0d81 |
| 0d00 | | | |
| 0x818023f4: 3D_hssrx_qcc_ctl[00] | | 6949 6947 | |

xfipcs, fec, aec, & aet registers

=====

| | | | | | | | |
|-------------|------------------|------|----------|----------|----------|----------|--|
| 0x81c28400: | xfipcs_reg | [00] | 00002040 | 00000080 | 00000000 | | |
| | 00000000 | | 00000001 | 00000008 | 00000000 | 00000000 | |
| 0x81c28420: | xfipcs_reg | [08] | 00008c01 | 00000000 | 00000000 | | |
| | 00000000 | | 00000000 | 00000000 | 00000000 | 00000000 | |
| 0x81c28440: | xfipcs_reg | [16] | 00000000 | 00000000 | 00000000 | | |
| | 00000000 | | 00000040 | 00000000 | 00000000 | 00000000 | |
| 0x81c28460: | xfipcs_reg | [24] | 00000000 | 00000000 | 00000000 | | |
| | 00000000 | | 00000000 | 00000000 | 00000000 | 00000000 | |
| 0x81c28480: | xfipcs_reg | [32] | 00000004 | 00000000 | 00000000 | | |
| | 00000000 | | 00000000 | 00000000 | 00000000 | 00000000 | |
| 0x81c28620: | fec_32g_128g_reg | [08] | 00000000 | 00000000 | 00000000 | | |
| | 00000000 | | 00000000 | 00000000 | 00000000 | 00000000 | |
| 0x81c28648: | fec_32g_128g_reg | [18] | 00000000 | 00000000 | 00000000 | | |
| | 00000000 | | 00000000 | 00000000 | 00000000 | 00000000 | |
| 0x81c28a00: | aec_reg | [00] | 00000000 | 00000000 | 00000000 | | |
| | 00000000 | | 00000000 | 00000000 | 00000000 | 00000000 | |
| 0x81c28c00: | aet_reg | [00] | 00000000 | 00000000 | 00000000 | | |
| | 00000000 | | 00000000 | | | | |

bbc registers

=====

| | | | | | | | | |
|-------------|---------|--|---|---|---|---|---|---|
| 0x81c29800: | bbc_trc | | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | | | | | | | |
| 0x81c29840: | bbc_trc | | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | | | | | | | |
| 0x81c29880: | bbc_trc | | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | | | | | | | |
| 0x81c298c0: | bbc_trc | | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | | | | | | | |
| 0x81c29900: | bbc_trc | | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | | | | | | | |
| 0x81c29804: | bbc_mbc | | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | | | | | | | |
| 0x81c29844: | bbc_mbc | | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | | | | | | | |
| 0x81c29884: | bbc_mbc | | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | | | | | | | |
| 0x81c298c4: | bbc_mbc | | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | | | | | | | |
| 0x81c29904: | bbc_mbc | | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | | | | | | | |
| 0x81c29a00: | bbc_rcc | | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | | | | | | | |
| 0x81c29a20: | bbc_rcc | | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | | | | | | | |
| 0x81c29a40: | bbc_rcc | | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | | | | | | | |
| 0x81c29a60: | bbc_rcc | | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | | | | | | | |
| 0x81c29a80: | bbc_rcc | | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | | | | | | | |
| 0x81c29c00: | bbc_rqc | | 0 | 0 | 0 | 0 | 0 | 0 |

| | | | | | | | |
|-------------------------|-------------------------|----------|---|---|---|-------------|----------|
| 0 | | | | | | | |
| 0x81c29c20: | bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c29c40: | bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c29c60: | bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c29c80: | bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c29d00: | bbc_fbpc | 00000000 | | | | 0x81c29d04: | bbc_csc |
| 00000000 | | | | | | | |
| 0x81c29d08: | bbc_rcc_inc | 00000000 | | | | 0x81c29d0c: | |
| bbc_rqc_inc | 00000000 | | | | | | |
| 0x81c29d10: | bbc_fbpc_inc | 00000000 | | | | 0x81c29d14: | |
| bbc_tmc_inc | 00000000 | | | | | | |
| 0x81c29d18: | bbc_threshold | 00080100 | | | | 0x81c29d1c: | |
| bbc_counter_clr | 00000000 | | | | | | |
| 0x81c29d20: | bbc_debug_en | 00000000 | | | | 0x81c29d24: | bbc_ctrl |
| 00200020 | | | | | | | |
| 0x81c29d28: | bbc_rqc_rcc_thresh | 00000055 | | | | 0x81c29d34: | |
| bbc_bb_sc_n | 00000000 | | | | | | |
| 0x81c29d38: | bbc_crd_reco_debug | 00000000 | | | | 0x81c29d3c: | |
| bbc_crd_reco_debug_data | 00000000 | | | | | | |
| 0x81c29d40: | bbc_multi_frm_loss_cnt | 00000000 | | | | 0x81c29d44: | |
| bbc_multi_rdy_loss_cnt | 00000000 | | | | | | |
| 0x81c29d48: | bbc_1frm_loss_recov_cnt | 00000000 | | | | 0x81c29d4c: | |
| bbc_1rdy_loss_recov_cnt | 00000000 | | | | | | |
| 0x81c29d58: | bbc_int_status | 00000000 | | | | 0x81c29d5c: | |
| bbc_int_set | 00000000 | | | | | | |
| 0x81c29d60: | bbc_int_first | 00000000 | | | | 0x81c29d64: | |
| bbc_frm_rdy_rx_err_addr | 00000000 | | | | | | |
| 0x81c29d68: | bbc_frm_rdy_tx_err_addr | 00000000 | | | | 0x81c29d6c: | |
| bbc_trc_mbc_err_addr | 00000000 | | | | | | |
| 0x81c29d70: | bbc_frm_rdy_rx_dbl_ecc | 00000000 | | | | 0x81c29d74: | |
| bbc_frm_rdy_tx_dbl_ecc | 00000000 | | | | | | |
| 0x81c29d78: | bbc_trc_mbc_dbl_ecc | 00000000 | | | | | |
| 0x81c29d7c: | bbc_fsm_status | 00001011 | | | | 0x81c29d80: | |
| bbc_force_err | 00000000 | | | | | | |
| 0x81c29d84: | bbc_crdt_avail0 | ffffffff | | | | 0x81c29d88: | |
| bbc_crdt_avail1 | 000000ff | | | | | | |
| 0x81c29d8c: | bbc_scratch | 00000000 | | | | | |

FPS registers

=====

| | | | | | | | |
|---------------------|----------------|----------|--|--|--|-------------|--|
| 0x81c28004: | fps_er_enc_in | 00000000 | | | | 0x81c28008: | |
| fps_er_crc | 00000000 | | | | | | |
| 0x81c2800c: | fps_er_trunc | 00000000 | | | | 0x81c28010: | |
| fps_er_toolong | 00000000 | | | | | | |
| 0x81c28014: | fps_er_bad_eof | 00000000 | | | | 0x81c28018: | |
| fps_er_enc_out | 00000000 | | | | | | |
| 0x81c2801c: | fps_er_bad_os | 00000000 | | | | 0x81c28020: | |
| fps_er_flush | 00000000 | | | | | | |
| 0x81c28024: | fps_er_ifg | 00000000 | | | | 0x81c28038: | |
| fps_er_crc_good_eof | 00000000 | | | | | | |

```

0x81c2803c: fps_inv_arb          00000000    0x81c28040:
fps_slow_sts_status    00000000
0x81c28044: fps_tx_frm_cnt          00000000    0x81c28048:
fps_rx_frm_cnt        00000000
0x81c28050: fps_tx_word_cnt_hi      00000000    0x81c2804c:
fps_tx_word_cnt_lo    00000000
0x81c28058: fps_rx_word_cnt_hi      00000000    0x81c28054:
fps_rx_word_cnt_lo    00000000

```

BAL registers

=====

```

0x81c2f000: bal_desired_buf          00000000    0x81c2f004:
bal_alloc_buf         00000000
0x81c2f008: bal_busy_buf            00000000    0x81c2f00c:
bal_usable_buf        00000000
0x81c2f010: bal_max_bor_buf         00000000
0x81c2f014: bal_busy_buf_thresh     00000002

```

TXQ registers

=====

```

0x81c2b004: txq_phys_port_ctl        00450000
0x81c2b050: txq_link_skew           00000000
0x81c2b068: txq_cr_lk_dttm_intr_sts [00] 00000000 00000000
0x81c2b070: txq_cr_lk_dttm_intr_en [00] 00000000 00000000
0x81c2b024: txq_disc_frm_trap_cnt    00000014

```

FDS registers

=====

```

0x81c2c000: fds_rxf_ctl              00000002    0x81c2c004:
fds_rxf_wait_thresh   00000909
0x81c2c018: fds_rxf_first_error      00000000    0x81c2c01c:
fds_rxf_first_error_info 00000000
0x81c2c020: fds_rxf_inout_pkt_cnt    00000000
0x81c2c008: fds_rxf_err_int_status   00000000    0x81c2c024:
fds_rxf_fifo_status   00888888
0x81c2d000: fds_txf_ctl              0000003a    0x81c2d004:
fds_txf_wait_ifg_thresh 00a00106
0x81c2d008: fds_txf_err_int_status   00000000    0x81c2d024:
fds_txf_fifo_status   00088888
0x81c2d02c: fds_txf_bbc_scs         00000000

```

Logical TXQ registers

=====

```

0x81c2b000: txq_log_port_ctl        00000002    0x81c2b008:
txq_port_status       00000000
0x81c2b00c: txq_todo_flags          [00] 00000000 00000000
0x81c2b014: txq_spd_match_desc      [00] 00000000 00000000 00000000
00000000
0x81c2b024: txq_spd_match_desc      [04] 00000014
0x81c2b028: txq_vc_weight           [00] 01010101 01010101 01010101
01010101
0x81c2b038: txq_vc_weight           [04] 01010101 01010101 01010101
01010101
0x81c2b048: txq_vc_weight           [08] 01010101 00010101

```

```

0x81c2b054: txq_cong_dttn_ctrl      00000000
0x81c2b058: txq_cong_dttn_intr_sts [00] 00000000 00000000
0x81c2b060: txq_cong_dttn_intr_en  [00] 00000000 00000000
0x81c2b078: txq_bw_limit_en_reg    [00] 00000000 00000000
0x81c2b080: txq_bw_gua_en_reg     [00] 00000000 00000000
0x81c2b088: txq_vc_group          [00] 03030300 03030303 03030303
03030303
0x81c2b098: txq_vc_group          [04] 03030303 03030303 03030303
03030303
0x81c2b0a8: txq_vc_group          [08] 03030303 03030303 00000000
00000000
0x81c2b0b0: txq_bw_thresh_group   [00] 00000000 00000000 00000000
00000000
0x81c2b0c0: txq_bw_thresh_group   [04] 00000000 00000000 00000000
00000000
0x81c2b0d0: txq_bw_thresh_group   [08] 00000000 00000000 00000000
00000000
0x81c2b0e0: txq_bw_thresh_group  [12] 00000000 00000000 00000000
00000000
0x81c2b0f0: txq_bw_thresh_group  [16] 00000000 00000000 00000000
00000000
0x81c2b100: txq_bw_thresh_group  [20] 00000000 00000000 00000000
00000000
0x81c2b110: txq_bw_thresh_group  [24] 00000000 00000000 00000000
00000000
0x81c2b120: txq_bw_thresh_group  [28] 00000000 00000000 00000000
00000000
0x81c2b130: txq_bw_thresh_group  [32] 00000000 00000000 00000000
00000000
0x81c2b140: txq_bw_thresh_group  [36] 00000000 00000000 00000000
00000000

```

txq Congestion detection Statistics RAM

=====

```

0x81090320: vc[0]          00000000      0x81090324: vc[1]
00000000
0x81090328: vc[2]          00000000      0x8109032c: vc[3]
00000000
0x81090330: vc[4]          00000000      0x81090334: vc[5]
00000000
0x81090338: vc[6]          00000000      0x8109033c: vc[7]
00000000
0x81090340: vc[8]          00000000      0x81090344: vc[9]
00000000
0x81090348: vc[10]         00000000     0x8109034c: vc[11]
00000000
0x81090350: vc[12]         00000000     0x81090354: vc[13]
00000000
0x81090358: vc[14]         00000000     0x8109035c: vc[15]
00000000
0x81090360: vc[16]         00000000     0x81090364: vc[17]
00000000
0x81090368: vc[18]         00000000     0x8109036c: vc[19]
00000000

```


| | | |
|--------------------|----------|--------------------|
| 0x81090370: vc[20] | 00000000 | 0x81090374: vc[21] |
| 00000000 | | |
| 0x81090378: vc[22] | 00000000 | 0x8109037c: vc[23] |
| 00000000 | | |
| 0x81090380: vc[24] | 00000000 | 0x81090384: vc[25] |
| 00000000 | | |
| 0x81090388: vc[26] | 00000000 | 0x8109038c: vc[27] |
| 00000000 | | |
| 0x81090390: vc[28] | 00000000 | 0x81090394: vc[29] |
| 00000000 | | |
| 0x81090398: vc[30] | 00000000 | 0x8109039c: vc[31] |
| 00000000 | | |
| 0x810903a0: vc[32] | 00000000 | 0x810903a4: vc[33] |
| 00000000 | | |
| 0x810903a8: vc[34] | 00000000 | 0x810903ac: vc[35] |
| 00000000 | | |
| 0x810903b0: vc[36] | 00000000 | 0x810903b4: vc[37] |
| 00000000 | | |
| 0x810903b8: vc[38] | 00000000 | 0x810903bc: vc[39] |
| 00000000 | | |

Logical STS registers

=====

| | | |
|----------------------------------|----------------------------|------------------------------|
| 0x81584444: sts_ftb_type1_miss | 00000000 | |
| 0x81584448: sts_ftb_type2_miss | 00000000 | |
| 0x8158444c: sts_ftb_type6_miss | 00000000 | |
| 0x81584450: sts_hard_zoning_miss | 00000000 | |
| 0x81584454: sts_lun_zoning_miss | 00000000 | |
| 0x8158445c: sts_unroutable | 00000000 | |
| 0x81581474: sts_rte_cl2 | 00000000 | 0x81581478: |
| sts_rte_cl3 | 00000000 | 0x8158147c: sts_rte_link_ctl |
| 00000000 | 0x81584468: sts_tx_timeout | 00000000 |

Logical STS filter registers

=====

| | | | | |
|-------------------------|------|----------|----------|----------|
| 0x815843c0: stsflt_trig | [00] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x815843d0: stsflt_trig | [04] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x815843e0: stsflt_trig | [08] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x815843f0: stsflt_trig | [12] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584400: stsflt_trig | [16] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584410: stsflt_trig | [20] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584420: stsflt_trig | [24] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584430: stsflt_trig | [28] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81584440: stsflt_trig | [32] | | | |

Logical STS discard registers

=====

| | | |
|------------------------------------|----------|-------------|
| 0x81581744: disc_mcast_wka | 00000000 | 0x81581748: |
| disc_inv_did | 00000000 | |
| 0x8158174c: disc_cl1_cl4 | 00000000 | 0x81581750: |
| disc_sid_chk_fail | 00000000 | |
| 0x81581754: disc_inv_dom_egid_txpt | 00000000 | 0x81581758: |
| disc_vft_hop_cnt_1 | 00000000 | |
| 0x8158175c: disc_classf | 00000000 | 0x81581760: |
| disc_fcp_cdb_inv | 00000000 | |
| 0x81581764: disc_vfid_trap_enabled | 00000000 | 0x81581768: |
| disc_vfid_hdr_chk_fail | 00000000 | |
| 0x8158176c: disc_shim_cksum_fail | 00000000 | 0x81581770: |
| disc_fed_edit_cmd_err | 00000000 | |
| 0x81581774: disc_ftb_vm_mode | 00000000 | 0x81581778: |
| disc_ftb_agnt2_miss | 00000000 | |
| 0x8158177c: disc_ecb_reserved | 00000000 | 0x81581780: |
| disc_ecb_de_pad_err | 00000000 | |
| 0x81581784: disc_ecb_de_tag_err | 00000000 | 0x81581788: |
| disc_ecb_de_seq_err | 00000000 | |
| 0x8158178c: disc_ecb_err | 00000000 | 0x81581790: |
| disc_ftb_type4_match | 00000000 | |
| 0x81581794: disc_fcp_rsp_ftb_type4 | 00000000 | 0x81581798: |
| disc_ftb_type5_match | 00000000 | |
| 0x8158179c: disc_ftb_type3_match | 00000000 | 0x815817a0: |
| disc_els_ftb_type3 | 00000000 | |
| 0x815817a4: disc_ftb_type1_match | 00000000 | 0x815817a8: |
| disc_els_rsp_ex_port | 00000000 | |
| 0x815817ac: disc_inv_drp_dps | 00000000 | 0x815817b0: |
| disc_did_lookup_miss | 00000000 | |
| 0x815817b4: disc_ftb_type2_match | 00000000 | 0x815817b8: |
| disc_trpd_plogi_pdisc | 00000000 | |
| 0x815817bc: disc_type2_lookup_miss | 00000000 | 0x815817c0: |
| disc_ftb_type6_match | 00000000 | |
| 0x815817c4: disc_els_rep_ex_port | 00000000 | 0x815817c8: |
| disc_els_sid_lkup_bit1 | 00000000 | |
| 0x815817cc: disc_els_sid_lkup_bit0 | 00000000 | 0x815817d0: |
| disc_bls_frm_trap_bit1 | 00000000 | |
| 0x815817d4: disc_ftb_token_err | 00000000 | 0x815817d8: |
| disc_asic_internal_err | 00000000 | |
| 0x815817dc: disc_hard_zone_miss | 00000000 | 0x815817e0: |
| disc_lun_zone_miss | 00000000 | |
| 0x815817e4: disc_flt_frame_disc | 00000000 | 0x815817e8: |
| disc_flt_parity_err | 00000000 | |
| 0x815817ec: disc_frame_marked_du | 00000000 | 0x815817f0: |
| disc_frame_marked_to | 00000000 | |
| 0x815817f4: disc_lkup_rte_prty_err | 00000000 | |

portstatshow 62

| | | |
|----------|---|--------------------------|
| stat_wtx | 0 | 4-byte words transmitted |
| stat_wrx | 0 | 4-byte words received |
| stat_ftx | 0 | Frames transmitted |
| stat_frx | 0 | Frames received |

| | | | | | |
|------------------------------|--------|------------|---------|----------|-------------------------|
| stat_c2_frx | 0 | | | | Class 2 frames received |
| stat_c3_frx | 0 | | | | Class 3 frames received |
| stat_lc_rx | 0 | | | | Link control frames |
| received | | | | | |
| stat_mc_rx | 0 | | | | Multicast frames |
| received | | | | | |
| stat_mc_to | 0 | | | | Multicast timeouts |
| stat_mc_tx | 0 | | | | Multicast frames |
| transmitted | | | | | |
| tim_txcrd_z | 0 | | | | Time TX Credit Zero |
| (2.5Us ticks) | | | | | |
| tim_txcrd_z_vc | 0- 3: | 0 | 0 | 0 | 0 |
| tim_txcrd_z_vc | 4- 7: | 0 | 0 | 0 | 0 |
| tim_txcrd_z_vc | 8-11: | 0 | 0 | 0 | 0 |
| tim_txcrd_z_vc | 12-15: | 0 | 0 | 0 | 0 |
| lat_tot_pkt_vc | 0- 3: | 1 | 1 | 1 | 1 |
| lat_tot_pkt_vc | 4- 7: | 1 | 1 | 1 | 1 |
| lat_tot_pkt_vc | 8-11: | 1 | 1 | 1 | 1 |
| lat_tot_pkt_vc | 12-15: | 1 | 1 | 1 | 1 |
| lat_hi_time_vc | 0- 3: | 0 | 0 | 0 | 0 |
| lat_hi_time_vc | 4- 7: | 0 | 0 | 0 | 0 |
| lat_hi_time_vc | 8-11: | 0 | 0 | 0 | 0 |
| lat_hi_time_vc | 12-15: | 0 | 0 | 0 | 0 |
| lat_lo_time_vc | 0- 3: | 1 | 1 | 1 | 1 |
| lat_lo_time_vc | 4- 7: | 1 | 1 | 1 | 1 |
| lat_lo_time_vc | 8-11: | 1 | 1 | 1 | 1 |
| lat_lo_time_vc | 12-15: | 1 | 1 | 1 | 1 |
| max_latency_vc | 0- 3: | 1 | 1 | 1 | 1 |
| max_latency_vc | 4- 7: | 1 | 1 | 1 | 1 |
| max_latency_vc | 8-11: | 1 | 1 | 1 | 1 |
| max_latency_vc | 12-15: | 1 | 1 | 1 | 1 |
| latency_dma_ts | | 09-09-2024 | UTC Mon | 08:47:27 | TXQ |
| Latency DMA TimeStamp | | | | | |
| fec_cor_detected | 0 | | | | Count of blocks that |
| were corrected by FEC | | | | | |
| fec_uncor_detected | 0 | | | | Count of blocks that |
| were left uncorrected by FEC | | | | | |
| er_enc_in | 0 | | | | Encoding errors inside |
| of frames | | | | | |
| er_crc | 0 | | | | Frames with CRC errors |
| er_trunc | 0 | | | | Frames shorter than |
| minimum | | | | | |
| er_toolong | 0 | | | | Frames longer than |
| maximum | | | | | |
| er_bad_eof | 0 | | | | Frames with bad end-of- |
| frame | | | | | |
| er_enc_out | 0 | | | | Encoding error outside |
| of frames | | | | | |
| er_bad_os | 0 | | | | Invalid ordered set |
| er_pcs_blk | 0 | | | | PCS block errors |
| er_rx_c3_timeout | 0 | | | | Class 3 receive frames |
| discarded due to timeout | | | | | |
| er_tx_c3_timeout | 0 | | | | Class 3 transmit frames |
| discarded due to timeout | | | | | |

| | | |
|-----------------------|-----------------------------|--------------------------|
| er_unroutable | 0 | Frames that are |
| unroutable | | |
| er_unreachable | 0 | Frame with unreachable |
| destination | | |
| er_other_discard | 0 | Other discards |
| er_type1_miss | 0 | frames with FTB type 1 |
| miss | | |
| er_type2_miss | 0 | frames with FTB type 2 |
| miss | | |
| er_type6_miss | 0 | frames with FTB type 6 |
| miss | | |
| er_zone_miss | 0 | frames with hard zoning |
| miss | | |
| er_lun_zone_miss | 0 | frames with LUN zoning |
| miss | | |
| er_crc_good_eof | 0 | Crc error with good eof |
| er_inv_arb | 0 | Invalid ARB |
| er_single_credit_loss | 0 | Single vcrdy/frame loss |
| on link | | |
| er_multi_credit_loss | 0 | Multiple vcrdy/frame |
| loss on link | | |
| other_credit_loss | 0 | Link timeout/complete |
| credit loss | | |
| phy_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | Timestamp of |
| phy_port stats clear | | |
| lgc_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | Timestamp of |
| lgc_port stats clear | | |
| fec_corrected_rate | 0 | FEC Corrected blocks per |
| second | | |

portstats64show 62

| | | |
|---------------|---|--|
| stat64_wtx | 0 | top_int : 4-byte words transmitted |
| | 0 | bottom_int : 4-byte words transmitted |
| stat64_wrx | 0 | top_int : 4-byte words received |
| | 0 | bottom_int : 4-byte words received |
| stat64_ftx | 0 | top_int : Frames transmitted |
| | 0 | bottom_int : Frames transmitted |
| stat64_frx | 0 | top_int : Frames received |
| | 0 | bottom_int : Frames received |
| stat64_c2_frx | 0 | top_int : Class 2 frames received |
| | 0 | bottom_int : Class 2 frames received |
| stat64_c3_frx | 0 | top_int : Class 3 frames received |
| | 0 | bottom_int : Class 3 frames received |
| stat64_lc_rx | 0 | top_int : Link control frames received |
| | 0 | bottom_int : Link control frames |
| received | | |
| stat64_mc_rx | 0 | top_int : Multicast frames received |
| | 0 | bottom_int : Multicast frames received |
| stat64_mc_to | 0 | top_int : Multicast timeouts |
| | 0 | bottom_int : Multicast timeouts |
| stat64_mc_tx | 0 | top_int : Multicast frames transmitted |
| | 0 | bottom_int : Multicast frames |
| transmitted | | |
| tim64_rdy_pri | 0 | top_int : Time R_RDY high priority |

| | | |
|---|---|--|
| tim64_txcrd_z | 0 | bottom_int : Time R_RDY high priority |
| | 0 | top_int : Time BB_credit zero |
| er64_enc_in | 0 | bottom_int : Time BB_credit zero |
| frames | 0 | top_int : Encoding errors inside of |
| | 0 | bottom_int : Encoding errors inside of |
| frames | 0 | top_int : Frames with CRC errors |
| er64_crc | 0 | bottom_int : Frames with CRC errors |
| er64_trunc | 0 | top_int : Frames shorter than minimum |
| | 0 | bottom_int : Frames shorter than minimum |
| er64_toolong | 0 | top_int : Frames longer than maximum |
| | 0 | bottom_int : Frames longer than maximum |
| er64_bad_eof | 0 | top_int : Frames with bad end-of-frame |
| | 0 | bottom_int : Frames with bad end-of- |
| frame | | |
| er64_enc_out | 0 | top_int : Encoding error outside of |
| frames | 0 | bottom_int : Encoding error outside of |
| | 0 | bottom_int : Encoding error outside of |
| frames | 0 | top_int : Class 3 frames discarded |
| er64_disc_c3 | 0 | bottom_int : Class 3 frames discarded |
| | 0 | bottom_int : Class 3 frames discarded |
| er64_pcs_blk | 0 | top_int : PCS block errors |
| | 0 | bottom_int : PCS block errors |
| stat64_rateTxFrame | 0 | Tx frame rate (fr/sec) |
| stat64_rateRxFrame | 0 | Rx frame rate (fr/sec) |
| stat64_rateTxPeakFrame | 0 | Tx peak frame rate (fr/sec) |
| stat64_rateRxPeakFrame | 0 | Rx peak frame rate (fr/sec) |
| stat64_rateTxWord | 0 | Tx Word rate (words/sec) |
| stat64_rateRxWord | 0 | Rx Word rate (words/sec) |
| stat64_rateTxPeakWord | 0 | Tx peak Word rate (words/sec) |
| stat64_rateRxPeakWord | 0 | Rx peak Word rate (words/sec) |
| stat64_PRJTFrames | 0 | top_int : Number of PRJT frames |
| returned to this port | 0 | bottom_int : Number of PRJT |
| | 0 | bottom_int : Number of PRJT |
| frames returned to this port | | |
| stat64_PBSYFrames | 0 | top_int : Number of PBSY frames |
| returned to this port | 0 | bottom_int : Number of PBSY |
| | 0 | bottom_int : Number of PBSY |
| frames returned to this port | | |
| stat64_inputBuffersFull | 0 | top_int : Number of occurrences |
| when all input buffers full | 0 | bottom_int : Number of |
| | 0 | bottom_int : Number of |
| occurrences when all input buffers full | | |
| stat64_rxClass1Frames | 0 | top_int : Number of class 1 |
| frames received | 0 | bottom_int : Number of class 1 |
| | 0 | bottom_int : Number of class 1 |
| frames received | | |
| stat64_aveTxFrameSize | 0 | Average Tx Frame size |
| stat64_aveRxFrameSize | 0 | Average Rx Frame size |
| Lr_in | 0 | top_int |
| | 0 | bottom_int |
| Ols_in | 0 | top_int |
| | 0 | bottom_int |

```

Lr_out          0          top_int
                0          bottom_int
Ols_out         0          top_int
                0          bottom_int
Link_failure    0          top_int
                0          bottom_int
Invalid_CRC     0          top_int
                0          bottom_int
Invalid_word    0          top_int
                0          bottom_int
Protocol_err    0          top_int
                0          bottom_int
Loss_of_sig     0          top_int
                0          bottom_int
Loss_of_sync    0          top_int
                0          bottom_int
er_bad_os       0          top_int : Invalid ordered set
                0          bottom_int: Invalid ordered set

```

```

portrouteshow 62
port address ID: 0x013e00
external unicast routing table:
  0: Embedded
 255: Embedded
internal unicast routing table:
  0: Embedded

```

```
portcamshow 62
```

```

-----
Port  SID used  DID used  SID entries  DID entries
62    0         0        000000      000000
-----

```

```
ptbufshow, ptcreditshow, ptdatashow, ptstatsshow 62
```

```

S:
S:VF Enable:          1
S:
S:C4 Global Variable:
S:-----
-----
S:trace_stop:        0
S:
S:C4 Phy Data Pointers: c4_phyp = 0xb6abb0c0
S:-----
-----
S:tnodep              0xbb830a80      pt
      0x43028005
S:proto_phyp          0xb8806a20      phy_cfg
0xb6abc100
S:c4_chp              0x97e28000      c4_lgcp
0x97f5c000
S:c4_phy_regp         0x81c28000      proc_dir
0xb8514000

```

```

S:-----
-----
S:magic_id          0xc4345678      num_port_timer      12
S:prev_if_id       0x43020005      S:ftx                0
      tov                0
S:initialized       0                port_idx             5
S:ui_idx           62                slot_no
      0
S:blade_idx        5                sw_usr_ports         400
S:unused           0                intr_debounced
      0
S:aec_status       0x0                reason_code
      0
S:debug            0x00000004      debug_trc_line       0
S:rxbuf_list_head 0xffffffff      rxbuf_list_tail
0xffffffff
S:isAePort         0                port_misc_data
      0
S:num_fault1_rx_disc 0                num_fault2_rx_disc   0
S:p_llli_cause0    0                p_sig_regained        0
S:p_sync_regained  0                enc_out
      0x0
S:cached_fps_status 0                cached_sts_status     0
S:cached_er_crc_good_eof 0
S:cached_er_bad_os 0                cached_er_too_long    0
S:cached_er_trunc  0
cached_tot_er_crc_good_eof 0
S:num_pt_excess_intr 0                num_no_fid            0
S:num_fault1_cnt   0                num_fault2_cnt
      0
S:num_fault_lip    0                num_fault_llli        0
S:num_fault_rx_fifo 0                num_fault_hss          0
S:num_fault_bwait  0                lli_intr_prim
      0
S:num_sw_link_to   0
be_link_err_mon_count 0
S:ecb_enc_enabled  0                ecb_comp_enabled
      0
S:ecb_rsv_enc      0                ecb_rsv_comp          0
S:ecb_enc_bm       0x0                ecb_key_index
0xffffffff
S:fab_idx          4
S:num_be_lto       0                lto_count_reset_intvl
      0
S:lr_count_reset_intvl 0                num_be_lr
      0
S:num_fault_qsfp   0                check_lto
      0
S:credit_loaded    0                num_credit_overrun
      0
S:fec_enabled      0x0                fec_los_to_flag       0x0
S:phy_stats_clear_ts 0                pcs_err_online
      0
S:pcs_err_light_det 0                pcs_err_ignore

```

```

      0
S:pcs_blk_err          0          pcs_hiber          0
S:phy_port_status     0          ecb_enc_lr_count
      0

S:dport_mode          0          avoid_lto_det     0
S:sn_debounced       0x0       sn_started_kr_reqd 0
S:major_timer_started 0x0       ready_bm          0x0
S:parln_1_bm         0x0       parln_0_bm        0x0
S:be_los_of_sync_event_intvl
be_los_of_sync_event  0
S:errataPtenable_cntr 0          errataPoll_cntr
      0
S:jda_rx_sig_loss_det 0          jda_rx_sig_loss_cnt
      0

S:encrypt_blk_error   0
S:
S:      c4_trunk
S:=====
S:mark_ts             0x0          deskew            0x0
S:master_phyp        0x0
S:
S:adelay[00]: 0x00000000 0x00000000 0x00000000 0x00000000
S:adelay[04]: 0x00000000 0x00000000 0x00000000 0x00000000
S:
S:      c4_buf
S:=====
S:tx_csc              0          rx_csc
      0
S:ld_vc_credits      0          tx_flag           0x0
S:alloc_buffers      0          req_buffers       0
S:est_buffers        20         ld_use_est        0
S:bb_sc_n            0          rx_bb_sc_n
      0
S:data_cr             5          nondata_cr
      6
S:cr_enable          0
S:ld_nondata_cr      6          tnodep
0xbb830b60
S:tx_credits[0] 0    0    0    0    0    0    0    0
S:tx_credits[8] 0    0    0    0    0    0    0    0
S:tx_credits[16]    0    0    0    0    0    0    0    0    0
S:tx_credits[24]    0    0    0    0    0    0    0    0    0
S:tx_credits[32]    0    0    0    0    0    0    0    0    0
S:rx_credits[0] 0    0    0    0    0    0    0    0
S:rx_credits[8] 0    0    0    0    0    0    0    0
S:rx_credits[16]    0    0    0    0    0    0    0    0    0
S:rx_credits[24]    0    0    0    0    0    0    0    0    0
S:rx_credits[32]    0    0    0    0    0    0    0    0    0
S:tx_mbc[0]         0    0    0    0    0    0    0    0
S:tx_mbc[8]         0    0    0    0    0    0    0    0
S:tx_mbc[16]        0    0    0    0    0    0    0    0
S:tx_mbc[24]        0    0    0    0    0    0    0    0
S:tx_mbc[32]        0    0    0    0    0    0    0    0
S:rx_mbc[0]         0    0    0    0    0    0    0    0

```


S:rx_mbc[8] 0 0 0 0 0 0 0 0
S:rx_mbc[16] 0 0 0 0 0 0 0 0
S:rx_mbc[24] 0 0 0 0 0 0 0 0
S:rx_mbc[32] 0 0 0 0 0 0 0 0

S:

S:C4 Chip Variables: c4_phyp->c4_chp = 0x97e28000

S:-----

S:version = 2.1

S:magic_id 0xc4234567 init_state 0x8

S:reset_reg_mem 0x1

S:ch_int0_en_bm 0x0 intr0_cause 0x0

S:ch_int1_en_bm 0x0 intr1_cause 0x0

S:ch_int2_en_bm 0x0 intr2_cause 0x0

S:ch 0x43010080 ch_cfg

0xb7013ba0

S:raslog_hndl.hndl 0x0 obj_halted 0x0

S:c4_chip_regp 0x80000000 c4_fpg_regp

0x81800000

S:num_chip_timer 0x5

S:hi_task_bm 0x0 lo_task_bm 0x0

S:c4_deferq.q_head 0x0 c4_deferq.q_tail 0x0

S:c4_tmrq.q_head 0x0 c4_tmrq.q_tail 0x0

slot_no 0

S:chip_inst 0 chip_idx 0

S:pll_initialized 1

pll_serdes_initialized 1

S:init_tries 0 init_ptEnableBM

0xba01b488

S:tick_polling 0xb980c9c0 sec_polling

0xb980c960

S:bb_fid 129

S:ecb_key_bm[0] 0x0 ecb_key_bm[1] 0x0

S:ecb_key_bm[2] 0x0 ecb_key_bm[3] 0x0

S:is_chip_enc_enabled 0

is_chip_comp_enabled 0x0

S:ftb_rsrcp->ftb_flags 0x0 act_rsrcp->act_flag 0x1

S:lue_rsrcp->lue_flags[0] 0x0 lue_rsrcp-

>lue_flags[1] 0x0

S:c4_phyp[00]: 0xb6ab0000 0xb6ab2080 0xb6ab4100 0xb6ab6180

S:c4_phyp[04]: 0xb6ab9040 0xb6abb0c0 0xb6abd140 0xb6ac0000

S:c4_phyp[08]: 0xb6ac2080 0xb6ac4100 0xb6ac6180 0xb6ac9040

S:c4_phyp[12]: 0xb6acb0c0 0xb6acd140 0xb6ad0000 0xb6ad2080

S:c4_phyp[16]: 0xb6ad4100 0xb6ad6180 0xb6ad9040 0xb6adb0c0

S:c4_phyp[20]: 0xb6add140 0xb6ae0000 0xb6ae2080 0xb6ae4100

S:c4_phyp[24]: 0xb6ae6180 0xb6ae9040 0xb6aeb0c0 0xb6aed140

S:c4_phyp[28]: 0xb6af0000 0xb6af2080 0xb6af4100 0xb6af6180

S:c4_phyp[32]: 0xb6af9040 0xb6afb0c0 0xb6afd140 0xb6b00000

S:c4_phyp[36]: 0xb6b02080 0xb6b04100 0xb6b06180 0xb6b09040

S:c4_phyp[40]: 0xb6b0b0c0 0xb6b0d140 0xb6b10000 0xb6b12080

S:c4_phyp[44]: 0xb6b14100 0xb6b16180 0xb6b19040 0xb6b1b0c0

S:c4_phyp[48]: 0xb6b1d140 0xb6b20000 0xb6b22080 0xb6b24100

S:c4_phyp[52]: 0xb6b26180 0xb6b29040 0xb6b2b0c0 0xb6b2d140

S:c4_phyp[56]: 0xb6b30000 0xb6b32080 0xb6b34100 0xb6b36180

```

S:c4_phyp[60]: 0xb6b39040 0xb6b3b0c0 0xb6b3d140 0xb6b40000
S:c4_lgcp[00]: 0x97f48000 0x97f4c000 0x97f50000 0x97f54000
S:c4_lgcp[04]: 0x97f58000 0x97f5c000 0x97f60000 0x97f64000
S:c4_lgcp[08]: 0x97f68000 0x97f6c000 0x97f70000 0x97f74000
S:c4_lgcp[12]: 0x97f78000 0x97f7c000 0x97f80000 0x97f84000
S:c4_lgcp[16]: 0x97f88000 0x97f8c000 0x97f90000 0x97f94000
S:c4_lgcp[20]: 0x97f98000 0x97f9c000 0x97fa0000 0x97fa4000
S:c4_lgcp[24]: 0x97fa8000 0x97fac000 0x97fb0000 0x97fb4000
S:c4_lgcp[28]: 0x97fb8000 0x97fbc000 0x97fc0000 0x97fc4000
S:c4_lgcp[32]: 0x97fc8000 0x97fcc000 0x97fd0000 0x97fd4000
S:c4_lgcp[36]: 0x97fd8000 0x97fdc000 0x97fe0000 0x97fe4000
S:c4_lgcp[40]: 0x97fe8000 0x97fec000 0x97ff0000 0x97ff4000
S:c4_lgcp[44]: 0x97ff8000 0x97ffc000 0x8e000000 0x8e004000
S:c4_lgcp[48]: 0x8e008000 0x8e00c000 0x8e010000 0x8e014000
S:c4_lgcp[52]: 0x8e018000 0x8e01c000 0x8e020000 0x8e024000
S:c4_lgcp[56]: 0x8e028000 0x8e02c000 0x8e030000 0x8e034000
S:c4_lgcp[60]: 0x8e038000 0x8e03c000 0x8e040000 0x8e044000
S:chip_timers[00]: 0xb980c720 0xb980c780 0xb980c7e0 0xb980c840
S:chip_timers[04]: 0xb980c8a0 0xb980c900
S:disc_trap_enable_required      0x0                rxlp_disc_log_stop
      0x0
S:curr_rxlp_frm_cnt      0x0                curr_rxlp_disc_frm_cnt  0x0
S:sw_disc_frm_cnt      0x0                last_disc_frm_cnt      0x0
S:txq_nopop_pr_cnt      0x0                pollErrataDfe_ptBM
0xba01b4b0
S:ftb_rsrpc->chip_ref[FTB_REF_CHP_EC][0]      0x0
ftb_rsrpc->chip_ref[FTB_REF_CHP_EC][1] 0x0
S:ftb_rsrpc->chip_ref[FTB_REF_CHP_EC][2]      0x0
ftb_rsrpc->chip_ref[FTB_REF_CHP_NRC][0] 0x0
S:ftb_rsrpc->chip_ref[FTB_REF_CHP_NRC][1]      0x0
ftb_rsrpc->chip_ref[FTB_REF_CHP_NRC][2] 0x0
S:
S:C4 Logical Port Variables
S:-----
-----
S:c4_lgc_regp      0x81c28000
S:c4_phyp:
S:      0xb6abb0c0      0x0                0x0                0x0

S:      0x0                0x0                0x0                0x0

S:master_phyp      0xb6abb0c0      if_id
0x43020005
S:min_phyp      0x0                max_phyp      0x0
S:num_phy_ports      1                lgc_num      5
S:num_iu_to      0                sw_txq_bm
0
S:port_fid      129                unused      0
S:port_group      0                lgc_stats_clear_ts
1725611419
S:domain_tbl_sel      0                area_tbl_sel
0
S:egid_tbl_sel      0
S:serv_lo_bm      0x0

```

```

S:
S:Proto Phy Variables:
S:-----
-----
S:magic_id          0xc4123456      asic_phyp
0xb6abb0c0
S:port_id           0x43028005      phy_cfg
0xb6abc100
S:upsm_hdl         0xb8010aa0      physm_hdl
0xb8010820
S:ov_snsn_hdl      0xb80106e0      sw_snsn_hdl
0xb8010780
S:ov_lksm_hdl      0xb80108c0      sw_lksm_hdl
0xb8010960
S:trksm_hdl        0xb8010a00      lr_flag          0x0
S:lr_active        0x0             qsfm_tsr_x_rate_sel
0x0

S:
S:UPSM             UP00: UPST_PORT_DISABLED  --> UP00: UPST_PORT_DISABLED
S:SNSM(OV)         SN00: OV_SNST_STOPPED    --> SN00: OV_SNST_STOPPED
S:SNSM(SW)         SW00: SW_SNST_STAGE_WS   --> SW00: SW_SNST_STAGE_WS
S:PHYSM            PP00: PHYST_STOPPED     --> PP00: PHYST_STOPPED
S:LKSM(OV)         LK00: OV_LKST_INACTIVE  --> LK00: OV_LKST_INACTIVE
S:LKSM(SW)         SW13: INACTIVE          --> SW13: INACTIVE
S:TRKSM            TRK0: TRKST_INIT        --> TRK0: TRKST_INIT
S:
S:physm variables:
S:-----
-----
S:proto_phyp       0xb8806a20      physm_hdl
0xb8010820
S:force_offline    0               copper            0
S:fault_reason     0: UNKNOWN
S:phy_media_present 0
S:
S:snsn variables:
S:-----
-----
S:speed           0xff           proto_phyp
0xb8806a20
S:hw_sn_tries_left 0x0           sw_sn_tries_left 0x0
S:curr_txsp_count 0x0           curr_tx_indx
S:tx_max          0x0           curr_rxsp_count
0x0
S:curr_tx         0x0           curr_rx_indx
0x0
S:rx_max          0x0           rx_mem
0x0
S:curr_rx         0x0
0x0
S:rxsp_rec_count 0x0
S:nc_start        0x0           tx_start          0x0
S:sync_start      0x0           sync_present      0x0
S:diag_auto       0x0           diag_speed        0xff

```

```

S:striped_wd_tov          3000          hw_wd_tov
    3000
S:step                    0x0          qsfp28_speed_mode
    0x0
S:qsfp_mode0_hw_sn_tries_left  0x0
S:qsfp_mode1_hw_sn_tries_left  0x0
S:
S:lksm variables:
S:-----
-----
S:proto_phyph            0xb8806a20    ov_lksm_hdl
0xb80108c0
sw_lksm_hdl              0xb8010960
num_lf1                  0
S:hw_link_tries_left    0          sw_link_tries_left    0
S:buf_ptype              0x0          stored_entry_state    0x6
S:handshake_owner       0x0          mark_unsent
    0x0
S:busybuf_stuck          0x0          lr_wait                0x0
S:
S:trksm variables:
S:-----
-----
S:Not a trunk port
S:
S:upsm variables:
S:-----
-----
S:proto_phyph            0xb8806a20    upsm_hdl
0xb8010aa0
S:bb_credits              0          port_beacon            0
S:port_diag_flag        0          force_offline
    0
S:port_fault_rsn         0: PORT_NO_FAULT
S:retry_init_rsn         0: UNKNOWN
S:linit_reason           0          linit_result            0
S:ie_fctl_mode           0          fec_in_sync_tries_left  0
S:retry_sn_fail_init     0
retry_link_fail_init     0
S:excess_lr_count        0
S:
S:c4_ch_cfg
S:-----
-----
S:c4_desc_ring_size      256      292      256      256      292
292      2      292
S:thresh_def             0          16          1          0
S:intr_tries             500          cmem_pattern
0xdeadbeef
S:cmem_pattern_upwd      2          cmem_init_time          16
S:cmem_init_tries        5
S:ctrl_par_thresh        2          data_par_thresh
4
S:cam_par_thresh         4          buf_loss_thresh

```

```

12
S:crit_par_thresh          2          non_crit_par_thresh
6
S:pci_abort_thresh        10          pci_err_thresh          5
S:excess_chintr_thresh    8          sw_err_thresh           20
S:err_sample_period       300        intr_sleep
20000
S:frame_timeout           2500        proxy_dev               16384
S:vf_route                81920       qos                     2048
S:stats                   2048        f_redirect              2048
S:rsp_trap                2048        lun_zoning              20480
S:area_mode               0          ftb_max_loop[0]        0
S:ftb_max_loop[1]         6          ftb_max_loop[2]        9
S:ftb_max_loop[3]         10         ftb_max_loop[4]        10
S:ftb_max_loop[5]         5          ftb_max_loop[6]        6
S:ftb_seg_size[0]         0          ftb_seg_size[1]
16384
S:ftb_seg_size[2]         65536      ftb_seg_size[3]
16384
S:ftb_seg_size[4]         16384      ftb_seg_size[5]
65536
S:ftb_seg_size[6]         16384      ftb_seg_base[0]        0
S:ftb_seg_base[1]         0          ftb_seg_base[2]
65536
S:ftb_seg_base[3]         16384      ftb_seg_base[4]
32768
S:ftb_seg_base[5]         131072    ftb_seg_base[6]
49152
asic_err_monitor_period1  300
asic_err_monitor_period2 86400
zone_chk_to_poll_period  25
zone_chk_class2_reject_tov 220
S:
S:c4_phy_cfg
S:-----
-----
S:version = 2.1
S:pt                      0x43028005    fab_ptr
0x9a800000
S:fabattr                 0x9a8000d4    fab_iop
0x9a800050
S:cfgbm                  0xbb8308c4    port_ctrl
0xb6abc118
S:pcap.pcap_bm           0x8d215547    pcap.pcap2_bm
0x2588289
S:pcap.pcap3_bm          0x1bebe0c
ui_idx                    62          S:slot_no
0
is_icl                    0          S:sw_usr_ports         400
S:neg_speed              0 0 0 0 0 0
S:my_domain              0x1          port_mode              0x0
S:hw_sn_maxtries         100        sw_sn_maxtries
0
S:hw_link_maxtries       10          sw_link_maxtries      5

```

```

S:rx_cyc_tov          28          rttov          300
S:bufrdy_tov         300         busybuf_tov    286
S:mark_tov           300         lksm_tov       3000
S:buf_dealloc_wait   4          hw_wd_tov      3000
S:hw_lk_train_tov    540        hw_lk_test_tov
    150
S:syswait_tx_12_lips 1          lip_rx_tov     55
S:al_time_tov        15         lp_tov         2000
S:intr_tries_port    500        intr_mod_debounce
    250
S:intr_lsrflt_debounce 500       intr_efifo_debounce 100
S:port_no_fid        3          excess_ptintr_thresh 8
S:port_fault1_thresh 100        port_fault1_spur_thresh 250
S:port_fault1_disc_thresh 500       losync_tov     100
port_fault1_disc_spur_thresh 1000
S:port_fault2_thresh 5          en_8g_scramble
S:port_sw_link_to    15
    1
frc_hw_sn_mode       0x1
S:enc_poll_thresh    0          fec_enable
    0
S:fec_in_sync_to     50         fec_in_sync_try_max
    4
S:port_be_lto_threshold 100       port_be_lr_threshold
    2
S:be_cr_in_sync_to   5
port_credit_overrun_thresh 10
S:jda_sfp_losig_tov  400
jda_sfp_losig_try_max 30
S:striped_wd_tov     3000
no_sync_debounce     1200
S:
S:    fab_iop
S:=====
S:fab_iop->interop_mode 0x0       fab_iop->lab_mode 0x0
S:fab_iop->fl_bbc       0x0       fab_iop->fl_fan
    0x0
S:fab_iop->fl_cls       0x4       fab_iop->fl_rscn
    0x0
S:fab_iop->domain_id_offset 0x60     fab_iop-
>mcdt_fabric_mode     0x0
S:fab_iop->mcdt_default_zone 0x0       fab_iop-
>mcdt_safe_zone       0x0
S:
S:    port_ctrl
S:=====
S:port_ctrl.port_type 1          port_ctrl.port_grp 0
S:port_ctrl.port_number 62       port_ctrl.vc_mode 1
S:
S:    port_ctrl.lcap
S:=====
S:has_serdes          0          has_media      1
S:topology            1          skip_nego      0
S:skip_pnego          0          skip_init_event 0

```

```

S:en_shim          0          speed_neg
    1
S:loop_back        0          num_speeds          5
S:fec_enable       0
S:
S:    port_ctrl.speed_list array
S:=====
S:speed_list[0].auto_neg 1    speed_list[0].lnk_speed 0x0000000a
S:speed_list[1].auto_neg 1    speed_list[1].lnk_speed 0x00000008
S:speed_list[2].auto_neg 1    speed_list[2].lnk_speed 0x00000006
S:speed_list[3].auto_neg 1    speed_list[3].lnk_speed 0x00000005
S:speed_list[4].auto_neg 1    speed_list[4].lnk_speed 0x00000003
S:speed_list[5].auto_neg 0    speed_list[5].lnk_speed 0x00000000
S:
S:    port_ctrl.cm
S:=====
S:port_ctrl.cm.num_vcs          8
S:port_ctrl.cm.min_bufs        8
S:port_ctrl.cm.cr_shar_bufs    0
S:port_ctrl.vc_alloc
S:port_ctrl.vc_alloc          2 0 1 1 1 1 1 1
S:port_ctrl.vc_alloc          0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.norm_vc_alloc
S:port_ctrl.norm_vc_alloc      4 0 5 5 5 5 1 1
S:port_ctrl.norm_vc_alloc      0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S:port_ctrl.cm.skip_bb_credit  0
S:port_ctrl.cm.use_shim_based_sublist 0
S:
S:    port_ctrl.serdes_set
S:=====
S:serdes_type          0x8
S:serdes_data_t.ibm_hss_serdes.tx_drive_power          0x1
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b_sign     0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_b          0x0
S:serdes_data_t.ibm_hss_serdes.pre_emphasis_a          0x0
S:serdes_data_t.ibm_hss_serdes.rxeq                    0x0
S:
S:    cfgbm
S:=====
S:old_distance          0x0          gport_lockdown          0x0
S:tport                0x1          speed                    0x0
S:disable_eport        0x0          fcacc                    0x0
S:lport_lockdown       0x0          priv_lport_lockdown     0x0
0x0
S:vcxlt_linit          0x0          delay_flogi              0x0
S:isl_interop          0x0          distance                  0x0
S:BufStarvFlag         0x0          credit_sharing            0x0
S:lport_halfduplex     0x0          lport_fairness            0x0
S:soft_neg             0x0          asn_frc_hwretry           0x0
S:cr_recov             0x0          fport_buffers             0x0
S:export               0x0          export_mode                0x0
0x0

```

S:csctl_en 0x0 mirror_port 0x0
S:fault_delay 0x0 non_dfe 0x0
S:fec_configured*(0=ENAB) 0 fec_tts
0

S:port_persistently_disabled (permanently) 0 (0)

S:

S: cfg property

S:=====

S:priv_pcfg_bm 0x00000000 lgcl_pcfg_bm
0xbb830904

S:fport_buffer 0x00000000

S:

S:

S:C4 Discard Cntrs: rxlp_stats = 0xb6abb470

S:-----

S:disc_mcast_wka 0x0 disc_inv_did 0x0

S:disc_cl1_cl4 0x0 disc_sid_chk_fail 0x0

S:disc_inv_dom_egid_txpt 0x0 disc_vft_hop_cnt_1
0x0

S:disc_classf 0x0 disc_fcp_cdb_inv 0x0

S:disc_vfid_trap_enabled 0x0

disc_vfid_hdr_chk_fail 0x0

S:disc_shim_cksum_fail 0x0 disc_fed_edit_cmd_err 0x0

S:disc_shim_cksum_fail 0x0 disc_fed_edit_cmd_err 0x0

S:disc_ftb_vm_mode 0x0 disc_ftb_agn_t2_miss 0x0

S:disc_ecb_de_pad_err 0x0 disc_ecb_de_tag_err 0x0

S:disc_ecb_de_seq_err 0x0 disc_ecb_err 0x0

S:disc_ftb_type4_match 0x0 disc_fcp_rsp_ftb_type4 0x0

S:disc_fcp_rsp_ftb_type4 0x0 disc_ftb_type5_match
0x0

S:disc_ftb_type3_match 0x0 disc_els_ftb_type3 0x0

S:disc_ftb_type1_match 0x0 disc_els_rsp_ex_port 0x0

S:disc_inv_drp_dps 0x0 disc_did_lookup_miss 0x0

S:disc_ftb_type2_match 0x0 disc_trpd_plogi_pdisc 0x0

S:disc_type2_lookup_miss 0x0 disc_ftb_type6_match
0x0

S:disc_els_rep_ex_port 0x0 disc_els_sid_lkup_bit1 0x0

S:disc_els_sid_lkup_bit0 0x0

disc_bls_frm_trap_bit1 0x0

S:disc_ftb_token_err 0x0 disc_asic_internal_err 0x0

S:disc_hard_zone_miss 0x0 disc_lun_zone_miss 0x0

S:discflt_frame_disc 0x0 discflt_parity_err 0x0

S:disc_frame_marked_du 0x0 disc_frame_marked_to 0x0

E:Connection type: FE

E:Port type: E_port

E:Trunk port: No

E:Configured Speed: AUTO_SPEED_NEGO

E:Max Capable Speed: 32G

E:Current SNSM Speed: UNDEFINED

E:Hardware TX Speed: 32G (0x00000004)

E:Hardware RX Speed: 32G (0x00000040)

E:

E:Interrupts: 0 Link_failure: 0

| | | | |
|-------------------|---|------------------|---|
| Loss_of_sync: | 0 | Loss_of_sig: | 0 |
| E:Lli: | 0 | Invalid_word: | 0 |
| E:trapped_frm: | 0 | fwd_status_ok: | 0 |
| E:fwd_timeout: | 0 | fwd_tx_unavail: | 0 |
| E:fwd_unroutable: | 0 | fwd_zone_out: | 0 |
| E:fwd_other_err: | 0 | frm_err_discard: | 0 |
| E:Fltr listA: | 0 | Fltr listB: | 0 |
| E:Zone trap fwd: | 0 | Zone trap disc: | 0 |
| E:shim_csum: | 0 | RTE_perr: | 0 |
| E:Invalid_crc: | 0 | Delim_err: | 0 |
| E:Protocol_err: | 0 | | |
| E:Lr_in: | 0 | Lr_out: | 0 |
| E:Ols_in: | 0 | Ols_out: | 0 |

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FILTER DATA

Shadow settings:

```

Filter Enable: 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass: 0x00000000

```

Real settings:

Enable RAM: 0x00000000, 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass RAM: 0x00000000

Shadowed filters:

Filter 0: Not Installed (MIRROR1)(LISTA)

c4_fldenable[0] = 0x00000000 0x00000000 0x00000000
0x00000000

c4_fldnegate[0] = 0x00000000, c4_fltr_config[0] = 0x00000000

Filter 1: Not Installed (MIRROR2)(LISTA)

c4_fldenable[1] = 0x00000000 0x00000000 0x00000000
0x00000000

c4_fldnegate[1] = 0x00000000, c4_fltr_config[1] = 0x00000000

Filter 2: Not Installed (MIRROR3)(LISTA)

c4_fldenable[2] = 0x00000000 0x00000000 0x00000000
0x00000000

c4_fldnegate[2] = 0x00000000, c4_fltr_config[2] = 0x00000000

Filter 3: Not Installed (MIRROR4)(LISTA)

c4_fldenable[3] = 0x00000000 0x00000000 0x00000000
0x00000000

c4_fldnegate[3] = 0x00000000, c4_fltr_config[3] = 0x00000000

Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
c4_fldenable[4] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[4] = 0x00000000,c4_fltr_config[4] = 0x00000000

Filter 5: Not Installed (ZONING TRAP)(LISTA)
c4_fldenable[5] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[5] = 0x00000000,c4_fltr_config[5] = 0x00000000

Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
c4_fldenable[6] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[6] = 0x00000000,c4_fltr_config[6] = 0x00000000

Filter 7: Not Installed (TIN TRAP)(LISTA)
c4_fldenable[7] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[7] = 0x00000000,c4_fltr_config[7] = 0x00000000

Filter 8: Not Installed (FICON CUP)(LISTA)
c4_fldenable[8] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[8] = 0x00000000,c4_fltr_config[8] = 0x00000000

Filter 9: Not Installed (FICON CUP DST)(LISTA)
c4_fldenable[9] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[9] = 0x00000000,c4_fltr_config[9] = 0x00000000

Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
c4_fldenable[10] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[10] = 0x00000000,c4_fltr_config[10] =
0x00000000

Filter 11: Not Installed (SIM)(LISTA)
c4_fldenable[11] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[11] = 0x00000000,c4_fltr_config[11] =
0x00000000

Filter 12: Not Installed (UNUSED)(LISTA)
c4_fldenable[12] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[12] = 0x00000000,c4_fltr_config[12] =
0x00000000

Filter 13: Not Installed (UNUSED)(LISTA)
c4_fldenable[13] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[13] = 0x00000000,c4_fltr_config[13] =
0x00000000

Filter 14: Not Installed (UNUSED)(LISTA)
c4_fldenable[14] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[14] = 0x00000000,c4_fltr_config[14] =
0x00000000

Filter 15: Not Installed (UNUSED)(LISTA)
c4_fldenable[15] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[15] = 0x00000000,c4_fltr_config[15] =
0x00000000

Filter 16: Not Installed (PERF1)(LISTA)
c4_fldenable[16] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[16] = 0x00000000,c4_fltr_config[16] =
0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
c4_fldenable[17] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[17] = 0x00000000,c4_fltr_config[17] =
0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
c4_fldenable[18] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[18] = 0x00000000,c4_fltr_config[18] =
0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
c4_fldenable[19] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[19] = 0x00000000,c4_fltr_config[19] =
0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
c4_fldenable[20] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[20] = 0x00000000,c4_fltr_config[20] =
0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
c4_fldenable[21] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[21] = 0x00000000,c4_fltr_config[21] =
0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
c4_fldenable[22] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[22] = 0x00000000,c4_fltr_config[22] =
0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
c4_fldenable[23] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[23] = 0x00000000,c4_fltr_config[23] =
0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
c4_fldenable[24] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[24] = 0x00000000,c4_fltr_config[24] =
0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
c4_fldenable[25] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[25] = 0x00000000,c4_fltr_config[25] =
0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
c4_fldenable[26] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[26] = 0x00000000,c4_fltr_config[26] =

```
0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
    c4_fldenable[27] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[27] = 0x00000000,c4_fltr_config[27] =
0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
    c4_fldenable[28] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[28] = 0x00000000,c4_fltr_config[28] =
0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
    c4_fldenable[29] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[29] = 0x00000000,c4_fltr_config[29] =
0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    c4_fldenable[30] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[30] = 0x00000000,c4_fltr_config[30] =
0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    c4_fldenable[31] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[31] = 0x00000000,c4_fltr_config[31] =
0x00000000
```

Real filters:

```
Filter 0: Not Installed (MIRROR1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
```

Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 7: Not Installed (TIN TRAP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 8: Not Installed (FICON CUP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 9: Not Installed (FICON CUP DST)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 11: Not Installed (SIM)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 12: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 13: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 14: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 15: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 16: Not Installed (PERF1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 17: Not Installed (PERF2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 18: Not Installed (PERF3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter 19: Not Installed (PERF4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,

0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter dirty indicator: 0x00000000
Performance filters: 0
Port Mirror filters: 0 (0x0)

FIELD DATA

Shadowed fields:

```
fldoffset[0] = 0x00, fldmask[0] = 0x00, fldvalue_dyna[0]:0x00 0x00
0x00 0x00
fldcontrol[0].inuse = 0x0  fldcontrol[0].refcnt = 0x00 0x00 0x00
0x00
fldoffset[1] = 0x00, fldmask[1] = 0x00, fldvalue_dyna[1]:0x00 0x00
0x00 0x00
fldcontrol[1].inuse = 0x0  fldcontrol[1].refcnt = 0x00 0x00 0x00
0x00
fldoffset[2] = 0x00, fldmask[2] = 0x00, fldvalue_dyna[2]:0x00 0x00
0x00 0x00
fldcontrol[2].inuse = 0x0  fldcontrol[2].refcnt = 0x00 0x00 0x00
0x00
fldoffset[3] = 0x00, fldmask[3] = 0x00, fldvalue_dyna[3]:0x00 0x00
0x00 0x00
fldcontrol[3].inuse = 0x0  fldcontrol[3].refcnt = 0x00 0x00 0x00
0x00
fldoffset[4] = 0x00, fldmask[4] = 0x00, fldvalue_dyna[4]:0x00 0x00
0x00 0x00
fldcontrol[4].inuse = 0x0  fldcontrol[4].refcnt = 0x00 0x00 0x00
0x00
fldoffset[5] = 0x00, fldmask[5] = 0x00, fldvalue_dyna[5]:0x00 0x00
0x00 0x00
fldcontrol[5].inuse = 0x0  fldcontrol[5].refcnt = 0x00 0x00 0x00
0x00
fldoffset[6] = 0x00, fldmask[6] = 0x00, fldvalue_dyna[6]:0x00 0x00
0x00 0x00
fldcontrol[6].inuse = 0x0  fldcontrol[6].refcnt = 0x00 0x00 0x00
0x00
fldoffset[7] = 0x00, fldmask[7] = 0x00, fldvalue_dyna[7]:0x00 0x00
0x00 0x00
fldcontrol[7].inuse = 0x0  fldcontrol[7].refcnt = 0x00 0x00 0x00
0x00
fldoffset[8] = 0x00, fldmask[8] = 0x00, fldvalue_dyna[8]:0x00 0x00
0x00 0x00
fldcontrol[8].inuse = 0x0  fldcontrol[8].refcnt = 0x00 0x00 0x00
0x00
fldoffset[9] = 0x00, fldmask[9] = 0x00, fldvalue_dyna[9]:0x00 0x00
0x00 0x00
fldcontrol[9].inuse = 0x0  fldcontrol[9].refcnt = 0x00 0x00 0x00
0x00
fldoffset[10] = 0x00, fldmask[10] = 0x00, fldvalue_dyna[10]:0x00 0x00
0x00 0x00
fldcontrol[10].inuse = 0x0  fldcontrol[10].refcnt = 0x00 0x00 0x00
0x00
fldoffset[11] = 0x00, fldmask[11] = 0x00, fldvalue_dyna[11]:0x00 0x00
0x00 0x00
fldcontrol[11].inuse = 0x0  fldcontrol[11].refcnt = 0x00 0x00 0x00
```


0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000
0x00000000

Field dirty indicator: 0x00000000

FDB reference count fdb: 0 [0 0 0 0]
FDB reference count fdb: 1 [0 0 0 0]
FDB reference count fdb: 2 [0 0 0 0]
FDB reference count fdb: 3 [0 0 0 0]
FDB reference count fdb: 4 [0 0 0 0]
FDB reference count fdb: 5 [0 0 0 0]
FDB reference count fdb: 6 [0 0 0 0]
FDB reference count fdb: 7 [0 0 0 0]
FDB reference count fdb: 8 [0 0 0 0]
FDB reference count fdb: 9 [0 0 0 0]
FDB reference count fdb: 10 [0 0 0 0]
FDB reference count fdb: 11 [0 0 0 0]
FDB reference count fdb: 12 [0 0 0 0]
FDB reference count fdb: 13 [0 0 0 0]
FDB reference count fdb: 14 [0 0 0 0]
FDB reference count fdb: 15 [0 0 0 0]
FDB reference count fdb: 16 [0 0 0 0]
FDB reference count fdb: 17 [0 0 0 0]
FDB reference count fdb: 18 [0 0 0 0]
FDB reference count fdb: 19 [0 0 0 0]

Filter counters:

Filter counter 0: 0 (MIRROR1)
Filter counter 1: 0 (MIRROR2)
Filter counter 2: 0 (MIRROR3)
Filter counter 3: 0 (MIRROR4)
Filter counter 4: 0 (AEPORT_NON_MIRR_DROP)
Filter counter 5: 0 (ZONING TRAP)
Filter counter 6: 0 (FCR_EXPORT_DC)
Filter counter 7: 0 (TIN TRAP)
Filter counter 8: 0 (FICON CUP)
Filter counter 9: 0 (FICON CUP DST)
Filter counter 10: 0 (WELL KNOWN ADDR)
Filter counter 11: 0 (SIM)
Filter counter 12: 0 (UNUSED)
Filter counter 13: 0 (UNUSED)
Filter counter 14: 0 (UNUSED)
Filter counter 15: 0 (UNUSED)
Filter counter 16: 0 (PERF1)
Filter counter 17: 0 (PERF2)
Filter counter 18: 0 (PERF3)
Filter counter 19: 0 (PERF4)
Filter counter 20: 0 (PERF5)
Filter counter 21: 0 (PERF6)
Filter counter 22: 0 (PERF7)

Filter counter 23: 0 (PERF8)
Filter counter 24: 0 (PERF9)
Filter counter 25: 0 (PERF10)
Filter counter 26: 0 (PERF11)
Filter counter 27: 0 (PERF12)
Filter counter 28: 0 (OPM1)
Filter counter 29: 0 (OPM2)
Filter counter 30: 0 (IPM1)
Filter counter 31: 0 (IPM2)

ACL DATA

Logical port 5: Hard Zoning disabled, Soft Zoning disabled
Zone type: WWN Zoning
Frames with hard zone miss: 0

*** Please use filterportshow on user port 56 to display ACL hash
tables and Mirroring resources of thischip.
***We show this data only for the first physical port which is an
external port.

portFcPortCmdShow --slot 0 63 3
doing portFcPortCmdShow: arg1 = 3, arg2 = -2

portshow 63
portDisableReason: None
portCFlags: 0x0
portFlags: 0x4021 PRESENT U_PORT DISABLED LED
LocalSwcFlags: 0x0
portType: 26.0
POD Port: Need license to enable the port
portState: 2 Offline
Protocol: FC
portPhys: 2 No_Module portScn: 2 Offline
port generation number: 0
state transition count: 0

portId: 013f00
portIfId: 43020007
portWwn: 20:3f:d8:1f:cc:2c:99:90
portWwn of device(s) connected:
16b Area list:
Distance: normal
portSpeed: N32Gbps

FEC: Inactive
Credit Recovery: Inactive
LE domain: 0
Peer beacon: Off
FC Fastwrite: OFF
Interrupts: 0
Unknown: 0

Link_failure: 0 Frjt:
Loss_of_sync: 0 Fbsy:

```

Lli:                0          Loss_of_sig: 0
Proc_rqrd:          0          Protocol_err: 0
Timed_out:          0          Invalid_word: 0
Tx_unavail:         0          Invalid_crc: 0
Delim_err:          0          Address_err: 0
Lr_in:              0          Ols_in:      0
Lr_out:             0          Ols_out:    0

```

portloginshow 63

```

Type  PID      World Wide Name      credit df_sz cos
=====

```

portloginshow 63 -history

```

Type  PID      World Wide Name      logout time
=====

```

portregshow 63

LED registers

=====

```

0x81c3a000: c4_led_status      00000000      0x81c3a004:
c4_led_ctl      00000000

```

FPL registers

=====

```

0x81c38200: fpl_port_config      23490000
0x81c3820c: fpl_port_id_ctl      00000000      0x81c38210:
fpl_port_id_addr      00013f00
0x81c38214: fpl_port_speed      00000004      0x81c3821c:
fpl_lli_ctl      00000903
0x81c38228: fpl_lli_os_ctl      bc95b5b5      0x81c3822c:
fpl_lli_send_word      bc95b5b5
0x81c38230: fpl_lli_mark_rx      00000000      0x81c38234:
fpl_lli_rnd_trip_time      00000000
0x81c38238: fpl_lli_ns_status      80070007      0x81c3823c:
fpl_lli_intr_status      80070007
0x81c38244: fpl_lli_def      00000000      0x81c38254:
fpl_lli_intr_enable_clr      00100000
0x81c38258: fpl_err_intr_status      00000000      0x81c38260:
fpl_err_intr_enable_clr      00000000
0x81c38268: fpl_err_first_error      00000000      0x81c3826c:
fpl_speed_neg_ctl      00000000
0x81c38270: fpl_speed_neg_stat      00000000      0x81c38274:
fpl_softasn_ctl      0000000f
0x81c38278: fpl_link_init_ctl      00000000      0x81c3827c:
fpl_link_init_stat      00000000
0x81c38280: fpl_aec_ctl      00051060      0x81c38284:
fpl_aec_ctl2      04009f60
0x81c38288: fpl_pcs_ctl      00000160      0x81c3828c:
fpl_fec_ctl      00000441
0x81c38290: fpl_fec_cor      00000000      0x81c38294:

```

```

fpl_fec_uncor          00000000
0x81c38298: fpl_hss_link_ctl      0031f040    0x81c3829c:
fpl_afifo_link_ctl    00000a86
0x81c382a0: fpl_echo_lb_ctl        0000028c    0x81c382a4:
fpl_scratch           00000121
0x81c382a8: fpl_debug              00030005    0x81c382ac:
fpl_misc_debug        00001800
0x00000000: SW_shadow_reg          00000000    0x00000000:
SW_c4_phyp->cfgptr    00030000

```

per-fpg (per octet) registers

```

=====
0x8180382c: fpg_serdes_ctla0      81a37be7    0x81803830:
fpg_serdes_ctla1      81a37be7
0x81803834: fpg_serdes_ctlb0      81a1c3c3    0x81803838:
fpg_serdes_ctlb1      81a1c3c3
0x8180383c: fpg_serdes_xgmii_1ms  00067c28    0x81803840:
fpg_serdes_regtimctl  40e47946
0x81803844: fpg_serdes_asnrsttimctl 00000102

```

HSS PLL registers

```

=====
0x81803400: 00_hssplla_vco_coarse_cal0  00000000    0x81803404:
01_hssplla_vco_coarse_cal1  00000014
0x81803408: 02_hssplla_vco_coarse_cal2  00000000    0x8180340c:
03_hssplla_vco_coarse_cal3  00000000
0x81803410: 04_hssplla_vco_coarse_cal4  00000000    0x81803424:
09_hssplla_power_ctl        00000000
0x81803428: 0A_hssplla_charge_pump_ctl  00000004    0x81803438:
0E_hssplla_pll_misc_ctl     00000000
0x8180343c: 0F_hssplla_pclk_ctl          000000f8    0x81803440:
10_hssplla_eyem_intv_ctl     00000000
0x81803444: 11_hssplla_eyem_intv_lim1      00000000    0x81803448:
12_hssplla_eyem_intv_lim2    00000000
0x8180344c: 13_hssplla_eyem_intv_lim3      00000000    0x81803450:
14_hssplla_eyem_intv_lim4    00000000
0x818034f0: 3C_hssplla_macro_tst_ctl4      00000000    0x818034f4:
3D_hssplla_macro_tst_ctl3    00000000
0x818034f8: 3E_hssplla_macro_tst_ctl2      00000000    0x818034fc:
3F_hssplla_macro_tst_ctl1    00000000
0x81803500: 00_hssppll_vco_coarse_cal0  0000000a    0x81803504:
01_hssppll_vco_coarse_cal1  00000014
0x81803508: 02_hssppll_vco_coarse_cal2  00000000    0x8180350c:
03_hssppll_vco_coarse_cal3  00000000
0x81803510: 04_hssppll_vco_coarse_cal4  00000000    0x81803524:
09_hssppll_power_ctl        00000000
0x81803528: 0A_hssppll_charge_pump_ctl  00000004    0x81803538:
0E_hssppll_pll_misc_ctl     00000000
0x8180353c: 0F_hssppll_pclk_ctl          000000f8    0x81803540:
10_hssppll_eyem_intv_ctl     00000000
0x81803544: 11_hssppll_eyem_intv_lim1      00000000    0x81803548:
12_hssppll_eyem_intv_lim2    00000000
0x8180354c: 13_hssppll_eyem_intv_lim3      00000000    0x81803550:
14_hssppll_eyem_intv_lim4    00000000

```

| | | |
|--------------------------------------|----------|-------------|
| 0x818035f0: 3C_hsspll macro_tst_ctl4 | 00000000 | 0x818035f4: |
| 3D_hsspll macro_tst_ctl3 | 00000000 | |
| 0x818035f8: 3E_hsspll macro_tst_ctl2 | 00000000 | 0x818035fc: |
| 3F_hsspll macro_tst_ctl1 | 00000000 | |

HSS TX registers

=====

| | | |
|---|----------|-------------|
| 0x81802500: 00_hsstx_cfg_mode_PHY | 00009f48 | 0x81802504: |
| 01_hsstx_test_ctl | 00000000 | |
| 0x81802508: 02_hsstx_coeff_ctl_INV | 00000000 | 0x8180250c: |
| 03_hsstx_drv_mode_ctl | 00000000 | |
| 0x81802510: 04_hsstx_drv_ovrd_ctl | 00000010 | 0x81802514: |
| 05_hsstx_dclk_align_ovrd | 00000080 | |
| 0x81802518: 06_hsstx_imp_cal_ovrd | 00000c0c | 0x8180251c: |
| 07_hsstx_dclk_drift_tol | 00000004 | |
| 0x81802520: 08_hsstx_tap0_coeff_TUNE | 00000000 | 0x81802524: |
| 09_hsstx_tap1_coeff_TUNE | 00000003 | |
| 0x81802528: 0A_hsstx_tap2_coeff_TUNE | 00000018 | 0x8180252c: |
| 0B_hsstx_tap3_coeff_TUNE | 0000000d | |
| 0x81802534: 0D_hsstx_pol_INV | 0000000a | 0x81802538: |
| 0E_hsstx_ae_cmd | 00000000 | |
| 0x8180253c: 0F_hsstx_ae_stat | 00000000 | 0x81802540: |
| 10_hsstx_ae_tap0_TUNE | 00000000 | |
| 0x81802544: 11_hsstx_ae_tap1_TUNE | 00000000 | 0x81802548: |
| 12_hsstx_ae_tap2_TUNE | 00000028 | |
| 0x8180254c: 13_hsstx_ae_tap3_TUNE | 00000000 | 0x81802554: |
| 15_hsstx_app_tune | 0000120e | |
| 0x81802558: 16_hsstx_analog_diag | 00000000 | 0x81802560: |
| 18_hsstx_4x_seg_app | 0000aafa | |
| 0x81802564: 19_hsstx_2x_seg_app | 00000000 | 0x81802568: |
| 1A_hsstx_1x_seg_app | 0000ff5d | |
| 0x8180256c: 1B_hsstx_seg_4x_term_app | 00000000 | 0x81802570: |
| 1C_hsstx_seg_2x1x_term_app | 00000f00 | |
| 0x81802574: 1D_hsstx_tap_sign_app | 0000000a | 0x81802578: |
| 1E_hsstx_ext_addr_data | 00000001 | |
| 0x8180257c: 1F_hsstx_ext_addr_addr | 00000000 | 0x81802580: |
| 20_hsstx_pat_buf_bytes_1_0 | 00000000 | |
| 0x81802584: 21_hsstx_pat_buf_bytes_3_2 | 00000000 | 0x81802588: |
| 22_hsstx_pat_buf_bytes_5_4 | 00000000 | |
| 0x8180258c: 23_hsstx_pat_buf_bytes_7_6 | 00000000 | 0x8180259c: |
| 27_hsstx_8023az_ctl | 00000000 | |
| 0x818025a0: 28_hsstx_dcc_ctl | 000060c0 | 0x818025a4: |
| 29_hsstx_dcc_ovrd | 00000000 | |
| 0x818025a8: 2A_hsstx_dcc_app | 00000102 | 0x818025ac: |
| 2B_hsstx_dcc_timeout | 0000ffff | |
| 0x818025c0: 30_hsstx_tap_sign_ovrd | 00000000 | 0x818025c8: |
| 32_hsstx_seg_4x_ovrd | 00000000 | |
| 0x818025cc: 33_hsstx_seg_2x_ovrd | 00000000 | 0x818025d0: |
| 34_hsstx_seg_1x_ovrd | 00000000 | |
| 0x818025d8: 36_hsstx_tap_seg_4x_term_ovrd | 00000000 | 0x818025dc: |
| 37_hsstx_tap_seg_2x_term_ovrd | 00000000 | |
| 0x818025e0: 38_hsstx_tap_seg_1x_term_ovrd | 00000000 | 0x818025ec: |
| 3B_hsstx_mac_test_ctl5 | 00000000 | |
| 0x818025f0: 3C_hsstx_mac_test_ctl4 | 00000000 | 0x818025f4: |

| | | |
|------------------------------------|----------|-------------|
| 3D_hsstx_mac_test_ctl3 | 00000000 | |
| 0x818025f8: 3E_hsstx_mac_test_ctl2 | 00000000 | 0x818025fc: |
| 3F_hsstx_mac_test_ctl1 | 000000c6 | |

HSS RX registers

=====

| | | |
|---|----------|-------------|
| 0x81802700: 00_hssrx_cfg_mode_PHY | 00009e78 | 0x81802704: |
| 01_hssrx_test_ctl | 00000000 | |
| 0x81802708: 02_hssrx_phs_rot_ctl | 0000cb80 | 0x8180270c: |
| 03_hssrx_phs_rot_ofs_ctl | 00003610 | |
| 0x81802710: 04_hssrx_phs_rot_posn1 | 00001818 | 0x81802714: |
| 05_hssrx_phs_rot_posn2 | 00000006 | |
| 0x81802718: 06_hssrx_phs_rot_sta_ofs1 | 00000f1f | 0x8180271c: |
| 07_hssrx_phs_rot_sta_ofs2 | 0000001f | |
| 0x81802720: 08_hssrx_dfe_ctl_PHY | 00002002 | 0x81802724: |
| 09_hssrx_dfe_smpl_snap1 | 00000000 | |
| 0x81802728: 0A_hssrx_dfe_smpl_snap2 | 00008000 | 0x8180272c: |
| 0B_hssrx_vga_ctl1 | 000041fc | |
| 0x81802730: 0C_hssrx_vga_ctl2 | 00007aa0 | 0x81802734: |
| 0D_hssrx_vga_ctl3 | 000009e4 | |
| 0x81802738: 0E_hssrx_pwr_mgmt_ctl | 0000001f | 0x8180273c: |
| 0F_hssrx_iqamp_ctl1 | 0000001a | |
| 0x81802740: 10_hssrx_iqamp_ctl2 | 00000007 | 0x81802744: |
| 11_hssrx_dacap_dacan_sel | 00000003 | |
| 0x81802748: 12_hssrx_dacap_dacan | 00000001 | 0x8180274c: |
| 13_hssrx_daca_min | 00000000 | |
| 0x81802750: 14_hssrx_adac_ctl | 00000000 | 0x81802754: |
| 15_hssrx_ac_cp_ctl | 000031c3 | |
| 0x81802758: 16_hssrx_ac_cp_val | 00008054 | 0x8180275c: |
| 17_hssrx_dfe_h1h2h3_lcl_off_ch | 00000014 | |
| 0x81802760: 18_hssrx_dfe_h1h2h3_lcl_off_val | 00000000 | 0x81802764: |
| 19_hssrx_peaked_intg | 000000ff | |
| 0x81802768: 1A_hssrx_cdr_analog_sw | 0000ce00 | 0x8180276c: |
| 1B_hssrx_peaking_amp_init_c_PHY | 00000000 | |
| 0x81802770: 1C_hssrx_dac_dpc | 00000040 | 0x81802774: |
| 1D_hssrx_ddc | 00000000 | |
| 0x81802778: 1E_hssrx_int_stat_PHY | 00000c0f | 0x8180277c: |
| 1F_hssrx_dfe_func_ctl1_PHY | 0000ffff | |
| 0x81802780: 20_hssrx_dfe_func_ctl2_INV | 00007eff | 0x81802784: |
| 21_hssrx_ofs_ch_dcc_qcc_idx | 00002000 | |
| 0x81802788: 22_hssrx_dfe_ofs_val | 00000379 | 0x8180278c: |
| 23_hssrx_h_coeff_bist | 00000401 | |
| 0x81802790: 24_hssrx_ac_cap_bist | 00000000 | 0x81802794: |
| 25_hssrx_max_gain_path_idx_res | 00007800 | |
| 0x81802798: 26_hssrx_loff_ctl | 00000040 | 0x8180279c: |
| 27_hssrx_sigdet_ctl | 00004880 | |
| 0x818027a0: 28_hssrx_ana_ctl_sw | 00000000 | 0x818027a4: |
| 29_hssrx_intg_dac_ofs | 0000dfe3 | |
| 0x818027a8: 2A_hssrx_eye_ctl | 00000000 | 0x818027ac: |
| 2B_hssrx_eye_met | 00000004 | |
| 0x818027b0: 2C_hssrx_eye_met_err_cnt | 00000000 | 0x818027b4: |
| 2D_hssrx_eye_met_pdf_eyec | 00000000 | |
| 0x818027b8: 2E_hssrx_eye_met_pat_len | 0000007f | 0x818027bc: |
| 2F_hssrx_dfe_func_ctl3 | 0000dfff | |

| | | | |
|--|--------------------------|-------------|------|
| 0x818027c0: 30_hssrx_dfe_tap_ctl_idx_ptr | 00000008 | 0x818027c4: | |
| 31_hssrx_dfe_tap | 00003030 | | |
| 0x818027c8: 32_hssrx_lte_ctl_TUNE | 00001601 | 0x818027e4: | |
| 39_hssrx_int_stat2 | 0000c1ff | | |
| 0x818027e8: 3A_hssrx_ac_cpl_cur_src_adj | 00000043 | 0x818027ec: | |
| 3B_hssrx_dcd_ctl | 00007c49 | | |
| 0x818027f0: 3C_hssrx_dcc_ctl | 00000d41 | 0x818027f4: | |
| 3D_hssrx_qcc_ctl | 00006981 | | |
| 0x818027f8: 3E_hssrx_mac_test_ctl2 | 00000000 | 0x818027fc: | |
| 3F_hssrx_mac_test_ctl1 | 00000000 | | |
| 0x81802748: 12_hssrx_dacap_dacan[02] | 0100 0001 | | |
| 0x81802760: 18_hssrx_dfe_h1h2h3_lcl_off_va[00] | 0000 0000 0000 | | 0000 |
| 0000 0000 0000 0000 0000 | | | |
| 0x81802760: 18_hssrx_dfe_h1h2h3_lcl_off_va[08] | 0000 0000 0000 | | 0000 |
| 0000 0000 0000 0000 0000 | | | |
| 0x81802760: 18_hssrx_dfe_h1h2h3_lcl_off_va[16] | 0000 0000 0000 | | 0000 |
| 0000 0000 | | | |
| 0x81802788: 22_hssrx_dfe_ofs_val[00][00] | 007f 7e05 007e | 0379 7f00 | 7a09 |
| 0x81802788: 22_hssrx_dfe_ofs_val[03][00] | 7f00 7909 007f | 7901 007f | 7f7b |
| 0x81802788: 22_hssrx_dfe_ofs_val[06][00] | 7f7f 0303 7f7f | 0b7b 7f00 | 097d |
| 0x81802788: 22_hssrx_dfe_ofs_val[09][00] | 7f7f 7d79 0000 | 0707 7f7f | 030b |
| 0x81802788: 22_hssrx_dfe_ofs_val[12][00] | 7f7f 7f79 7f00 | 7b06 007f | 0303 |
| 0x81802788: 22_hssrx_dfe_ofs_val[15][00] | 7f7f 0f7e 7f00 | 037e 7f00 | 0305 |
| 0x81802788: 22_hssrx_dfe_ofs_val[18][00] | 7f7f 0001 007f | 037f 0000 | 0306 |
| 0x81802788: 22_hssrx_dfe_ofs_val[21][00] | 007f 0001 007f | 0001 007f | 0001 |
| 0x81802788: 22_hssrx_dfe_ofs_val[24][00] | 007f 7f7b 0000 | 7e79 7f00 | 7a03 |
| 0x81802794: 25_hssrx_max_gain_path_idx_res[00] | 18a8 20cf 28aa 308f 3800 | 005c 0846 | 1112 |
| 0x81802794: 25_hssrx_max_gain_path_idx_res[08] | 5801 6040 6802 7000 7800 | 40af 488a | 507b |
| 0x818027c4: 31_hssrx_dfe_tap[00] | 0000 0030 0030 3030 3030 | fffe 8181 | 0000 |
| 0x818027c4: 31_hssrx_dfe_tap[08] | 0000 | 3030 3030 | 3030 |
| 0x818027e8: 3A_hssrx_ac_cpl_cur_src_adj[00] | 0043 | 0043 0043 | 0043 |
| 0x818027ec: 3B_hssrx_dcd_ctl[00] | 5c00 7c44 | 7c49 5c00 | 7c43 |
| 0x818027f0: 3C_hssrx_dcc_ctl[00] | 0d00 | 0d41 0d82 | 0d83 |
| 0x818027f4: 3D_hssrx_qcc_ctl[00] | | 6945 6981 | |

xfipcs, fec, aec, & aet registers

=====

| | |
|------------------------|---------------------------------|
| 0x81c38400: xfipcs_reg | [00] 00002040 00000080 00000000 |
|------------------------|---------------------------------|


```

00000000 00000001 00000008 00000000 00000000
0x81c38420: xfipcs_reg [08] 00008c01 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c38440: xfipcs_reg [16] 00000000 00000000 00000000
00000000 00000040 00000000 00000000 00000000
0x81c38460: xfipcs_reg [24] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c38480: xfipcs_reg [32] 00000004 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c38620: fec_32g_128g_reg [08] 00000000 00000000 00000000
00000000 00000000 00000000 00000000
0x81c38648: fec_32g_128g_reg [18] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c38a00: aec_reg [00] 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
0x81c38c00: aet_reg [00] 00000000 00000000 00000000
00000000 00000000

```

bbc registers

=====

```

0x81c39800: bbc_trc 0 0 0 0 0 0 0
0
0x81c39840: bbc_trc 0 0 0 0 0 0 0
0
0x81c39880: bbc_trc 0 0 0 0 0 0 0
0
0x81c398c0: bbc_trc 0 0 0 0 0 0 0
0
0x81c39900: bbc_trc 0 0 0 0 0 0 0
0
0x81c39804: bbc_mbc 0 0 0 0 0 0 0
0
0x81c39844: bbc_mbc 0 0 0 0 0 0 0
0
0x81c39884: bbc_mbc 0 0 0 0 0 0 0
0
0x81c398c4: bbc_mbc 0 0 0 0 0 0 0
0
0x81c39904: bbc_mbc 0 0 0 0 0 0 0
0
0x81c39a00: bbc_rcc 0 0 0 0 0 0 0
0
0x81c39a20: bbc_rcc 0 0 0 0 0 0 0
0
0x81c39a40: bbc_rcc 0 0 0 0 0 0 0
0
0x81c39a60: bbc_rcc 0 0 0 0 0 0 0
0
0x81c39a80: bbc_rcc 0 0 0 0 0 0 0
0
0x81c39c00: bbc_rqc 0 0 0 0 0 0 0
0
0x81c39c20: bbc_rqc 0 0 0 0 0 0 0
0

```

| | | | | | | | |
|-------------------------------------|----------|---|---|---|---|----------------------|---|
| 0x81c39c40: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c39c60: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c39c80: bbc_rqc | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | | | | |
| 0x81c39d00: bbc_fbpc | 00000000 | | | | | 0x81c39d04: bbc_csc | |
| 00000000 | | | | | | | |
| 0x81c39d08: bbc_rcc_inc | 00000000 | | | | | 0x81c39d0c: | |
| bbc_rqc_inc | 00000000 | | | | | | |
| 0x81c39d10: bbc_fbpc_inc | 00000000 | | | | | 0x81c39d14: | |
| bbc_tmc_inc | 00000000 | | | | | | |
| 0x81c39d18: bbc_threshold | 00080100 | | | | | 0x81c39d1c: | |
| bbc_counter_clr | 00000000 | | | | | | |
| 0x81c39d20: bbc_debug_en | 00000000 | | | | | 0x81c39d24: bbc_ctrl | |
| 00200020 | | | | | | | |
| 0x81c39d28: bbc_rqc_rcc_thresh | 00000055 | | | | | 0x81c39d34: | |
| bbc_bb_sc_n | 00000000 | | | | | | |
| 0x81c39d38: bbc_crd_reco_debug | 00000000 | | | | | 0x81c39d3c: | |
| bbc_crd_reco_debug_data | 00000000 | | | | | | |
| 0x81c39d40: bbc_multi_frm_loss_cnt | 00000000 | | | | | 0x81c39d44: | |
| bbc_multi_rdy_loss_cnt | 00000000 | | | | | | |
| 0x81c39d48: bbc_1frm_loss_recov_cnt | 00000000 | | | | | 0x81c39d4c: | |
| bbc_1rdy_loss_recov_cnt | 00000000 | | | | | | |
| 0x81c39d58: bbc_int_status | 00000000 | | | | | 0x81c39d5c: | |
| bbc_int_set | 00000000 | | | | | | |
| 0x81c39d60: bbc_int_first | 00000000 | | | | | 0x81c39d64: | |
| bbc_frm_rdy_rx_err_addr | 00000000 | | | | | | |
| 0x81c39d68: bbc_frm_rdy_tx_err_addr | 00000000 | | | | | 0x81c39d6c: | |
| bbc_trc_mbc_err_addr | 00000000 | | | | | | |
| 0x81c39d70: bbc_frm_rdy_rx_dbl_ecc | 00000000 | | | | | 0x81c39d74: | |
| bbc_frm_rdy_tx_dbl_ecc | 00000000 | | | | | | |
| 0x81c39d78: bbc_trc_mbc_dbl_ecc | 00000000 | | | | | | |
| 0x81c39d7c: bbc_fsm_status | 00001011 | | | | | 0x81c39d80: | |
| bbc_force_err | 00000000 | | | | | | |
| 0x81c39d84: bbc_crdt_avail0 | ffffffff | | | | | 0x81c39d88: | |
| bbc_crdt_avail1 | 000000ff | | | | | | |
| 0x81c39d8c: bbc_scratch | 00000000 | | | | | | |

FPS registers

=====

| | | | | | | | |
|----------------------------|----------|--|--|--|--|-------------|--|
| 0x81c38004: fps_er_enc_in | 00000000 | | | | | 0x81c38008: | |
| fps_er_crc | 00000000 | | | | | | |
| 0x81c3800c: fps_er_trunc | 00000000 | | | | | 0x81c38010: | |
| fps_er_toolong | 00000000 | | | | | | |
| 0x81c38014: fps_er_bad_eof | 00000000 | | | | | 0x81c38018: | |
| fps_er_enc_out | 00000000 | | | | | | |
| 0x81c3801c: fps_er_bad_os | 00000000 | | | | | 0x81c38020: | |
| fps_er_flush | 00000000 | | | | | | |
| 0x81c38024: fps_er_ifg | 00000000 | | | | | 0x81c38038: | |
| fps_er_crc_good_eof | 00000000 | | | | | | |
| 0x81c3803c: fps_inv_arb | 00000000 | | | | | 0x81c38040: | |
| fps_slow_sts_status | 00000000 | | | | | | |
| 0x81c38044: fps_tx_frm_cnt | 00000000 | | | | | 0x81c38048: | |

```

fps_rx_frm_cnt          00000000
0x81c38050: fps_tx_word_cnt_hi      00000000    0x81c3804c:
fps_tx_word_cnt_lo      00000000
0x81c38058: fps_rx_word_cnt_hi      00000000    0x81c38054:
fps_rx_word_cnt_lo      00000000

```

BAL registers

=====

```

0x81c3f000: bal_desired_buf          00000000    0x81c3f004:
bal_alloc_buf           00000000
0x81c3f008: bal_busy_buf              00000000    0x81c3f00c:
bal_usable_buf          00000000
0x81c3f010: bal_max_bor_buf          00000000
0x81c3f014: bal_busy_buf_thresh      00000002

```

TXQ registers

=====

```

0x81c3b004: txq_phys_port_ctl          00470000
0x81c3b050: txq_link_skew                00000000
0x81c3b068: txq_cr_lk_dttm_intr_sts [00] 00000000 00000000
0x81c3b070: txq_cr_lk_dttm_intr_en [00] 00000000 00000000
0x81c3b024: txq_disc_frm_trap_cnt        00000014

```

FDS registers

=====

```

0x81c3c000: fds_rxf_ctl                    00000002    0x81c3c004:
fds_rxf_wait_thresh     00000909
0x81c3c018: fds_rxf_first_error          00000000    0x81c3c01c:
fds_rxf_first_error_info 00000000
0x81c3c020: fds_rxf_inout_pkt_cnt        00000000
0x81c3c008: fds_rxf_err_int_status      00000000    0x81c3c024:
fds_rxf_fifo_status     00888888
0x81c3d000: fds_txf_ctl                    0000003a    0x81c3d004:
fds_txf_wait_ifg_thresh 00a00106
0x81c3d008: fds_txf_err_int_status      00000000    0x81c3d024:
fds_txf_fifo_status     00088888
0x81c3d02c: fds_txf_bbc_scs            00000000

```

Logical TXQ registers

=====

```

0x81c3b000: txq_log_port_ctl          00000002    0x81c3b008:
txq_port_status         00000000
0x81c3b00c: txq_todo_flags              [00] 00000000 00000000
0x81c3b014: txq_spd_match_desc          [00] 00000000 00000000 00000000
00000000
0x81c3b024: txq_spd_match_desc          [04] 00000014
0x81c3b028: txq_vc_weight              [00] 01010101 01010101 01010101
01010101
0x81c3b038: txq_vc_weight              [04] 01010101 01010101 01010101
01010101
0x81c3b048: txq_vc_weight              [08] 01010101 00010101
0x81c3b054: txq_cong_dttm_ctrl          00000000
0x81c3b058: txq_cong_dttm_intr_sts     [00] 00000000 00000000
0x81c3b060: txq_cong_dttm_intr_en      [00] 00000000 00000000

```

| | | | | |
|---------------------------------|------|----------|----------|----------|
| 0x81c3b078: txq_bw_limit_en_reg | [00] | 00000000 | 00000000 | |
| 0x81c3b080: txq_bw_gua_en_reg | [00] | 00000000 | 00000000 | |
| 0x81c3b088: txq_vc_group | [00] | 03030300 | 03030303 | 03030303 |
| 03030303 | | | | |
| 0x81c3b098: txq_vc_group | [04] | 03030303 | 03030303 | 03030303 |
| 03030303 | | | | |
| 0x81c3b0a8: txq_vc_group | [08] | 03030303 | 03030303 | 00000000 |
| 00000000 | | | | |
| 0x81c3b0b0: txq_bw_thresh_group | [00] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c3b0c0: txq_bw_thresh_group | [04] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c3b0d0: txq_bw_thresh_group | [08] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c3b0e0: txq_bw_thresh_group | [12] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c3b0f0: txq_bw_thresh_group | [16] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c3b100: txq_bw_thresh_group | [20] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c3b110: txq_bw_thresh_group | [24] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c3b120: txq_bw_thresh_group | [28] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c3b130: txq_bw_thresh_group | [32] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |
| 0x81c3b140: txq_bw_thresh_group | [36] | 00000000 | 00000000 | 00000000 |
| 00000000 | | | | |

txq Congestion detection Statistics RAM

=====

| | | |
|--------------------|----------|--------------------|
| 0x81090460: vc[0] | 00000000 | 0x81090464: vc[1] |
| 00000000 | | |
| 0x81090468: vc[2] | 00000000 | 0x8109046c: vc[3] |
| 00000000 | | |
| 0x81090470: vc[4] | 00000000 | 0x81090474: vc[5] |
| 00000000 | | |
| 0x81090478: vc[6] | 00000000 | 0x8109047c: vc[7] |
| 00000000 | | |
| 0x81090480: vc[8] | 00000000 | 0x81090484: vc[9] |
| 00000000 | | |
| 0x81090488: vc[10] | 00000000 | 0x8109048c: vc[11] |
| 00000000 | | |
| 0x81090490: vc[12] | 00000000 | 0x81090494: vc[13] |
| 00000000 | | |
| 0x81090498: vc[14] | 00000000 | 0x8109049c: vc[15] |
| 00000000 | | |
| 0x810904a0: vc[16] | 00000000 | 0x810904a4: vc[17] |
| 00000000 | | |
| 0x810904a8: vc[18] | 00000000 | 0x810904ac: vc[19] |
| 00000000 | | |
| 0x810904b0: vc[20] | 00000000 | 0x810904b4: vc[21] |
| 00000000 | | |
| 0x810904b8: vc[22] | 00000000 | 0x810904bc: vc[23] |

```

00000000
0x810904c0: vc[24]      00000000      0x810904c4: vc[25]
00000000
0x810904c8: vc[26]      00000000      0x810904cc: vc[27]
00000000
0x810904d0: vc[28]      00000000      0x810904d4: vc[29]
00000000
0x810904d8: vc[30]      00000000      0x810904dc: vc[31]
00000000
0x810904e0: vc[32]      00000000      0x810904e4: vc[33]
00000000
0x810904e8: vc[34]      00000000      0x810904ec: vc[35]
00000000
0x810904f0: vc[36]      00000000      0x810904f4: vc[37]
00000000
0x810904f8: vc[38]      00000000      0x810904fc: vc[39]
00000000

```

Logical STS registers

=====

```

0x815845c4: sts_ftb_type1_miss      00000000
0x815845c8: sts_ftb_type2_miss      00000000
0x815845cc: sts_ftb_type6_miss      00000000
0x815845d0: sts_hard_zoning_miss    00000000
0x815845d4: sts_lun_zoning_miss     00000000
0x815845dc: sts_unroutable          00000000
0x815815f4: sts_rte_cl2             00000000      0x815815f8:
sts_rte_cl3             00000000      0x815815fc: sts_rte_link_ctl
00000000      0x815845e8: sts_tx_timeout          00000000

```

Logical STS filter registers

=====

```

0x81584540: stsflt_trig [00] 00000000 00000000 00000000
00000000
0x81584550: stsflt_trig [04] 00000000 00000000 00000000
00000000
0x81584560: stsflt_trig [08] 00000000 00000000 00000000
00000000
0x81584570: stsflt_trig [12] 00000000 00000000 00000000
00000000
0x81584580: stsflt_trig [16] 00000000 00000000 00000000
00000000
0x81584590: stsflt_trig [20] 00000000 00000000 00000000
00000000
0x815845a0: stsflt_trig [24] 00000000 00000000 00000000
00000000
0x815845b0: stsflt_trig [28] 00000000 00000000 00000000
00000000
0x815845c0: stsflt_trig [32]

```

Logical STS discard registers

=====

```

0x81581a2c: disc_mcast_wka      00000000      0x81581a30:

```

```

disc_inv_did          00000000
0x81581a34: disc_cl1_cl4          00000000    0x81581a38:
disc_sid_chk_fail    00000000
0x81581a3c: disc_inv_dom_egid_txpt 00000000    0x81581a40:
disc_vft_hop_cnt_1   00000000
0x81581a44: disc_classf          00000000    0x81581a48:
disc_fcp_cdb_inv     00000000
0x81581a4c: disc_vfid_trap_enabled 00000000    0x81581a50:
disc_vfid_hdr_chk_fail 00000000
0x81581a54: disc_shim_cksum_fail 00000000    0x81581a58:
disc_fed_edit_cmd_err 00000000
0x81581a5c: disc_ftb_vm_mode      00000000    0x81581a60:
disc_ftb_agnt2_miss  00000000
0x81581a64: disc_ecb_reserved    00000000    0x81581a68:
disc_ecb_de_pad_err  00000000
0x81581a6c: disc_ecb_de_tag_err  00000000    0x81581a70:
disc_ecb_de_seq_err  00000000
0x81581a74: disc_ecb_err          00000000    0x81581a78:
disc_ftb_type4_match 00000000
0x81581a7c: disc_fcp_rsp_ftb_type4 00000000    0x81581a80:
disc_ftb_type5_match 00000000
0x81581a84: disc_ftb_type3_match 00000000    0x81581a88:
disc_els_ftb_type3   00000000
0x81581a8c: disc_ftb_type1_match 00000000    0x81581a90:
disc_els_rsp_ex_port 00000000
0x81581a94: disc_inv_drp_dps     00000000    0x81581a98:
disc_did_lookup_miss 00000000
0x81581a9c: disc_ftb_type2_match 00000000    0x81581aa0:
disc_trpd_plogi_pdisc 00000000
0x81581aa4: disc_type2_lookup_miss 00000000    0x81581aa8:
disc_ftb_type6_match 00000000
0x81581aac: disc_els_rep_ex_port 00000000    0x81581ab0:
disc_els_sid_lkup_bit1 00000000
0x81581ab4: disc_els_sid_lkup_bit0 00000000    0x81581ab8:
disc_bls_frm_trap_bit1 00000000
0x81581abc: disc_ftb_token_err   00000000    0x81581ac0:
disc_asic_internal_err 00000000
0x81581ac4: disc_hard_zone_miss  00000000    0x81581ac8:
disc_lun_zone_miss   00000000
0x81581acc: discflt_frame_disc   00000000    0x81581ad0:
discflt_parity_err   00000000
0x81581ad4: disc_frame_marked_du 00000000    0x81581ad8:
disc_frame_marked_to 00000000
0x81581adc: disc_lkup_rte_prty_err 00000000

```

portstatsshow 63

```

stat_wtx          0          4-byte words transmitted
stat_wrx          0          4-byte words received
stat_ftx          0          Frames transmitted
stat_frx          0          Frames received
stat_c2_frx       0          Class 2 frames received
stat_c3_frx       0          Class 3 frames received
stat_lc_rx        0          Link control frames

```

| | | | | | |
|------------------------------|------------|-----|-----|----------|-------------------------|
| received | | | | | |
| stat_mc_rx | 0 | | | | Multicast frames |
| received | | | | | |
| stat_mc_to | 0 | | | | Multicast timeouts |
| stat_mc_tx | 0 | | | | Multicast frames |
| transmitted | | | | | |
| tim_txcrd_z | 0 | | | | Time TX Credit Zero |
| (2.5Us ticks) | | | | | |
| tim_txcrd_z_vc 0- 3: | 0 | 0 | 0 | 0 | |
| tim_txcrd_z_vc 4- 7: | 0 | 0 | 0 | 0 | |
| tim_txcrd_z_vc 8-11: | 0 | 0 | 0 | 0 | |
| tim_txcrd_z_vc 12-15: | 0 | 0 | 0 | 0 | |
| lat_tot_pkt_vc 0- 3: | 1 | 1 | 1 | 1 | |
| lat_tot_pkt_vc 4- 7: | 1 | 1 | 1 | 1 | |
| lat_tot_pkt_vc 8-11: | 1 | 1 | 1 | 1 | |
| lat_tot_pkt_vc 12-15: | 1 | 1 | 1 | 1 | |
| lat_hi_time_vc 0- 3: | 0 | 0 | 0 | 0 | |
| lat_hi_time_vc 4- 7: | 0 | 0 | 0 | 0 | |
| lat_hi_time_vc 8-11: | 0 | 0 | 0 | 0 | |
| lat_hi_time_vc 12-15: | 0 | 0 | 0 | 0 | |
| lat_lo_time_vc 0- 3: | 1 | 1 | 1 | 1 | |
| lat_lo_time_vc 4- 7: | 1 | 1 | 1 | 1 | |
| lat_lo_time_vc 8-11: | 1 | 1 | 1 | 1 | |
| lat_lo_time_vc 12-15: | 1 | 1 | 1 | 1 | |
| max_latency_vc 0- 3: | 1 | 1 | 1 | 1 | |
| max_latency_vc 4- 7: | 1 | 1 | 1 | 1 | |
| max_latency_vc 8-11: | 1 | 1 | 1 | 1 | |
| max_latency_vc 12-15: | 1 | 1 | 1 | 1 | |
| latency_dma_ts | 09-09-2024 | UTC | Mon | 08:47:27 | TXQ |
| Latency DMA TimeStamp | | | | | |
| fec_cor_detected | 0 | | | | Count of blocks that |
| were corrected by FEC | | | | | |
| fec_uncor_detected | 0 | | | | Count of blocks that |
| were left uncorrected by FEC | | | | | |
| er_enc_in | 0 | | | | Encoding errors inside |
| of frames | | | | | |
| er_crc | 0 | | | | Frames with CRC errors |
| er_trunc | 0 | | | | Frames shorter than |
| minimum | | | | | |
| er_toolong | 0 | | | | Frames longer than |
| maximum | | | | | |
| er_bad_eof | 0 | | | | Frames with bad end-of- |
| frame | | | | | |
| er_enc_out | 0 | | | | Encoding error outside |
| of frames | | | | | |
| er_bad_os | 0 | | | | Invalid ordered set |
| er_pcs_blk | 0 | | | | PCS block errors |
| er_rx_c3_timeout | 0 | | | | Class 3 receive frames |
| discarded due to timeout | | | | | |
| er_tx_c3_timeout | 0 | | | | Class 3 transmit frames |
| discarded due to timeout | | | | | |
| er_unroutable | 0 | | | | Frames that are |
| unroutable | | | | | |
| er_unreachable | 0 | | | | Frame with unreachable |

| | | |
|-----------------------|-----------------------------|--------------------------|
| destination | | |
| er_other_discard | 0 | Other discards |
| er_type1_miss | 0 | frames with FTB type 1 |
| miss | | |
| er_type2_miss | 0 | frames with FTB type 2 |
| miss | | |
| er_type6_miss | 0 | frames with FTB type 6 |
| miss | | |
| er_zone_miss | 0 | frames with hard zoning |
| miss | | |
| er_lun_zone_miss | 0 | frames with LUN zoning |
| miss | | |
| er_crc_good_eof | 0 | Crc error with good eof |
| er_inv_arb | 0 | Invalid ARB |
| er_single_credit_loss | 0 | Single vcrdy/frame loss |
| on link | | |
| er_multi_credit_loss | 0 | Multiple vcrdy/frame |
| loss on link | | |
| other_credit_loss | 0 | Link timeout/complete |
| credit loss | | |
| phy_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | Timestamp of |
| phy_port stats clear | | |
| lgc_stats_clear_ts | 09-06-2024 UTC Fri 08:30:19 | Timestamp of |
| lgc_port stats clear | | |
| fec_corrected_rate | 0 | FEC Corrected blocks per |
| second | | |

portstats64show 63

| | | |
|---------------|---|--|
| stat64_wtx | 0 | top_int : 4-byte words transmitted |
| | 0 | bottom_int : 4-byte words transmitted |
| stat64_wrx | 0 | top_int : 4-byte words received |
| | 0 | bottom_int : 4-byte words received |
| stat64_ftx | 0 | top_int : Frames transmitted |
| | 0 | bottom_int : Frames transmitted |
| stat64_frx | 0 | top_int : Frames received |
| | 0 | bottom_int : Frames received |
| stat64_c2_frx | 0 | top_int : Class 2 frames received |
| | 0 | bottom_int : Class 2 frames received |
| stat64_c3_frx | 0 | top_int : Class 3 frames received |
| | 0 | bottom_int : Class 3 frames received |
| stat64_lc_rx | 0 | top_int : Link control frames received |
| | 0 | bottom_int : Link control frames |
| received | | |
| stat64_mc_rx | 0 | top_int : Multicast frames received |
| | 0 | bottom_int : Multicast frames received |
| stat64_mc_to | 0 | top_int : Multicast timeouts |
| | 0 | bottom_int : Multicast timeouts |
| stat64_mc_tx | 0 | top_int : Multicast frames transmitted |
| | 0 | bottom_int : Multicast frames |
| transmitted | | |
| tim64_rdy_pri | 0 | top_int : Time R_RDY high priority |
| | 0 | bottom_int : Time R_RDY high priority |
| tim64_txcrd_z | 0 | top_int : Time BB_credit zero |
| | 0 | bottom_int : Time BB_credit zero |

| | | |
|---|---|--|
| er64_enc_in | 0 | top_int : Encoding errors inside of |
| frames | 0 | bottom_int : Encoding errors inside of |
| frames | | |
| er64_crc | 0 | top_int : Frames with CRC errors |
| | 0 | bottom_int : Frames with CRC errors |
| er64_trunc | 0 | top_int : Frames shorter than minimum |
| | 0 | bottom_int : Frames shorter than minimum |
| er64_toolong | 0 | top_int : Frames longer than maximum |
| | 0 | bottom_int : Frames longer than maximum |
| er64_bad_eof | 0 | top_int : Frames with bad end-of-frame |
| | 0 | bottom_int : Frames with bad end-of- |
| frame | | |
| er64_enc_out | 0 | top_int : Encoding error outside of |
| frames | 0 | bottom_int : Encoding error outside of |
| frames | | |
| er64_disc_c3 | 0 | top_int : Class 3 frames discarded |
| | 0 | bottom_int : Class 3 frames discarded |
| er64_pcs_blk | 0 | top_int : PCS block errors |
| | 0 | bottom_int : PCS block errors |
| stat64_rateTxFrame | 0 | Tx frame rate (fr/sec) |
| stat64_rateRxFrame | 0 | Rx frame rate (fr/sec) |
| stat64_rateTxPeakFrame | 0 | Tx peak frame rate (fr/sec) |
| stat64_rateRxPeakFrame | 0 | Rx peak frame rate (fr/sec) |
| stat64_rateTxWord | 0 | Tx Word rate (words/sec) |
| stat64_rateRxWord | 0 | Rx Word rate (words/sec) |
| stat64_rateTxPeakWord | 0 | Tx peak Word rate (words/sec) |
| stat64_rateRxPeakWord | 0 | Rx peak Word rate (words/sec) |
| stat64_PRJTFrames | 0 | top_int : Number of PRJT frames |
| returned to this port | 0 | bottom_int : Number of PRJT |
| frames returned to this port | | |
| stat64_PBSYFrames | 0 | top_int : Number of PBSY frames |
| returned to this port | 0 | bottom_int : Number of PBSY |
| frames returned to this port | | |
| stat64_inputBuffersFull | 0 | top_int : Number of occurrences |
| when all input buffers full | 0 | bottom_int : Number of |
| occurrences when all input buffers full | | |
| stat64_rxClass1Frames | 0 | top_int : Number of class 1 |
| frames received | 0 | bottom_int : Number of class 1 |
| frames received | | |
| stat64_aveTxFrameSize | 0 | Average Tx Frame size |
| stat64_aveRxFrameSize | 0 | Average Rx Frame size |
| Lr_in | 0 | top_int |
| | 0 | bottom_int |
| 0ls_in | 0 | top_int |
| | 0 | bottom_int |
| Lr_out | 0 | top_int |
| | 0 | bottom_int |
| 0ls_out | 0 | top_int |

```

Link_failure      0          bottom_int
                  0          top_int
Invalid_CRC       0          bottom_int
                  0          top_int
Invalid_word      0          bottom_int
                  0          top_int
Protocol_err      0          bottom_int
                  0          top_int
Loss_of_sig       0          top_int
                  0          bottom_int
Loss_of_sync      0          top_int
                  0          bottom_int
er_bad_os         0          top_int : Invalid ordered set
                  0          bottom_int: Invalid ordered set

```

```

portrouteshow 63
port address ID: 0x013f00
external unicast routing table:
  0: Embedded
 255: Embedded
internal unicast routing table:
  0: Embedded

```

portcamshow 63

```

-----
Port  SID used  DID used  SID entries  DID entries
63    0         0         000000      000000
-----

```

ptbufshow, ptcreditshow, ptdatashow, ptstatsshow 63

```

S:
S:VF Enable:          1
S:
S:C4 Global Variable:
S:-----
-----
S:trace_stop:        0
S:
S:C4 Phy Data Pointers: c4_phyp = 0xb6ac0000
S:-----
-----
S:tndep              0xbb833000      pt
  0x43028007
S:proto_phyp         0xb8807120      phy_cfg
0xb6ac1040
S:c4_chp              0x97e28000      c4_lgcp
0x97f64000
S:c4_phy_regp        0x81c38000      proc_dir
0xb8514dc0
S:-----
-----
S:magic_id           0xc4345678      num_port_timer      12

```

| | | | |
|----------------------------|------------|-----------------------|-----|
| S:prev_if_id | 0x43020007 | S:ftx | 0 |
| tov | 0 | | |
| S:initialized | 0 | port_idx | 7 |
| S:ui_idx | 63 | slot_no | |
| 0 | | | |
| S:blade_idx | 7 | sw_usr_ports | 400 |
| S:unused | 0 | intr_debounced | |
| 0 | | | |
| S:aec_status | 0x0 | reason_code | |
| 0 | | | |
| S:debug | 0x00000004 | debug_trc_line | 0 |
| S:rxbuf_list_head | 0xffffffff | rxbuf_list_tail | |
| 0xffffffff | | | |
| S:isAePort | 0 | port_misc_data | |
| 0 | | | |
| S:num_fault1_rx_disc | 0 | num_fault2_rx_disc | 0 |
| S:p_lli_cause0 | 0 | p_sig_regained | 0 |
| S:p_sync_regained | 0 | enc_out | |
| 0x0 | | | |
| S:cached_fps_status | 0 | cached_sts_status | 0 |
| S:cached_er_crc_good_eof | 0 | cached_er_too_long | 0 |
| S:cached_er_bad_os | 0 | | |
| S:cached_er_trunc | 0 | | |
| cached_tot_er_crc_good_eof | 0 | | |
| S:num_pt_excess_intr | 0 | num_no_fid | 0 |
| S:num_fault1_cnt | 0 | num_fault2_cnt | |
| 0 | | | |
| S:num_fault_lip | 0 | num_fault_lli | 0 |
| S:num_fault_rx_fifo | 0 | num_fault_hss | 0 |
| S:num_fault_bwait | 0 | lli_intr_prim | |
| 0 | | | |
| S:num_sw_link_to | 0 | | |
| be_link_err_mon_count | 0 | | |
| S:ecb_enc_enabled | 0 | ecb_comp_enabled | |
| 0 | | | |
| S:ecb_rsv_enc | 0 | ecb_rsv_comp | 0 |
| S:ecb_enc_bm | 0x0 | ecb_key_index | |
| 0xffffffff | | | |
| S:fab_idx | 4 | | |
| S:num_be_lto | 0 | lto_count_reset_intvl | |
| 0 | | | |
| S:lr_count_reset_intvl | 0 | num_be_lr | |
| 0 | | | |
| S:num_fault_qsfp | 0 | check_lto | |
| 0 | | | |
| S:credit_loaded | 0 | num_credit_overrun | |
| 0 | | | |
| S:fec_enabled | 0x0 | fec_los_to_flag | 0x0 |
| S:phy_stats_clear_ts | 1725611419 | pcs_err_online | |
| 0 | | | |
| S:pcs_err_light_det | 0 | pcs_err_ignore | |
| 0 | | | |
| S:pcs_blk_err | 0 | pcs_hiber | 0 |
| S:phy_port_status | 0 | ecb_enc_lr_count | |

```

0
S:dport_mode 0 avoid_lto_det 0
S:sn_debounced 0x0 sn_started_kr_reqd 0
S:major_timer_started 0x0 ready_bm 0x0
S:parln_1_bm 0x0 parln_0_bm 0x0
S:be_los_of_sync_event_intvl 0
be_los_of_sync_event 0
S:errataPtenable_cntr 0 errataPoll_cntr
0
S:jda_rx_sig_loss_det 0 jda_rx_sig_loss_cnt
0
S:encrypt_blk_error 0
S:
S: c4_trunk
S:=====
S:mark_ts 0x0 deskew 0x0
S:master_phyp 0x0
S:
S:adelay[00]: 0x00000000 0x00000000 0x00000000 0x00000000
S:adelay[04]: 0x00000000 0x00000000 0x00000000 0x00000000
S:
S: c4_buf
S:=====
S:tx_csc 0 rx_csc
0
S:ld_vc_credits 0 tx_flag 0x0
S:alloc_buffers 0 req_buffers 0
S:est_buffers 20 ld_use_est 0
S:bb_sc_n 0 rx_bb_sc_n
0
S:data_cr 5 nondata_cr
6
S:cr_enable 0
S:ld_nondata_cr 6 tnodep
0xbb8330e0
S:tx_credits[0] 0 0 0 0 0 0 0 0
S:tx_credits[8] 0 0 0 0 0 0 0 0
S:tx_credits[16] 0 0 0 0 0 0 0 0 0
S:tx_credits[24] 0 0 0 0 0 0 0 0 0
S:tx_credits[32] 0 0 0 0 0 0 0 0 0
S:rx_credits[0] 0 0 0 0 0 0 0 0
S:rx_credits[8] 0 0 0 0 0 0 0 0
S:rx_credits[16] 0 0 0 0 0 0 0 0 0
S:rx_credits[24] 0 0 0 0 0 0 0 0 0
S:rx_credits[32] 0 0 0 0 0 0 0 0 0
S:tx_mbc[0] 0 0 0 0 0 0 0 0
S:tx_mbc[8] 0 0 0 0 0 0 0 0
S:tx_mbc[16] 0 0 0 0 0 0 0 0
S:tx_mbc[24] 0 0 0 0 0 0 0 0
S:tx_mbc[32] 0 0 0 0 0 0 0 0
S:rx_mbc[0] 0 0 0 0 0 0 0 0
S:rx_mbc[8] 0 0 0 0 0 0 0 0
S:rx_mbc[16] 0 0 0 0 0 0 0 0
S:rx_mbc[24] 0 0 0 0 0 0 0 0

```

```

S:rx_mbc[32]    0    0    0    0    0    0    0    0
S:
S:C4 Chip Variables: c4_phyp->c4_chp = 0x97e28000
S:-----
-----
S:version = 2.1
S:magic_id      0xc4234567      init_state      0x8
S:reset_reg_mem 0x1
S:ch_int0_en_bm 0x0      intr0_cause     0x0
S:ch_int1_en_bm 0x0      intr1_cause     0x0
S:ch_int2_en_bm 0x0      intr2_cause     0x0
S:ch            0x43010080      ch_cfg
0xb7013ba0
S:raslog_hndl.hndl 0x0      obj_halted      0x0
S:c4_chip_regp  0x80000000      c4_fpg_regp
0x81800000
S:num_chip_timer 0x5
S:hi_task_bm    0x0      lo_task_bm      0x0
S:c4_deferq.q_head 0x0      c4_deferq.q_tail 0x0
S:c4_tmrq.q_head 0x0      c4_tmrq.q_tail  0x0
slot_no        0
S:chip_inst     0      chip_idx        0
S:pll_initialized      1
pll_serdes_initialized 1
S:init_tries      0      init_ptEnableBM
0xba01b488
S:tick_polling    0xb980c9c0      sec_polling
0xb980c960
S:bb_fid          129
S:ecb_key_bm[0]   0x0      ecb_key_bm[1]   0x0
S:ecb_key_bm[2]   0x0      ecb_key_bm[3]   0x0
S:is_chip_enc_enabled
is_chip_comp_enabled 0x0
S:ftb_rsrcp->ftb_flags 0x0      act_rsrcp->act_flag 0x1
S:lue_rsrcp->lue_flags[0] 0x0      lue_rsrcp-
>lue_flags[1] 0x0
S:c4_phyp[00]: 0xb6ab0000 0xb6ab2080 0xb6ab4100 0xb6ab6180
S:c4_phyp[04]: 0xb6ab9040 0xb6abb0c0 0xb6abd140 0xb6ac0000
S:c4_phyp[08]: 0xb6ac2080 0xb6ac4100 0xb6ac6180 0xb6ac9040
S:c4_phyp[12]: 0xb6acbc0c 0xb6acd140 0xb6ad0000 0xb6ad2080
S:c4_phyp[16]: 0xb6ad4100 0xb6ad6180 0xb6ad9040 0xb6adb0c0
S:c4_phyp[20]: 0xb6add140 0xb6ae0000 0xb6ae2080 0xb6ae4100
S:c4_phyp[24]: 0xb6ae6180 0xb6ae9040 0xb6aeb0c0 0xb6aed140
S:c4_phyp[28]: 0xb6af0000 0xb6af2080 0xb6af4100 0xb6af6180
S:c4_phyp[32]: 0xb6af9040 0xb6afb0c0 0xb6afd140 0xb6b00000
S:c4_phyp[36]: 0xb6b02080 0xb6b04100 0xb6b06180 0xb6b09040
S:c4_phyp[40]: 0xb6b0b0c0 0xb6b0d140 0xb6b10000 0xb6b12080
S:c4_phyp[44]: 0xb6b14100 0xb6b16180 0xb6b19040 0xb6b1b0c0
S:c4_phyp[48]: 0xb6b1d140 0xb6b20000 0xb6b22080 0xb6b24100
S:c4_phyp[52]: 0xb6b26180 0xb6b29040 0xb6b2b0c0 0xb6b2d140
S:c4_phyp[56]: 0xb6b30000 0xb6b32080 0xb6b34100 0xb6b36180
S:c4_phyp[60]: 0xb6b39040 0xb6b3b0c0 0xb6b3d140 0xb6b40000
S:c4_lgcp[00]: 0x97f48000 0x97f4c000 0x97f50000 0x97f54000
S:c4_lgcp[04]: 0x97f58000 0x97f5c000 0x97f60000 0x97f64000

```

```

S:c4_lgcp[08]: 0x97f68000 0x97f6c000 0x97f70000 0x97f74000
S:c4_lgcp[12]: 0x97f78000 0x97f7c000 0x97f80000 0x97f84000
S:c4_lgcp[16]: 0x97f88000 0x97f8c000 0x97f90000 0x97f94000
S:c4_lgcp[20]: 0x97f98000 0x97f9c000 0x97fa0000 0x97fa4000
S:c4_lgcp[24]: 0x97fa8000 0x97fac000 0x97fb0000 0x97fb4000
S:c4_lgcp[28]: 0x97fb8000 0x97fbc000 0x97fc0000 0x97fc4000
S:c4_lgcp[32]: 0x97fc8000 0x97fcc000 0x97fd0000 0x97fd4000
S:c4_lgcp[36]: 0x97fd8000 0x97fdc000 0x97fe0000 0x97fe4000
S:c4_lgcp[40]: 0x97fe8000 0x97fec000 0x97ff0000 0x97ff4000
S:c4_lgcp[44]: 0x97ff8000 0x97ffc000 0x8e000000 0x8e004000
S:c4_lgcp[48]: 0x8e008000 0x8e00c000 0x8e010000 0x8e014000
S:c4_lgcp[52]: 0x8e018000 0x8e01c000 0x8e020000 0x8e024000
S:c4_lgcp[56]: 0x8e028000 0x8e02c000 0x8e030000 0x8e034000
S:c4_lgcp[60]: 0x8e038000 0x8e03c000 0x8e040000 0x8e044000
S:chip_timers[00]: 0xb980c720 0xb980c780 0xb980c7e0 0xb980c840
S:chip_timers[04]: 0xb980c8a0 0xb980c900
S:disc_trap_enable_required      0x0          rxlp_disc_log_stop
          0x0
S:curr_rxlp_frm_cnt      0x0          curr_rxlp_disc_frm_cnt  0x0
S:sw_disc_frm_cnt      0x0          last_disc_frm_cnt      0x0
S:txq_nopop_pr_cnt      0x0          pollErrataDfe_ptBM
0xba01b4b0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][0]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][1] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_EC][2]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][0] 0x0
S:ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][1]      0x0
ftb_rsrcp->chip_ref[FTB_REF_CHP_NRC][2] 0x0
S:
S:C4 Logical Port Variables
S:-----
-----
S:c4_lgc_regp      0x81c38000
S:c4_phyp:
S:      0xb6ac0000      0x0          0x0          0x0

S:      0x0          0x0          0x0          0x0

S:master_phyp      0xb6ac0000      if_id
0x43020007
S:min_phyp      0x0          max_phyp      0x0
S:num_phy_ports      1          lgc_num      7
S:num_iu_to      0          sw_txq_bm
0
S:port_fid      129          unused      0
S:port_group      0          lgc_stats_clear_ts
1725611419
S:domain_tbl_sel      0          area_tbl_sel
0
S:egid_tbl_sel      0
S:serv_lo_bm      0x0
S:
S:Proto Phy Variables:
S:-----

```

```

-----
S:magic_id          0xc4123456      asic_phyp
0xb6ac0000
S:port_id          0x43028007      phy_cfg
0xb6ac1040
S:upsm_hdl        0xb8011640      physm_hdl
0xb80113c0
S:ov_sns_hdl      0xb8011280      sw_sns_hdl
0xb8011320
S:ov_lks_hdl      0xb8011460      sw_lks_hdl
0xb8011500
S:trks_hdl        0xb80115a0      lr_flag          0x0
S:lr_active        0x0          qsf_txr_rate_sel
0x0

S:
S:UPSM            UP00: UPST_PORT_DISABLED  --> UP00: UPST_PORT_DISABLED
S:SNSM(OV)        SN00: OV_SNST_STOPPED      --> SN00: OV_SNST_STOPPED
S:SNSM(SW)        SW00: SW_SNST_STAGE_WS  --> SW00: SW_SNST_STAGE_WS
S:PHYSM           PP00: PHYST_STOPPED      --> PP00: PHYST_STOPPED
S:LKSM(OV)        LK00: OV_LKST_INACTIVE  --> LK00: OV_LKST_INACTIVE
S:LKSM(SW)        SW13: INACTIVE          --> SW13: INACTIVE
S:TRKSM           TRK0: TRKST_INIT        --> TRK0: TRKST_INIT
S:
S:physm variables:
S:-----
-----
S:proto_phyp      0xb8807120      physm_hdl
0xb80113c0
S:force_offline   0          copper          0
S:fault_reason    0: UNKNOWN
S:phy_media_present 0
S:
S:sns variables:
S:-----
-----
S:speed          0xff          proto_phyp
0xb8807120
S:hw_sn_tries_left 0x0          sw_sn_tries_left 0x0
S:curr_txsp_count 0x0          curr_tx_indx
S:tx_max         0x0
0x0
S:curr_tx        0x0          curr_rxsp_count
0x0
S:rx_max         0x0          curr_rx_indx
0x0
S:curr_rx        0x0          rx_mem
0x0
S:rxsp_rec_count 0x0
S:nc_start       0x0          tx_start          0x0
S:sync_start     0x0          sync_present      0x0
S:diag_auto      0x0          diag_speed        0xff
S:striped_wd_tov 3000         hw_wd_tov
3000
S:step           0x0          qsf28_speed_mode

```



```

S:pci_abort_thresh      10                pci_err_thresh      5
S:excess_chintr_thresh  8                sw_err_thresh      20
S:err_sample_period    300              intr_sleep
20000
S:frame_timeout        2500                proxy_dev          16384
S:vf_route             81920              qos                2048
S:stats                2048              f_redirect         2048
S:rsp_trap             2048              lun_zoning         20480
S:area_mode            0                ftb_max_loop[0]   0
S:ftb_max_loop[1]     6                ftb_max_loop[2]   9
S:ftb_max_loop[3]    10                ftb_max_loop[4]  10
S:ftb_max_loop[5]     5                ftb_max_loop[6]   6
S:ftb_seg_size[0]     0                ftb_seg_size[1]  16384
S:ftb_seg_size[2]    65536              ftb_seg_size[3]
16384
S:ftb_seg_size[4]    16384              ftb_seg_size[5]
65536
S:ftb_seg_size[6]    16384              ftb_seg_base[0]   0
S:ftb_seg_base[1]    0                ftb_seg_base[2]
65536
S:ftb_seg_base[3]    16384              ftb_seg_base[4]
32768
S:ftb_seg_base[5]    131072             ftb_seg_base[6]
49152
asic_err_monitor_period1 300
asic_err_monitor_period2 86400
zone_chk_to_poll_period 25
zone_chk_class2_reject_tov
S:
S:c4_phy_cfg
S:-----
-----
S:version = 2.1
S:pt                   0x43028007         fab_ptr
0x9a800000
S:fabattr              0x9a8000d4         fab_iop
0x9a800050
S:cfgbm                0xbb832e04         port_ctrl
0xb6ac1058
S:pcap.pcap_bm         0x8d215547         pcap.pcap2_bm
0x2588289
S:pcap.pcap3_bm       0x1bebe0c
ui_idx                 63                S:slot_no
0
is_icl                 0                S:sw_usr_ports    400
S:neg_speed            0 0 0 0 0 0
S:my_domain            0x1                port_mode          0x0
S:hw_sn_maxtries      100                sw_sn_maxtries
0
S:hw_link_maxtries    10                sw_link_maxtries  5
S:rx_cyc_tov          28                rttov             300
S:bufrdy_tov          300              busybuf_tov       286
S:mark_tov            300              lksm_tov          3000

```

```

S:buf_dealloc_wait      4          hw_wd_tov      3000
S:hw_lk_train_tov      540          hw_lk_test_tov
    150
S:syswait_tx_12_lips   1          lip_rx_tov     55
S:al_time_tov          15          lp_tov         2000
S:intr_tries_port      500          intr_mod_debounce
    250
S:intr_lsrflt_debounce 500          intr_efifo_debounce 100
S:port_no_fid          3          excess_ptintr_thresh 8
S:port_fault1_thresh  100          port_fault1_spur_thresh 250
S:port_fault1_disc_thresh 500
port_fault1_disc_spur_thresh 1000
S:port_fault2_thresh  5          losync_tov     100
S:port_sw_link_to     15          en_8g_scramble
    1
frc_hw_sn_mode         0x1
S:enc_poll_thresh     0          fec_enable
    0
S:fec_in_sync_to      50          fec_in_sync_try_max
    4
S:port_be_lto_threshold 100          port_be_lr_threshold
    2
S:be_cr_in_sync_to    5
port_credit_overrun_thresh 10
S:jda_sfp_losig_tov   400
jda_sfp_losig_try_max 30
S:striped_wd_tov      3000
no_sync_debounce      1200
S:
S:    fab_iop
S:=====
S:fab_iop->interop_mode 0x0          fab_iop->lab_mode 0x0
S:fab_iop->fl_bbc      0x0          fab_iop->fl_fan
    0x0
S:fab_iop->fl_cls      0x4          fab_iop->fl_rscn
    0x0
S:fab_iop->domain_id_offset 0x60          fab_iop-
>mcdt_fabric_mode     0x0
S:fab_iop->mcdt_default_zone 0x0          fab_iop-
>mcdt_safe_zone       0x0
S:
S:    port_ctrl
S:=====
S:port_ctrl.port_type  1          port_ctrl.port_grp  0
S:port_ctrl.port_number 63          port_ctrl.vc_mode   1
S:
S:    port_ctrl.lcap
S:=====
S:has_serdes           0          has_media          1
S:topology             1          skip_nego          0
S:skip_pnego           0          skip_init_event    0
S:en_shim              0          speed_neg
    1
S:loop_back            0          num_speeds         5

```

```

S: fec_enable          0
S:
S:   port_ctrl.speed_list array
S: =====
S: speed_list[0].auto_neg  1    speed_list[0].lnk_speed  0x0000000a
S: speed_list[1].auto_neg  1    speed_list[1].lnk_speed  0x00000008
S: speed_list[2].auto_neg  1    speed_list[2].lnk_speed  0x00000006
S: speed_list[3].auto_neg  1    speed_list[3].lnk_speed  0x00000005
S: speed_list[4].auto_neg  1    speed_list[4].lnk_speed  0x00000003
S: speed_list[5].auto_neg  0    speed_list[5].lnk_speed  0x00000000
S:
S:   port_ctrl.cm
S: =====
S: port_ctrl.cm.num_vcs          8
S: port_ctrl.cm.min_bufs        8
S: port_ctrl.cm.cr_shar_bufs    0
S: port_ctrl.vc_alloc
S: port_ctrl.vc_alloc          2 0 1 1 1 1 1 1
S: port_ctrl.vc_alloc          0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S: port_ctrl.norm_vc_alloc
S: port_ctrl.norm_vc_alloc      4 0 5 5 5 5 1 1
S: port_ctrl.norm_vc_alloc      0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0
S: port_ctrl.cm.skip_bb_credit    0
S: port_ctrl.cm.use_shim_based_sublist  0
S:
S:   port_ctrl.serdes_set
S: =====
S: serdes_type          0x8
S: serdes_data_t.ibm_hss_serdes.tx_drive_power  0x0
S: serdes_data_t.ibm_hss_serdes.pre_emphasis_b_sign  0x1
S: serdes_data_t.ibm_hss_serdes.pre_emphasis_b  0x0
S: serdes_data_t.ibm_hss_serdes.pre_emphasis_a  0x0
S: serdes_data_t.ibm_hss_serdes.rxeq          0x0
S:
S:   cfgbm
S: =====
S: old_distance          0x0          gport_lockdown          0x0
S: tport                0x1          speed                    0x0
S: disable_eport        0x0          fcacc                   0x0
S: lport_lockdown      0x0          0x0                    priv_lport_lockdown
0x0
S: vcxlt_linit          0x0          delay_flogi             0x0
S: isl_interop          0x0          distance                0x0
S: BufStarvFlag        0x0          credit_sharing          0x0
S: lport_halfduplex    0x0          lport_fairness          0x0
S: soft_neg            0x0          asn_frc_hwretry        0x0
S: cr_recov            0x0          fport_buffers           0x0
S: export              0x0          0x0                    export_mode
0x0
S: csctl_en            0x0          mirror_port             0x0
S: fault_delay         0x0          non_dfe                 0x0
S: fec_configured*(0=ENAB)  0          fec_tts

```

```

0
S:port_persistently_disabled (permanently) 0 (0)
S:
S:   cfg property
S:=====
S:priv_pcfg_bm          0x00000000    lgcl_pcfg_bm
0xbb832e44
S:fport_buffer         0x00000000
S:
S:
S:C4 Discard Cntrs: rxlp_stats = 0xb6ac03b0
S:-----
-----
S:disc_mcast_wka      0x0          disc_inv_did          0x0
S:disc_cl1_cl4       0x0          disc_sid_chk_fail    0x0
S:disc_inv_dom_egid_txpt 0x0          disc_vft_hop_cnt_1
0x0
S:disc_classf        0x0          disc_fcp_cdb_inv     0x0
S:disc_vfid_trap_enabled 0x0
disc_vfid_hdr_chk_fail 0x0
S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err 0x0
S:disc_shim_cksum_fail 0x0          disc_fed_edit_cmd_err 0x0
S:disc_ftb_vm_mode   0x0          disc_ftb_agnt2_miss  0x0
S:disc_ecb_de_pad_err 0x0          disc_ecb_de_tag_err  0x0
S:disc_ecb_de_seq_err 0x0          disc_ecb_err          0x0
S:disc_ftb_type4_match 0x0          disc_fcp_rsp_ftb_type4 0x0
S:disc_fcp_rsp_ftb_type4 0x0          disc_ftb_type5_match
0x0
S:disc_ftb_type3_match 0x0          disc_els_ftb_type3   0x0
S:disc_ftb_type1_match 0x0          disc_els_rsp_ex_port 0x0
S:disc_inv_drp_dps   0x0          disc_did_lookup_miss 0x0
S:disc_ftb_type2_match 0x0          disc_trpd_plogi_pdisc 0x0
S:disc_type2_lookup_miss 0x0          disc_ftb_type6_match
0x0
S:disc_els_rep_ex_port 0x0          disc_els_sid_lkup_bit1 0x0
S:disc_els_sid_lkup_bit0 0x0
disc_bls_frm_trap_bit1 0x0
S:disc_ftb_token_err 0x0          disc_asic_internal_err 0x0
S:disc_hard_zone_miss 0x0          disc_lun_zone_miss   0x0
S:disc_flt_frame_disc 0x0          disc_flt_parity_err  0x0
S:disc_frame_marked_du 0x0          disc_frame_marked_to  0x0
E:Connection type: FE
E:Port type: E_port
E:Trunk port: No
E:Configured Speed: AUTO_SPEED_NEGO
E:Max Capable Speed: 32G
E:Current SNSM Speed: UNDEFINED
E:Hardware TX Speed: 32G (0x00000004)
E:Hardware RX Speed: 32G (0x00000040)
E:
E:Interrupts: 0          Link_failure: 0
Loss_of_sync: 0          Loss_of_sig: 0
E:Lli: 0          Invalid_word: 0
E:trapped_frm: 0          fwd_status_ok: 0

```

```

E: fwd_timeout: 0          fwd_tx_unavail: 0
E: fwd_unroutable: 0      fwd_zone_out: 0
E: fwd_other_err: 0      frm_err_discard: 0
E: Fltr listA: 0         Fltr listB: 0
E: Zone trap fwd: 0      Zone trap disc: 0
E: shim_csum: 0          RTE_perr: 0
E: Invalid_crc: 0        Delim_err: 0
E: Protocol_err: 0
E: Lr_in: 0              Lr_out: 0
E: Ols_in: 0             Ols_out: 0

```

filterportshow 63

FILTER DATA

Shadow settings:

```

Filter Enable: 0x00000000
Redir RAM[0]: 0x00000000
Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass: 0x00000000

```

Real settings:

```

Enable RAM: 0x00000000, 0x00000000
Redir RAM[0]: 0x00000000

```

Redir RAM[1]: 0x00000000
Redir RAM[2]: 0x00000000
Redir RAM[3]: 0x00000000
Redir RAM[4]: 0x00000000
Redir RAM[5]: 0x00000000
Redir RAM[6]: 0x00000000
Redir RAM[7]: 0x00000000
Redir RAM[8]: 0x00000000
Redir RAM[9]: 0x00000000
Redir RAM[10]: 0x00000000
Redir RAM[11]: 0x00000000
Redir RAM[12]: 0x00000000
Redir RAM[13]: 0x00000000
Redir RAM[14]: 0x00000000
Redir RAM[15]: 0x00000000
Redir RAM[16]: 0x00000000
Redir RAM[17]: 0x00000000
Redir RAM[18]: 0x00000000
Redir RAM[19]: 0x00000000
Redir RAM[20]: 0x00000000
Redir RAM[21]: 0x00000000
Redir RAM[22]: 0x00000000
Redir RAM[23]: 0x00000000
Redir RAM[24]: 0x00000000
Redir RAM[25]: 0x00000000
Redir RAM[26]: 0x00000000
Redir RAM[27]: 0x00000000
Redir RAM[28]: 0x00000000
Redir RAM[29]: 0x00000000
Redir RAM[30]: 0x00000000
Redir RAM[31]: 0x00000000
Bypass RAM: 0x00000000

Shadowed filters:

Filter 0: Not Installed (MIRROR1)(LISTA)
c4_fldenable[0] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[0] = 0x00000000,c4_fltr_config[0] = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
c4_fldenable[1] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[1] = 0x00000000,c4_fltr_config[1] = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
c4_fldenable[2] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[2] = 0x00000000,c4_fltr_config[2] = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
c4_fldenable[3] = 0x00000000 0x00000000 0x00000000
0x00000000
c4_fldnegate[3] = 0x00000000,c4_fltr_config[3] = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
c4_fldenable[4] = 0x00000000 0x00000000 0x00000000
0x00000000

```
    c4_fldnegate[4] = 0x00000000,c4_fltr_config[4] = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
    c4_fldenable[5] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[5] = 0x00000000,c4_fltr_config[5] = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
    c4_fldenable[6] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[6] = 0x00000000,c4_fltr_config[6] = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
    c4_fldenable[7] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[7] = 0x00000000,c4_fltr_config[7] = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
    c4_fldenable[8] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[8] = 0x00000000,c4_fltr_config[8] = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
    c4_fldenable[9] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[9] = 0x00000000,c4_fltr_config[9] = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
    c4_fldenable[10] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[10] = 0x00000000,c4_fltr_config[10] =
0x00000000
Filter 11: Not Installed (SIM)(LISTA)
    c4_fldenable[11] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[11] = 0x00000000,c4_fltr_config[11] =
0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
    c4_fldenable[12] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[12] = 0x00000000,c4_fltr_config[12] =
0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
    c4_fldenable[13] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[13] = 0x00000000,c4_fltr_config[13] =
0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
    c4_fldenable[14] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[14] = 0x00000000,c4_fltr_config[14] =
0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
    c4_fldenable[15] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[15] = 0x00000000,c4_fltr_config[15] =
0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
    c4_fldenable[16] = 0x00000000 0x00000000 0x00000000
0x00000000
```

```
    c4_fldnegate[16] = 0x00000000,c4_fltr_config[16] =
0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
    c4_fldenable[17] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[17] = 0x00000000,c4_fltr_config[17] =
0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
    c4_fldenable[18] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[18] = 0x00000000,c4_fltr_config[18] =
0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
    c4_fldenable[19] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[19] = 0x00000000,c4_fltr_config[19] =
0x00000000
Filter 20: Not Installed (PERF5)(LISTA)
    c4_fldenable[20] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[20] = 0x00000000,c4_fltr_config[20] =
0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
    c4_fldenable[21] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[21] = 0x00000000,c4_fltr_config[21] =
0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
    c4_fldenable[22] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[22] = 0x00000000,c4_fltr_config[22] =
0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
    c4_fldenable[23] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[23] = 0x00000000,c4_fltr_config[23] =
0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
    c4_fldenable[24] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[24] = 0x00000000,c4_fltr_config[24] =
0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
    c4_fldenable[25] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[25] = 0x00000000,c4_fltr_config[25] =
0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
    c4_fldenable[26] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[26] = 0x00000000,c4_fltr_config[26] =
0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
    c4_fldenable[27] = 0x00000000 0x00000000 0x00000000
```



```
0x00000000
    c4_fldnegate[27] = 0x00000000,c4_fltr_config[27] =
0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
    c4_fldenable[28] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[28] = 0x00000000,c4_fltr_config[28] =
0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
    c4_fldenable[29] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[29] = 0x00000000,c4_fltr_config[29] =
0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    c4_fldenable[30] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[30] = 0x00000000,c4_fltr_config[30] =
0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    c4_fldenable[31] = 0x00000000 0x00000000 0x00000000
0x00000000
    c4_fldnegate[31] = 0x00000000,c4_fltr_config[31] =
0x00000000
```

Real filters:

```
Filter 0: Not Installed (MIRROR1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 1: Not Installed (MIRROR2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 2: Not Installed (MIRROR3)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 3: Not Installed (MIRROR4)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 4: Not Installed (AEPORT_NON_MIRR_DROP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 5: Not Installed (ZONING TRAP)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 6: Not Installed (FCR_EXPORT_DC)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
```

fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 7: Not Installed (TIN TRAP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 8: Not Installed (FICON CUP)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 9: Not Installed (FICON CUP DST)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 10: Not Installed (WELL KNOWN ADDR)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 11: Not Installed (SIM)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 12: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 13: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 14: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 15: Not Installed (UNUSED)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 16: Not Installed (PERF1)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 17: Not Installed (PERF2)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 18: Not Installed (PERF3)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 19: Not Installed (PERF4)(LISTA)
fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 20: Not Installed (PERF5)(LISTA)

```
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 21: Not Installed (PERF6)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 22: Not Installed (PERF7)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 23: Not Installed (PERF8)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 24: Not Installed (PERF9)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 25: Not Installed (PERF10)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 26: Not Installed (PERF11)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 27: Not Installed (PERF12)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 28: Not Installed (OPM1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 29: Not Installed (OPM2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 30: Not Installed (IPM1)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000
Filter 31: Not Installed (IPM2)(LISTA)
    fld enable ram = 0x00000000, 0x00000000, 0x00000000,
0x00000000,
    fld negate ram = 0x00000000, fltr config ram = 0x00000000

Filter dirty indicator: 0x00000000
Performance filters: 0
Port Mirror filters: 0 (0x0)
```

FIELD DATA

Shadowed fields:

```
fldoffset[0] = 0x00, fldmask[0] = 0x00, fldvalue_dyna[0]:0x00 0x00
0x00 0x00
fldcontrol[0].inuse = 0x0  fldcontrol[0].refcnt = 0x00 0x00 0x00
0x00
fldoffset[1] = 0x00, fldmask[1] = 0x00, fldvalue_dyna[1]:0x00 0x00
0x00 0x00
fldcontrol[1].inuse = 0x0  fldcontrol[1].refcnt = 0x00 0x00 0x00
0x00
fldoffset[2] = 0x00, fldmask[2] = 0x00, fldvalue_dyna[2]:0x00 0x00
0x00 0x00
fldcontrol[2].inuse = 0x0  fldcontrol[2].refcnt = 0x00 0x00 0x00
0x00
fldoffset[3] = 0x00, fldmask[3] = 0x00, fldvalue_dyna[3]:0x00 0x00
0x00 0x00
fldcontrol[3].inuse = 0x0  fldcontrol[3].refcnt = 0x00 0x00 0x00
0x00
fldoffset[4] = 0x00, fldmask[4] = 0x00, fldvalue_dyna[4]:0x00 0x00
0x00 0x00
fldcontrol[4].inuse = 0x0  fldcontrol[4].refcnt = 0x00 0x00 0x00
0x00
fldoffset[5] = 0x00, fldmask[5] = 0x00, fldvalue_dyna[5]:0x00 0x00
0x00 0x00
fldcontrol[5].inuse = 0x0  fldcontrol[5].refcnt = 0x00 0x00 0x00
0x00
fldoffset[6] = 0x00, fldmask[6] = 0x00, fldvalue_dyna[6]:0x00 0x00
0x00 0x00
fldcontrol[6].inuse = 0x0  fldcontrol[6].refcnt = 0x00 0x00 0x00
0x00
fldoffset[7] = 0x00, fldmask[7] = 0x00, fldvalue_dyna[7]:0x00 0x00
0x00 0x00
fldcontrol[7].inuse = 0x0  fldcontrol[7].refcnt = 0x00 0x00 0x00
0x00
fldoffset[8] = 0x00, fldmask[8] = 0x00, fldvalue_dyna[8]:0x00 0x00
0x00 0x00
fldcontrol[8].inuse = 0x0  fldcontrol[8].refcnt = 0x00 0x00 0x00
0x00
fldoffset[9] = 0x00, fldmask[9] = 0x00, fldvalue_dyna[9]:0x00 0x00
0x00 0x00
fldcontrol[9].inuse = 0x0  fldcontrol[9].refcnt = 0x00 0x00 0x00
0x00
fldoffset[10] = 0x00, fldmask[10] = 0x00, fldvalue_dyna[10]:0x00 0x00
0x00 0x00
fldcontrol[10].inuse = 0x0  fldcontrol[10].refcnt = 0x00 0x00 0x00
0x00
fldoffset[11] = 0x00, fldmask[11] = 0x00, fldvalue_dyna[11]:0x00 0x00
0x00 0x00
fldcontrol[11].inuse = 0x0  fldcontrol[11].refcnt = 0x00 0x00 0x00
0x00
fldoffset[12] = 0x00, fldmask[12] = 0x00, fldvalue_dyna[12]:0x00 0x00
0x00 0x00
```


0x00000000
0x00000000
0x00000000
0x00000000

Field dirty indicator: 0x00000000

FDB reference count fdb: 0 [0 0 0 0]
FDB reference count fdb: 1 [0 0 0 0]
FDB reference count fdb: 2 [0 0 0 0]
FDB reference count fdb: 3 [0 0 0 0]
FDB reference count fdb: 4 [0 0 0 0]
FDB reference count fdb: 5 [0 0 0 0]
FDB reference count fdb: 6 [0 0 0 0]
FDB reference count fdb: 7 [0 0 0 0]
FDB reference count fdb: 8 [0 0 0 0]
FDB reference count fdb: 9 [0 0 0 0]
FDB reference count fdb: 10 [0 0 0 0]
FDB reference count fdb: 11 [0 0 0 0]
FDB reference count fdb: 12 [0 0 0 0]
FDB reference count fdb: 13 [0 0 0 0]
FDB reference count fdb: 14 [0 0 0 0]
FDB reference count fdb: 15 [0 0 0 0]
FDB reference count fdb: 16 [0 0 0 0]
FDB reference count fdb: 17 [0 0 0 0]
FDB reference count fdb: 18 [0 0 0 0]
FDB reference count fdb: 19 [0 0 0 0]

Filter counters:

Filter counter 0: 0 (MIRROR1)
Filter counter 1: 0 (MIRROR2)
Filter counter 2: 0 (MIRROR3)
Filter counter 3: 0 (MIRROR4)
Filter counter 4: 0 (AEPORT_NON_MIRR_DROP)
Filter counter 5: 0 (ZONING TRAP)
Filter counter 6: 0 (FCR_EXPORT_DC)
Filter counter 7: 0 (TIN TRAP)
Filter counter 8: 0 (FICON CUP)
Filter counter 9: 0 (FICON CUP DST)
Filter counter 10: 0 (WELL KNOWN ADDR)
Filter counter 11: 0 (SIM)
Filter counter 12: 0 (UNUSED)
Filter counter 13: 0 (UNUSED)
Filter counter 14: 0 (UNUSED)
Filter counter 15: 0 (UNUSED)
Filter counter 16: 0 (PERF1)
Filter counter 17: 0 (PERF2)
Filter counter 18: 0 (PERF3)
Filter counter 19: 0 (PERF4)
Filter counter 20: 0 (PERF5)
Filter counter 21: 0 (PERF6)
Filter counter 22: 0 (PERF7)
Filter counter 23: 0 (PERF8)
Filter counter 24: 0 (PERF9)
Filter counter 25: 0 (PERF10)

Filter counter 26: 0 (PERF11)
Filter counter 27: 0 (PERF12)
Filter counter 28: 0 (OPM1)
Filter counter 29: 0 (OPM2)
Filter counter 30: 0 (IPM1)
Filter counter 31: 0 (IPM2)

ACL DATA

Logical port 7: Hard Zoning disabled, Soft Zoning disabled
Zone type: WWN Zoning
Frames with hard zone miss: 0

*** Please use filterportshow on user port 56 to display ACL hash
tables and Mirroring resources of thischip.
***We show this data only for the first physical port which is an
external port.

real 0m7.423s
user 0m4.076s
sys 0m3.032s

Group End: start_fc_port_cmd
Mon Sep 9 08:47:27 UTC 2024
